Chapter 6

Conclusion and Future Scope

6.1 Introduction

The main objective of this thesis is to develop analytical models for the electrical characteristics of some gate-electrode and gate-oxide structure engineered homo/heterojunction double-gate (DG) TFETs. The effects of three different engineering techniques such as gate-electrode engineering, gate-oxide engineering, and source materials engineering on the electrical performance of the DG TFET structures have been investigated in the present thesis. The present chapter is devoted to summarize and conclude the works carried out in various chapters of this thesis. Finally, we will also outline some scopes for the future research related to the area considered in this thesis.

6.2 Chapter-Wise Summary and Conclusion

Chapter-1 introduces the CMOS scaling and their adverse short-channel effects (SCEs) on the performance of the MOS devices. Various non-classical MOSFET strictures have been briefly introduced to mitigate the short-channel effects. The tunnel field effect transistor (TFET) has been introduced as a potential non-classical MOS transistor for low-power VLSI applications due to their inherently low OFF-state current and much steeper subthreshold swing (SS) with value much lower than the minimum achievable value of 60 mV/decade in the conventional bulk MOSFETs. However, the low drain current and its dependence on the polarity of the applied gate bias (*i.e.,* ambipolar conduction) are the major limitations of the TFETs. Various

methods such as the gate-electrode engineering, gate-oxide engineering, and source-material engineering techniques for improving the drive current of the TFETs have been introduced. A detail literature survey has been carried out in this chapter for studying various techniques used for improving the ON-state current and minimizing the ambipolar conduction in the TFETs. Finally, based on the findings of the literature survey, the scopes of the present thesis have been outlined at the end of this chapter.

Chapter-2 includes the analytical modeling and ATLAS^{TM} based simulation for the electrical characteristics such as surface potential, drain current, and the threshold voltage of the DG TFETs with a vertical SiO_2/HfO_2 stacked gate-oxide structure. Parabolic approximation method has been used for solving the two-dimensional (2-D) Poisson's equation in the channel region to obtain the channel potential distribution of the device. The channel potential model includes the effect of depletion regions at source/channel and drain/channel junctions for better accuracy. The band-to-band tunneling generation rate has been expressed as a function of channel electric field derived from the channel potential of the device. The generation rate function has then been integrated analytically over the channel thickness to derive the drain current of the stacked-gate DG TFETs using the shortest tunneling path (L_t) concept. The maximum transconductance method has been used to extract the threshold voltage from the drain current of the device. The effects of various device parameters on the channel potential, drain current, and the threshold voltage of the proposed DG TFETs have been modeled and discussed in this chapter. The major observations can be summarized as follows.

- The analytical modeling of the potential function, electric field, threshold voltage and complete drain current of the SiO_2/high-k stacked gate-oxide structure based DG TFETs by considering both the effects of junction depletion

regions at the source/drain sides is reported possibly for the first time in this thesis.

- The variation of the surface potential along the channel is independent of the drain voltages (V_{DS}) except at the drain depletion region. This implies that the short-channel effects (SCEs) including the drain induced barrier lowering (DIBL) is nearly negligible in our proposed SiO_2/high-*k* stacked gate-oxide based DG TFETs structure.
- The respective depletion widths L_1 and L_3 at the source/channel and drain/channel junctions are V_{GS} dependent parameters. Thus their effects on the modeling of TFET characteristics can not be ignored.
- The drain current (I_d) is observed to be increased with high-*k* dielectric constant to the increased tunneling caused by the increased lateral electric field at the source/channel junction.
- The drain current (I_d) is observed to be decreased with channel thickness due to the decrease in the non-local BTBT volume of the device.
- The threshold voltage model derived from the drain current model using the maximum transconductance (TC) method is observed to be nearly independent of the channel length which implies a nearly zero threshold voltage roll-off in our proposed structure.
- A good agreement between the model results and commercially available ATLAS^{TM} based TCAD simulation data show the validity of our proposed analytical models developed in this chapter.

Chapter-3 presents the analytical modeling and ATLAS^{TM} based simulation for the electrical characteristics such as surface potential, drain current and threshold voltage of dual-material (DM) double-gate (DG) SiO_2/high-*k* stacked gate-oxide based TFET structures obtained by combining the concepts of both the gate-electrode (*i.e.*, dual material) engineering and gate-oxide engineering (*i.e.*, vertical SiO_2/HfO_2 stacked gate-oxide) in the DG TFETs. In the present DG TFET structure, the single-material (SM) gate-electrode considered in Chapter-2 has been replaced two metal-like materials of two different work functions connected in non-overlapped cascaded manner with the lower work function material at the source side to form the gate-electrode of the device. The potential function, drain current and threshold voltage of the proposed device have been modelled in the similar manner as considered in Chapter-3. It is shown that the drain current, subthreshold swing (SS), I_{ON}/I_{OFF} and ambipolar reduction characteristics can be significantly improved over the conventional DG TFETs by selecting proper work function values of the gate electrode materials. The effects of different device parameters like channel length, tunneling-to-auxiliary gate length ratio, channel thickness, doping concentration, etc. on the electrical characteristics of the device have been investigated in details. The major observations of this chapter can be outlined as follows:

- The work functions of the tunneling gate and auxiliary gates (*i.e.*, the gate electrode material with lower work function at the source and drain sides respectively) of the proposed device are observed to play significant roles in optimizing the drain current, I_{ON}/I_{OFF} ratio, ambipolar effect, and SS of the proposed DM DG TFETs.
- The I_{ON}/I_{OFF} ratio of the SM DG TFET with function 4.2 eV is higher than that of the DM DG TFET (*i.e.*, φ_t = 4.2eV and φ_a = 4.6 eV) and SM DG

TFET with work function 4.4 eV. However, the ambipolar conduction current of the proposed DM DG structure is the lowest among the above three DG TFET structures considered above.

- The values of channel length, tunneling-to-auxiliary gate length ratio and source doping concentration can be used to optimize the I_{ON}/I_{OFF} ratio and SS of the proposed DM DG TFETs. Thus, as compared to the SM DG TFETs considered in Chapter-2, the lengths of the tunneling and auxiliary gate-electrodes and their corresponding work functions in the proposed DM DG TFET structures can be used as additional parameters for the performance optimization of the TFETs.
- The proposed model is also found to be applicable for both the direct bandgap (*e.g.*, InAs) and indirect bandgap (Si) channel materials.
- Model results are found to be in good agreement with the commercially available SILVACO ATLAS^{TM} based TCAD simulation data.

Chapter-4 reports the analytical modeling of surface potential, drain current and threshold voltage of dual-material (DM) heterogeneous gate dielectric (HGD) double-gate (DG) TFETs by incorporating the features of both gate-electrode (*i.e.*, dual material) engineering and gate-oxide (*i.e.*, lateral SiO_2/HfO_2 stacked gate) engineering in a DG TFET with localized interface charges. The structure is obtained by replacing the vertical SiO_2/high-*k* stacked gate structure in DM DG TFET considered in Chapter-3 by the laterally connected SiO_2 and high-*k* in a non-overlapped cascaded manner. Following the parabolic-approximation technique of Chapter-2, the 2-D Poisson's equation has been solved for channel potential of the device by considering the effects of the localized charges near the source/channel junction, mobile charges in channel

region and charges of the depletion regions formed at source/channel and drain/channel junctions. The band-to-band tunneling (BTBT) generation rate has been developed by taking the effects of the electric fields at source/channel and drain/channel junctions. The drain current model for both the positive and negative gate voltages (*i.e.* including the ambipolar conduction region) has been derived by using the tangent line approximation (TLA) method. The threshold voltage model has been developed by using the concept of shortest tunneling path of the proposed DM-HGD DG TFET structure. The impact of localized interface charges on the drain current and threshold voltage by varying the device dimensions are also investigated. Some important observations of this chapter are briefly discussed in the following:

- The analytical modeling of surface potential, drain current and threshold voltage of DM-HGD DG TFETs by considering the effects of localized charges near the source/channel junction, mobile charges in channel and charges at the depletion regions at source/channel and drain/channel junctions is investigated possibly for the first time in this thesis.
- The dual-modulation nature (*i.e.,* intrinsic property) of the surface potential of the proposed TFET structure is also investigated in this chapter.
- The proposed drain current is found to be valid for all gate bias including the ambipolar conduction region of the device.
- Although the threshold voltage is observed to be increased at low drain voltages (V_{DS}), however it becomes nearly independent of V_{DS} at higher V_{DS} values possibly due to the dominant gate control over the device.
- For a fixed channel length, the threshold voltage roll-off against localized charge density is independent of the channel thickness of the proposed device.

- It has been observed that the drain current is highly affected by the localized charges at low gate bias voltages while the threshold voltage is observed to be highly affected by the localized charges at low drain bias voltages of the device.
- The model results are validated by finding a good matching between the model results and their corresponding ATLAS^{TM} based TCAD simulation data.

Chapter-5 presents the analytical modeling for the electrical characteristics of a vertical stacked gate-oxide SiO_2/high-*k* based double-gate (DG) heterojunction TFET (HJ TFET) structure obtained by replacing Si of the source by Ge or any other lower band gap material (while maintaining Si in both the channel and drain regions) in the DG TFET structure investigated in Chapter-2. All the electrical characteristics discussed in the previous chapters have also been investigated for the proposed DG HJ TFET with a vertical SiO_2/high-*k* gate oxide region. The surface potential model has been developed by considering the effects of accumulation/inversion charges as well as the charges of depletion regions at source/channel and drain/channel junctions. The tangent line approximation (TLA) method of Chapter-4 has been directly used to model the drain current of the device. Finally, the threshold voltage model has been developed by using the shortest tunneling path concept as discussed in Chapter-4. The proposed model has also been shown suitable for Si homojunction-based TFETs and silicon-on-insulator (SOI) based HJTFETs. Such a universal model can be very useful for the optimization of the electrical performance of various TFET structures. The effects of different device parameters such as the channel length, channel thickness, and doping concentration on the electrical characteristics of the proposed device have been investigated. The major observations of this chapter are discussed below:

- The analytical modeling of surface potential, drain current, and the threshold voltage of stacked gate-oxide SiO_2/HfO_2 based DG HJTFETs by considering charges of depletion regions (at source/channel and drain/channel junctions) and accumulation/inversion charges in the channel region has been investigated possibly for the first time in this thesis.
- The concept of TLA method has been used to calculate the drain current by numerically integrating the BTBT generation rate over the entire channel volume of the device as discussed in Chapter-4.
- The effects of electric field formation at the drain/channel interface at low gate and high drain bias voltages have been considered for improving the accuracy of the drain current model in the subthreshold region of operation of the device.
- The drain current for different channel lengths but for a fixed channel thickness shows that the proposed structure is best suitable for L = 50nm to achieve the maximum value of the I_{ON}/I_{OFF} current ratio.
- The threshold voltage (V_{th}) of the proposed device is observed to be nearly independent of the channel length. This implies that the proposed TFET structure has nearly zero threshold voltage roll-off.
- The proposed models developed for Ge(source)/Si(channel) based HJTFETs are also shown to be applicable for InAs(source)/GaSb (channel) based HJTFETs as well as for the silicon-on-insulator (SOI) based HJTFETs. Such a universal model can be very useful for the optimization of the electrical performance of various TFET structures.
- A good matching between our model results and ATLAS^{TM} based TCAD data confirms the validity of our proposed models.

6.3 Future Scope of Work

In this thesis, we have presented the 2-D analytical modeling for electrical characteristics of some gate-electrode and gate-oxide structure engineered homo/heterojunction double-gate (DG) TFETs. In this section, we will outline some future scopes of research related to the area of research carried out in this thesis which are given as follows:

- In the present work, we have considered channel thickness above 12 nm to avoid the quantum mechanical effects on the drain current of the TFETs. We have observed that the model results are deviated from the TCAD simulation data when the channel thickness above 10 nm is considered. Thus, a rigorous theoretical investigation is required for making the proposed models valid for all channel thickness even below 10 nm.
- The analysis of analog and RF performances of the gate-electrode-material and gate-oxide engineered homo/heterojunction double-gate (DG) TFETs proposed in this thesis may also be considered as an important future research.
- The equivalent circuit models for small-signal low-frequency as well as small-signal high-frequency applications of the gate-electrode and gate-oxide structure engineered home/heterojunction double-gate (DG) TFETs could be very useful for the design and simulation of various analog and digital circuits using the proposed TFET devices in this thesis.
- The modeling presented in this thesis for DG TFET may be extended for the Fin-TFETs, Tri-gate, and Gate-All-Around (GAA) TFETs. The concepts can also be applied to other non-classical MOSFET structures like the Junctionless Field Effect Transistors (JFETs) and Ring MOSFETs etc.

- A capacitance model of gate-electrode and gate-oxide structure engineered home/heterojunction double-gate (DG) TFETs could be developed.