Chapter 4

Analytical Model for Electrical Characteristics of Dual Metal Heterogeneous Gate Dielectric Double-Gate TFETs With Localized Interface Charges

4.1 Introduction

We have observed from the literature survey that the heterogeneous gate dielectric (HGD) based DG TFETs (obtained by replacing the conventional SiO_2 gate-oxide by the cascade connection of HfO_2 and SiO_2 in an non-overlapped manner in the DG TFETs) have better ON current and smaller subthreshold swing (SS) over the conventional SiO_2 dielectric based-DG TFETs [Choi and Lee (2010), Wang *et al.* (2016), and Gracia *et al.* (2017)]. Further, the scaling of the conventional TFETs are reported to be suffered from the interface donor/acceptor traps charges (*i.e.*, positive/negative localized charges) due to the presence of a high transverse electric field at the source/channel junction [Vishnoi and Kumar (2014), Mishra *et al.* (2016), Madan and Chaujar (2017)]. In addition, it is also observed from the literature survey of Chapter-1 that the surface potential of the TFETs becomes insensitive for high gate voltage and low drain voltage due to mobile charge carriers (*i.e.*, inversion /accumulation charge for p-/n- type channel material) in the channel [Wu *et al.* (2014), Xu *et al.* (2016), Mohammadi and Khaveh (2017)]. However, to the best of our knowledge, no compact models for surface potential, drain current and threshold voltage of the dual-material (DM) heterogeneous gate dielectric (HGD) DG TFETs

have been reported by taking all the effects of the localized charges near the source/channel junction due to high electric field, mobile charges of the accumulation/inversion regions in the channel, and depletion regions at source/channel and drain/channel junction into consideration.

The inherent capability of improving the ON-current, ambipolar conduction and subthreshold characteristics of the dual-material gate (DMG) structure in DG TFETs have already been shown in Chapter-3. In this Chapter, we will investigate the performance characteristics of a newly proposed DM-HGD DG TFET structure obtained by replacing the vertical SiO_2/high-*k* stacked oxide in the DM DG TFETs of Chapter-3 by the laterally connected SiO_2 and high-*k* gate-oxide structure in a cascaded and non-overlapped manner. We will attempt to develop a unified model for electrical characteristics of the DM-HGD DG TFETs by taking the effects of localized charges near the source/channel junction, mobile charges in channel region (for high gate and low drain bias) and charges in the depletion regions of the device. Our proposed model results have been matched with ATLAS^{TM} based TCAD simulation data for validation of our model. The layout of the present chapter is given as follows:

Section 4.2 deals with the modeling of the surface potential of our proposed DM-HGD DG TFET structure by considering the effects of localized charges near the source/channel junction, mobile charges in channel region and charges of depletion regions at the source/channel and drain/channel junctions as considered in Chapter-3. Based on surface potential model, electric field has been derived and used to calculate the BTBT generation rate at both source/channel and drain/channel junction. The tangent line approximation (TLA) method has been used to obtain the drain current. Finally, modeling of the threshold voltage has been developed by using the shortest

tunneling path. Some important results and discussions related to the effects of oxide interface charges on the surface potential, electric field, drain current and threshold voltage of DM-HGD DG TFETs have been presented in Sec. 4.3. Finally, Sec. 4.4 includes the summary and conclusion of the present chapter.

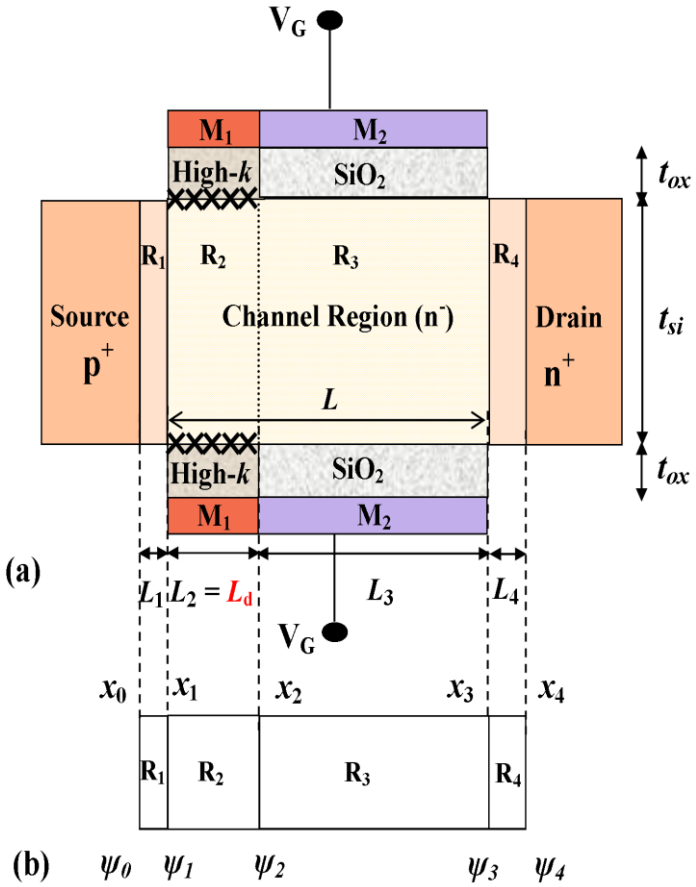

Fig. 4.1: (a) Schematic of DM-HGD DG TFET with localized interface charges; (b) Surface junction potential of DM-HGD DG TFET

4.2 Model Formulation

The schematic cross-sectional view of DM-HGD DG TFET with localized interface charges is shown in Fig. 4.1(a). Here L_1, L_2, L_3, L_4, L_d, L, t_{ox} and t_{si} are source/channel depletion length, tunneling gate length, auxiliary gate length,

drain/channel depletion length, localized charge length, channel length, gate-oxide thickness, and channel thickness of the device, respectively. Figure 4.1(b) shows the surface junction potentials ψ_0, ψ_1, ψ_2, ψ_3 and ψ_4 at the corresponding position x_0, x_1, x_2, x_3 and x_4, respectively.

4.1.1 Modeling of Surface Potential

The surface potential becomes either sensitive or insensitive to mobile charges in the channel depending upon the applied gate and drain bias of TFET devices [Wu *et al.* (2014), Jain *et al.* (2017)]. The regime of operation of the TFET in which the surface potential becomes linearly dependent on the applied gate bias at a fixed drain voltage is called the depletion regime [Wu *et al.* (2014)]. On the other hand, the surface potential becomes insensitive to applied gate bias for a fixed drain voltage is called mobile regime [Pal and Dutta (2016)]. We have first developed the surface potential model for the depletion regime of operation, which is then modified by incorporating the mobile charge carriers to make it applicable for both the depletion and mobile regimes of operation of the TFETs.

4.2.1.1 2-D Electrostatic Surface Potential: Depletion Regime

In this case, the applied gate bias is assumed to be sufficiently low while the drain bias is considered to be high enough so that surface potential becomes linearly dependent on the applied gate voltage [Wu *et al.* (2014)]. Now, following the similar methods as considered in Chapter 3, the expression of 2-D electrostatic surface potential $\psi_{dep,s,i}(x)$ in different regions R_i $(i = 1, 2, 3, 4)$ can be given by

$$\psi_{dep,s,i}(x) = \psi_{0i}(x) + \left[V_{G,i}^{eff} - \psi_{0i}(x)\right](t_{Si}/2\lambda_i)^2 \tag{4.1}$$

where, $V_{G,i}^{eff} = V_{GS} - \varphi_{FB,i}$ is the effective gate voltage where V_{GS} is the gate-to-source voltage and $\varphi_{FB,i} = (\varphi_{FB0,i} - qN_{f,i}/C_i)$ is the effective flat band voltage where $\varphi_{FB0,i} = (\varphi_{M_i} - \chi_{Sub} - E_g/2)/q$ is the flat band voltage with $\varphi_{M_1} = \varphi_t$ and $\varphi_{M_2} = \varphi_a$ as the tunneling and auxiliary gate work functions, respectively; $N_{f,i}$ is the localized interface charge density with $N_{f,(1,3,4)} = 0$ and $N_{f,2} = \pm 1 \times 10^{12}\,\text{cm}^{-2}$ [Vishnoi and Kumar (2014)]; χ_{Sub} and E_g are the electron affinity and energy band-gap of the substrate material, respectively; q is the electrostatic charge; $\lambda_i = \sqrt{(C_{ch}/C_i + 1/4)t_{si}^2}$ is characteristic length with $C_{ch} = \varepsilon_{si}/t_{si}$ and C_i $(i = 1, 2, 3, 4)$ as the channel region capacitance, and gate-oxide capacitance in the region R_i $(i = 1, 2, 3, 4)$, respectively. We have considered $C_1 \cong (2/\pi)\varepsilon_{ox}/t_{eq}$ and $C_4 \cong (2/\pi)\varepsilon_{ox}/t_{ox}$ as the respective fringing field capacitances in R_1 and R_4 regions obtained by the conformal mapping techniques [Lin and Kuo (2003)]. $C_2 = \varepsilon_{ox}/t_{eq}$ and $C_3 = \varepsilon_{ox}/t_{ox}$ are the respective capacitances of high-*k* and SiO_2 with $t_{eq} = \varepsilon_{ox}t_k/\varepsilon_k$ as equivalent oxide thickness (EOT) where ε_{ox} and ε_k are the respective permittivities of SiO_2 and high-*k* gate dielectric, and $\psi_{0i}(x)$ is the center potential in the regions R_i $(i = 1, 2, 3, 4)$ which can be expressed as:

$$\psi_{0i}(x) = A_i \exp(\beta_i(x - x_{i-1})) + B_i \exp(-\beta_i(x - x_{i-1})) + P_i \tag{4.2}$$

$$P_i = V_{G,i}^{eff} + (qN_i\lambda_i^2/2\varepsilon_{si}), \qquad \beta_i^2 = 2/\lambda_i^2 \tag{4.3}$$

where, P_i is the mid-surface potential of the device and, A_i and B_i are arbitrary constants to be determined from boundary condition as the same manner in Chapter 2.

4.2.1.2 2-D Electrostatic Surface Potential: Impacts of Mobile Charges

In this sub-section, the impact of mobile charge carriers on the surface potential profile has been studied under a high gate and low drain bias conditions. The mobile charge carriers in the channel created under above-biased conditions saturate the mid-surface potential, P_i [Wu *et al.* (2014)] and narrow the characteristics length, λ_i [Shen *et al.* (2008)] of the device. To include the effect of the mobile charge carriers, we can write the mid surface potential, $P_{mob,i}$ by an empirical equation as [Wu *et al.* (2014)]:

$$P_{mob,i} = 0.5\left(P_i + \psi_m - \sqrt{(\psi_m - P_i)^2 + \delta^2} \right) \tag{4.4}$$

where, δ is the smoothing factor (whose value is 0.04 for whole operation region) and ψ_m is the mobile charge surface potential [Jain *et al*. (2017)]

$$\psi_m = \left[V_{DS} + \psi + u(P_i - V_{DS} - \psi) + v(P_i - V_{DS} - \psi)^2 \right] \tag{4.5}$$

where, u and v are two fitting parameters; ψ is the surface potential needed to create sufficient mobile charge carriers to protect the gate modulation which can be given by [Wu *et al.* (2014)]:

$$\psi = V_T \ln(N_{ch} N_m / n_i^2) \tag{4.6}$$

where, V_T is the thermal voltage; N_{ch} is the channel doping concentration; N_m is the mobile charge density corresponding to the transition from linear to saturation variation and its extracted value is $1\times10^{18}\ \mathrm{cm}^{-3}$ [Wu *et al.* (2014)].

Similarly, $\lambda_{mob,i}$ can be expressed by considering the mobile charge carriers in the channel regions by variational approach [Shen *et al.* (2008)] as:

$$\left(\frac{1}{\lambda_{mob,i}}\right)^2 = \left(\frac{1}{\lambda_i}\right)^2 - \left(\frac{8qN_{inv,i}}{t_{si}\varepsilon_{si}(\psi_0 - P_{mob.i})}\right) \tag{4.7}$$

where, ψ_0 is the built-in-potential between the source and the channel region and $N_{inv,i} = 2C_i(V_{G,i}^{eff} - P_{mob,i})$ is the inversion charge density [Pan and Chui (2012)].

Thus, the expression of 2-D electrostatic surface potential $\psi_{s,i}(x)$ after considering the mobile charge carriers can be expressed as:

$$\psi_{s,i}(x) = \psi_{mob,0i}(x) + \left[V_{G,i}^{eff} - \psi_{mob,0i}(x)\right]\left(t_{Si}/2\lambda_{mob,i}\right)^2 \tag{4.8}$$

$$\psi_{mob,0i}(x) = \left[A_i \exp(\beta_{mob,i}(x - x_{i-1})) + B_i \exp(-\beta_{mob,i}(x - x_{i-1})) + P_{mob.i}\right] \tag{4.9}$$

$$\beta_{mob,i}^2 = 2/\lambda_{mob,i}^2 \tag{4.10}$$

Now, the surface potential $\psi_{s,i}(x)$ is applicable for both the depletion and mobile regimes of operation of the device.

4.2.2 Modeling of Drain Current

The drain current (I_d) of TFET devices can be defined as the integral of BTBT generation rate (G_{BTBT}) over the entire tunneling volume and can be expressed by Kane's model [Kane (1960)]:

$$I_d = q\int_{Voiume} G_{BTBT}\,dV = qt_{si}\int A_{Kane}E^{\alpha}\exp\left(-\frac{B_{Kane}}{E}\right)dxdw \tag{4.11}$$

where, A_{Kane} and B_{Kane} are the Kane's tunneling process-dependent parameters [ATLAS (2013)]; α is a material-dependent parameter and its value is 2 for direct band-gap material (e.g., InAs) and 2.5 for indirect band-gap material (*e.g.*, Si); E is the local electric field.

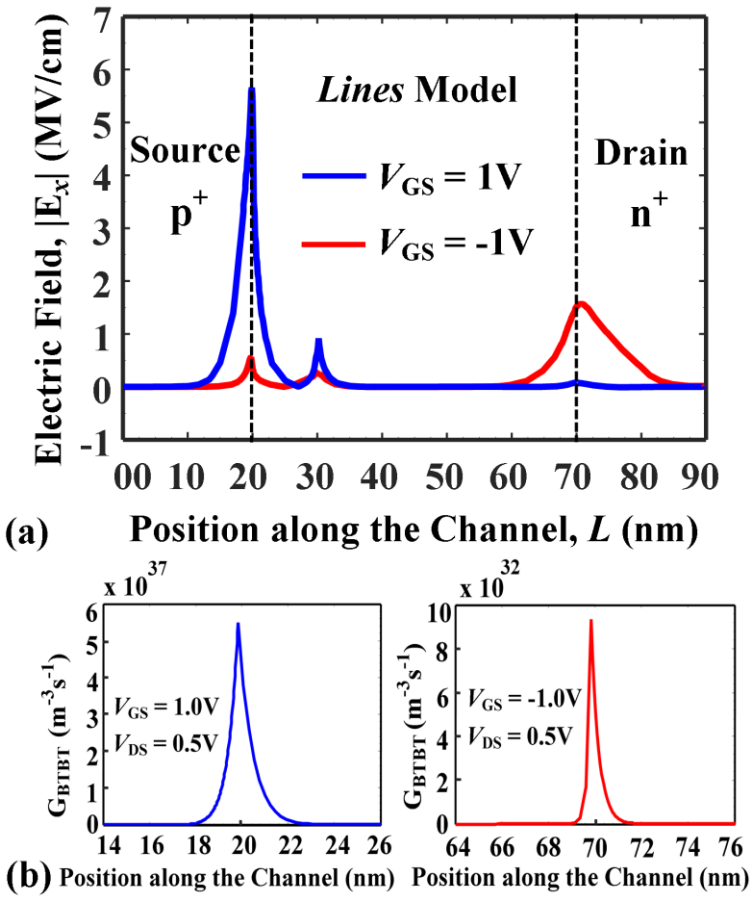

Fig. 4.2: Comparisons of (a) $|E_x|$, and (b) G_{BTBT} along the channel for different V_{GS} of DM-HDG DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm , V_{DS} = 0.5V

It has been mention that lateral electric field (E_x) considered mainly for obtaining the BTBT generation rate of TFETs device [Vishnoi and Kumar (2014), Upasana *et al.* (2015)]; So, E can be replaced by E_x for obtaining the BTBT generation rate. E_x can be derived by differentiating the $\psi_{s,i}(x)$ with respect to x, $(E_x = -\partial\psi_{s,i}(x)/\partial x)$. The variation of $|E_x|$ and its corresponding G_{BTBT} along the channel for different gate bias condition (*i.e.*, forward bias, $V_{GS} = 1\text{V}$ and ambipolar bias, $V_{GS} = -1\text{V}$) are shown in Fig. 4.2(a) and Fig. 4.2 (b) at constant $V_{DS} = 0.5\text{V}$ of DM-HGD DG TFET device. From the Fig. 4.2(a), it is cleared that the value of $|E_x|$ at source/channel junction in forward bias, $V_{GS} = 1\text{V}$ is much greater than ambipolar bias, $V_{GS} = -1\text{V}$; so, we have neglected the

effect of ambipolar bias for G_{BTBT} calculation in forward bias. Similarly, the value of $|E_x|$ at drain/channel junction for forward bias is much smaller than ambipolar bias; so we have neglected the effect of forward bias for G_{BTBT} calculation in ambipolar bias. So, we have calculated G_{BTBT} for different bias separately as shown in Fig. 4.2(b).

Fig. 4.3 and Fig. 4.4 show the energy band diagram along the channel for two different bias conditions (*i.e.*, forward and ambipolar bias) of DM-HGD DG TFET device. From the figure 4.3, it is observed that charge carriers tunnel from valance band of source to conduction band of channel region in forward bias $(V_{GS} = 1\mathrm{V}, V_{DS} = 0.5\mathrm{V})$. Similarly, charge carriers tunnel from valance band of channel to conduction band of drain in ambipolar bias $(V_{GS} = -1\mathrm{V}, V_{DS} = 0.5\mathrm{V})$ of DM-HGD DG TFET (see Fig. 4.4). Hence, we have calculated G_{BTBT} for obtaining the drain current in all bias (*i.e.*, ambipolar to forward bias) separately which is described in the subsection 4.2.2.1 and 4.2.2.2, respectively.

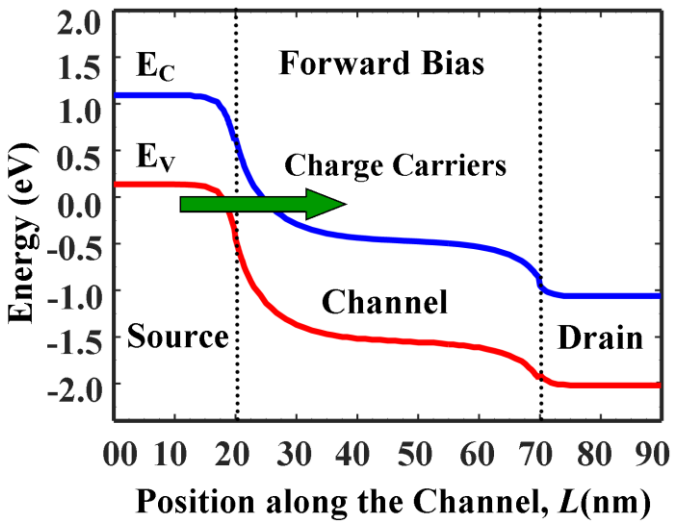

Fig. 4.3: Energy band diagram for forward gate bias (V_{GS} = 0.5V, V_{DS} = 0.5V) of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm

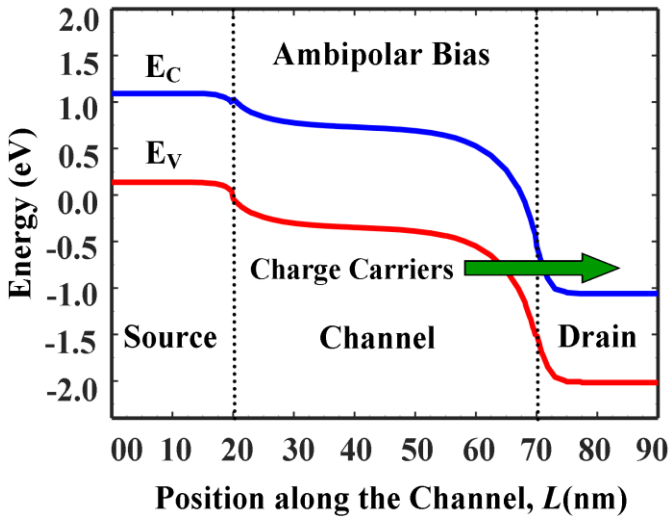

Fig. 4.4: Energy band diagram for ambipolar gate bias (V_{GS} = -0.5V , V_{DS} = 0.5V) of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm

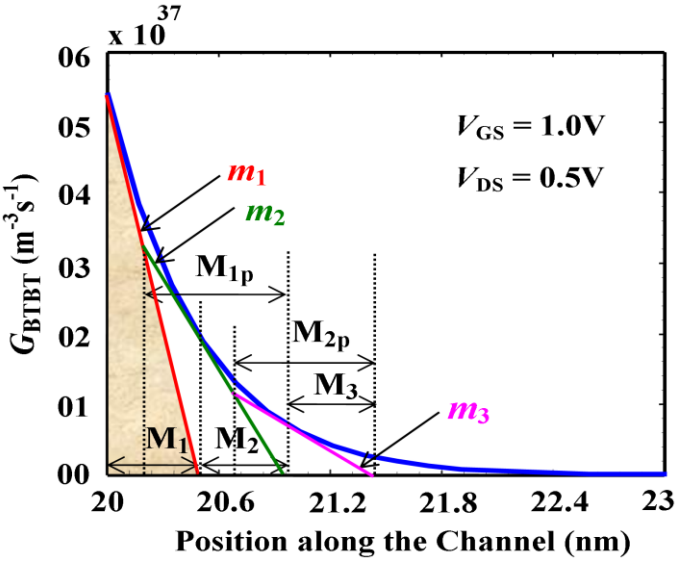

Fig. 4.5: G_{BTBT} along the channel for forward gate bias *i.e.*, V_{GS} = 1V, of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm , V_{DS} = 0.5V

4.2.2.1 BTBT Generation Rate in Forward Gate Bias

Under forward bias condition, we have calculated the area of G_{BTBT} curve at source/channel junction as shown in Fig. 4.5. The tangent line approximation (TLA) method [Vishnoi and Kumar (2015), Guan *et al.* (2017)] has been used for obtaining the area of G_{BTBT} curve to avoid numerical integration method.

Following the method of [Vishnoi and Kumar (2015), the area of G_{BTBT} curve can be expressed as:

$$G_{\mathrm{BTBT}}(For) = \left[(G_1 + G_2 + \ldots\ldots\ldots\ldots + G_n) - (G_{1p} + G_{2p} + \ldots\ldots + G_{(n-1)\mathrm{p}})\right] \tag{4.12}$$

where $G_1, G_2 \ldots\ldots G_n$ are the area under the tangent lines m_1, $m_2 \ldots\ldots m_n$; and $G_{1\mathrm{p}}$, $G_{2\mathrm{p}} \ldots\ldots G_{(n-1)\mathrm{p}}$ are the overlap area between the tangent lines m_1 & m_2, m_2 & m_3 and $m_{(n-1)}$ & m_n, respectively (see Fig. 4.5).

$$G_n = \frac{G'_{BTBT}}{2}\left[(L_1 + M_1 + M_2 + \ldots\ldots\ldots\ldots + M_{n-1})M^2_{(n-1)p}\right] \tag{4.13}$$

$$G_{(n-1)p} = \frac{G'_{BTBT}}{2}\left[(L_1 + M_1 + M_2 + \ldots\ldots\ldots\ldots + M_{n-2}) \times (M_{(n-1)p} - M_n)^2\right] \tag{4.14}$$

$$M_{(n-1)p} = \left[\frac{G'_{BTBT}\,(L_1 + M_1 + M_2 \ldots\ldots\ldots\ldots + M_{n-2})M_n}{M'_{BTBT} - M_{BTBT}}\right] \tag{4.15}$$

$$M_n = \left[\frac{G_{BTBT}\,(L_1 + M_1 + M_2 \ldots\ldots\ldots\ldots + M_{n-1})}{G'_{BTBT}\,(L_1 + M_1 + M_2 \ldots\ldots\ldots\ldots + M_{n-1})}\right] \tag{4.16}$$

$$M'_{BTBT} = G'_{BTBT}\,(L_1 + M_1 + M_2 \ldots\ldots\ldots\ldots + M_{n-2}) \tag{4.17}$$

$$M_{BTBT} = G'_{BTBT}\,(L_1 + M_1 + M_2 + \ldots\ldots\ldots M_{n-1}) \tag{4.18}$$

4.2.2.2 BTBT Generation Rate in Ambipolar Gate Bias

Fig. 4.6 shows the variation of G_{BTBT} along the channel of DM-HGD DG TFET in ambipolar bias condition (*i.e.*, $V_{GS} = -1\text{V}$). We have calculated the area of G_{BTBT} curve by using the TLA method in the same manner as described earlier for the forward bias condition.

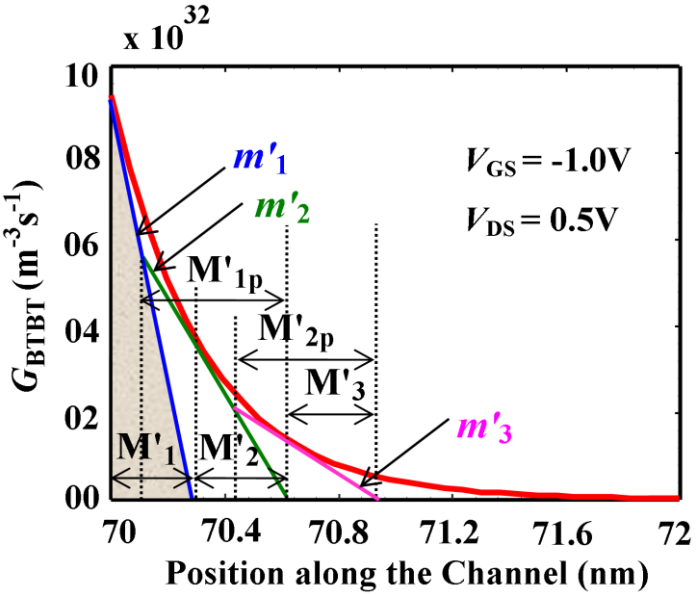

Fig. 4.6: G_{BTBT} along the channel for ambipolar gate bias *i.e.*, V_{GS} = -1V, of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm , V_{DS} = 0.5V

$$G_{\text{BTBT}}(Amb) = G_{\text{BTBT}}(For)\big|_{L_1 \Rightarrow L_1+L_2+L_3} \tag{4.19}$$

Since, both $G_{BTBT}(\text{For})$ and $G_{BTBT}(\text{Amb})$ are symmetrical about the interface junction, total G_{BTBT} can be expressed as:

$$G_{BTBT} = 2\left(G_{BTBT}(For) + G_{BTBT}(Amb)\right) \tag{4.20}$$

It is reported that about 95% accuracy can be achieved in the calculation of the area of G_{BTBT} curve by using the TLA method if the minimum number of steps is n = 4

[Vishnoi and Kumar (2015), Guan *et al.* (2017)].

Assuming a fixed channel width $(w = 1\mu m)$ in Eq. (4.11), I_d can be expressed in the $(Amp/\mu m)$ as:

$$I_d = (qt_{si}G_{\text{BTBT}} + I_{lea.})f_{\text{fermi}} \tag{4.21}$$

where, $f_{\text{fermi}} = 1 - 2/(1 + \exp(V_{DS}/\xi V_T))$ is the correction factor [Zhang and Chan (2014)] which is introduced to ensure zero I_d at $V_{DS} = 0\text{V}$ in the output characteristics of the device; ξ is an empirical parameter; $I_{lea.}$ is the leakage current which is included in calculation of I_d by an empirical equation given by [Pal and Dutta (2016)]:

$$I_{lea.} = 1\times10^{-16}\exp(-(V_{GS} - \varphi_{FB,2})/7V_T) \tag{4.22}$$

4.2.3 Modeling of Threshold Voltage

Threshold voltage $(\text{say } V_{th})$ is an important parameter of any TFET device. It can be defined as the gate voltage (V_{GS}) at which the energy tunneling barrier tends to saturate [Boucart and Ionescu (2008)]. We have used the concept of shortest tunneling path $(L_t^{\min})$ to extract the threshold voltage (V_{th}) of the device under study [Chander and Baishya (2015)]. The $L_t^{\min}$ can be defined as the lateral distance from the source/channel junction $(x = 0)$ to the point $(x = L_t^{\min})$ where the surface potential is changed by E_g/q. Thus, $L_t^{\min}$ can be expressed as [Dash and Mishra (2015)]:

$$L_t^{\min} = x(\psi_0 + E_g/q) - x(\psi_0) \tag{4.23}$$

When the surface potential at $x = L_t^{\min}$ reaches at the potential of $V_{DS} + V_T\ln(N_4/n_i)$ for $V_{DS} \le 0.5\text{V}$ [Chander and Baishya (2015)] and $\psi_{S,3}$ [Pal and Dutta (2016)] for

$V_{DS} > 0.5\text{V}$; then the exponential function of I_d becomes a linear function of the applied V_{GS}; and the corresponding $V_{GS} = V_{th}$ is obtained by solving the following equation:

$$\psi_{s,i}(x = L_t^{\min})\Big|_{V_{GS}=V_{th}} = \psi_4 = V_{DS} + V_T \ln(N_4/n_i) \tag{4.24}$$

where, V_{DS}, N_4 and ψ_4 are the drain-to-source voltage, drain doping concentration and built-in-potential between drain/channel junction, respectively.

Fig. 4.7 and Fig. 4.8 shows how to extract V_{th} from the surface potential plot through $L_t^{\min}$ concept of the TFET devices. The variation of surface potential along the channel for $V_{GS} = 1\text{V}, V_{DS} = 0.5\text{V}$ of DM-HGD DG TFET is shown in Fig. 4.7 where the surface potential variation with V_{GS} is shown in Fig. 4.8. When the surface potential at $x = L_t^{\min}$ reaches the potential ψ_4 in Fig. 4.7, the corresponding value of V_{GS} is the threshold voltage V_{th} of the device (see Fig. 4.8).

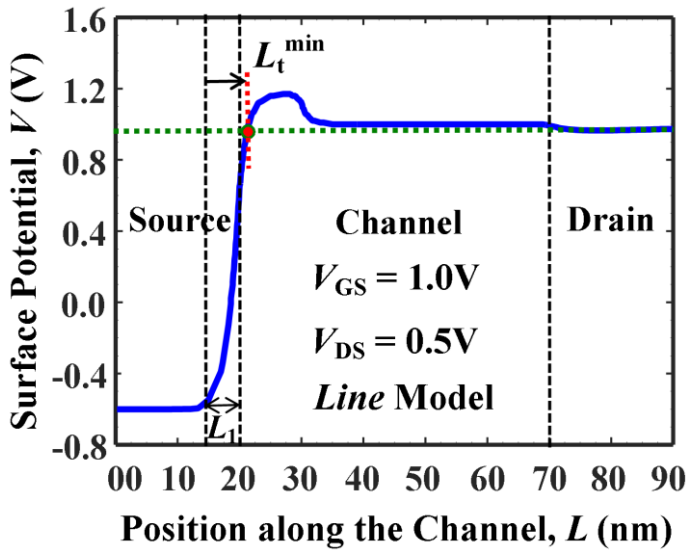

Fig. 4.7: Variation of surface potential along the channel of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm , V_{GS} = 1.0V , V_{DS} = 0.5V

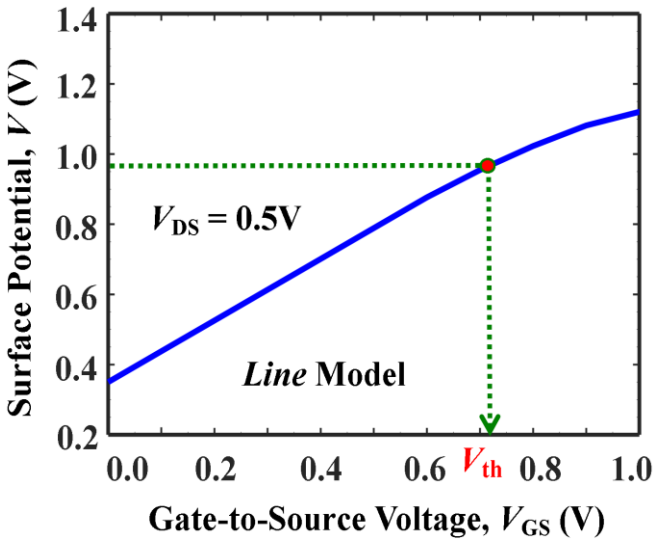

Fig. 4.8: Extraction of V_{th} from surface potential versus V_{GS} curve (Fig. 4.7) by using L_t^{min} of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm

4.3 Results and Discussion

In this section, the model results of DM-HGD DG TFETs are validated with the ATLAS^{TM} TCAD simulation data. The Non-local BTBT, Trap-assist tunneling (TAT), Shockley-Read-Hall recombination (SRH), Concentration and electric field dependent Lombardi (CVT), Auger recombination and bandgap-narrowing (BGN) models have been included in the TCAD simulation tool for characterizing the transport behavior of the DM-HGD DG TFET under consideration. The syntax "*Interface*" has been used to capture the fixed interface charges of the proposed device in TCAD simulation. The doping concentration of source, channel and drain are $N_1 = 1\times10^{20}\,\text{cm}^{-3}$, $N_2 = N_3 = 1\times10^{16}\,\text{cm}^{-3}$ and, $N_4 = 5\times10^{18}\,\text{cm}^{-3}$ with $L_2 = 10\,\text{nm}$, $L_3 = 40\,\text{nm}$, $L = 50\,\text{nm}$, $t_{ox} = 2\,\text{nm}$, $t_{si} = 12\,\text{nm}$, respectively. The tunneling and auxiliary gate work function are taken as $\varphi_1 = 4.2\,\text{eV}\,(\text{Mo, IrO}_2)$ and $\varphi_2 = 4.6\,\text{eV}\,(\text{Ta,W})$ for the maximum ON-to-OFF current ratio of the device as discussed in Chapter 3. First of all, the dual-modulation

nature of surface potential of the device is studied in Fig. 4.9 to Fig. 4.12; which is the intrinsic property of any TFET devices. In this property, when the surface potential is controlled by the gate bias for a fixed V_{DS}, the TFET is said to work under the gate-control regime while it is said to work under drain-control regime if the surface potential is controlled by the drain voltage for a fixed V_{GS} [Wu *et al.* (2014)].

Fig. 4.9 shows the variation of surface potential along the channel for different V_{GS}. It is observed from the figure that the surface potential is increased with the increase of V_{GS}. Further, when V_{GS} is increased more than a certain value, $(i.e., V_{GS} > 0.8\text{V})$, the surface potential becomes insensitive to V_{GS}.

The variation of surface potential with V_{GS} for different V_{DS} is shown in Fig. 4.10. It is observed that the surface potential varies linearly with low V_{GS} (*i.e.*, gate-control regime). However, beyond a certain value of V_{GS}, the surface potential is screened from further bending (*i.e.*, drain-control regime) due to the creation of a significant amount of mobile charge carriers in the channel [Wu *et al.* (2014)]. A good matching between the TCAD and model results confirms the validity of the surface potential model of the DM-HGD DG TFETs understudy when the model includes the effect of mobile charge carriers in the channel. However, a considerable amount of mismatching between model and TCAD simulation results is observed when we model the surface potential without considering the mobile charge carriers (WTCMC). Clearly, the inclusion of mobile charge carriers in our model for proposed the DM-HGD DG TFET is well justified.

In Fig. 4.11, the variation of surface potential along the channel is shown for different V_{DS} but for a fixed $V_{GS} = 1\text{V}$. The surface potential is observed to be increased with the increase of V_{DS}. However, when V_{DS} is increased beyond a certain value

($i.e., V_{DS} > 0.6\text{V}$), the surface potential is saturated (*i.e.*, becomes insensitive to V_{DS} as observed in Fig. 4.10). This property is known as dual-modulation property of the surface potential of TFET devices [Wu *et al.* (2014)].

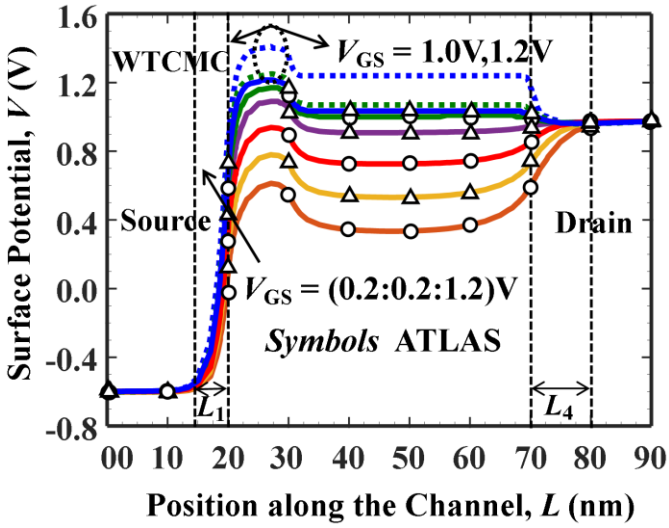

Fig. 4.9: Variation of surface potential along the channel for different V_{GS} of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm , V_{DS} = 0.5V

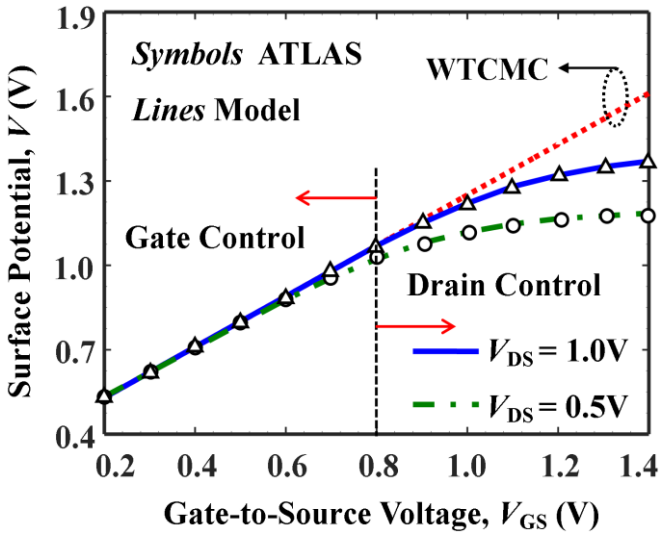

Fig. 4.10: Variation of surface potential against V_{GS} for different V_{DS} of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm

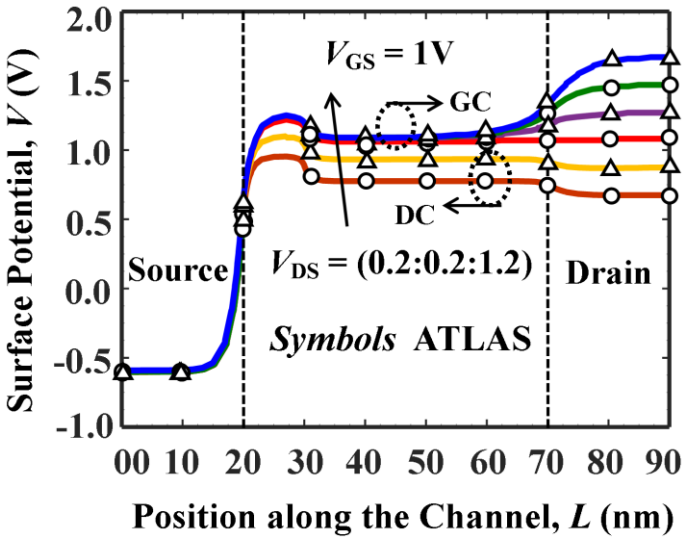

Fig. 4.11: Variation of surface potential along the channel for different V_{DS} of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm , V_{GS} = 1V

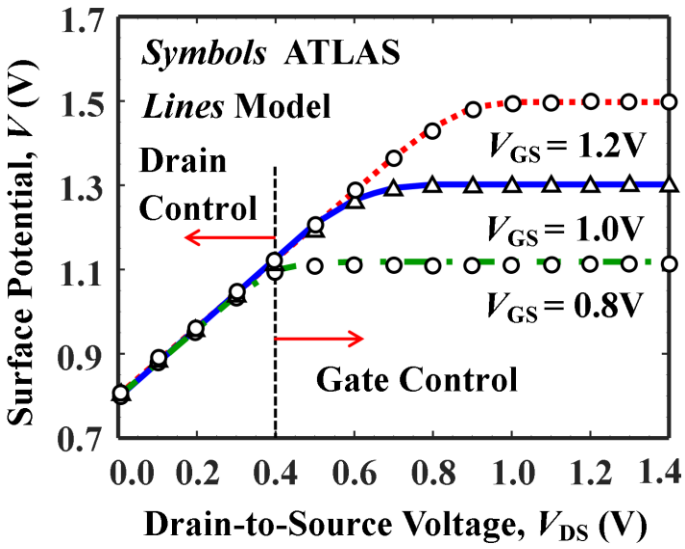

Fig. 4.12: Variation of surface potential against V_{DS} for different V_{GS} of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm

The variation of surface potential against V_{DS} for different V_{GS} as shown in Fig. 4.12 confirms that the surface potential not only depends on V_{GS} but also on V_{DS}. It linearly varies with low V_{DS} (*i.e.*, drain control regime) but is pinned and becomes independent of V_{DS} (*i.e.*, gate control regime) at higher V_{DS} values. It is observed from Fig. 4.9 to Fig. 4.12 that the proposed device operates in depletion (*i.e.*, gate control) regime for $V_{GS} \leq 0.8\text{V}$ and $V_{DS} \geq 0.6\text{V}$. Otherwise, it operates in the mobile (*i.e.*, drain control) regime. It is also observed that both gate and drain-control regimes of the device are increased (decreased) with the increase (decrease) in V_{DS} and V_{GS}.

The variations of surface potential and its corresponding electric field along the channel for different N_f have been plotted in Fig. 4.13 and Fig. 4.14, respectively. It is observed that both the surface potential and its corresponding electric field are increased (decreased) with the increase (decrease) in the positive (negative) values of N_f due to decrease (increase) in the effective flat band voltage.

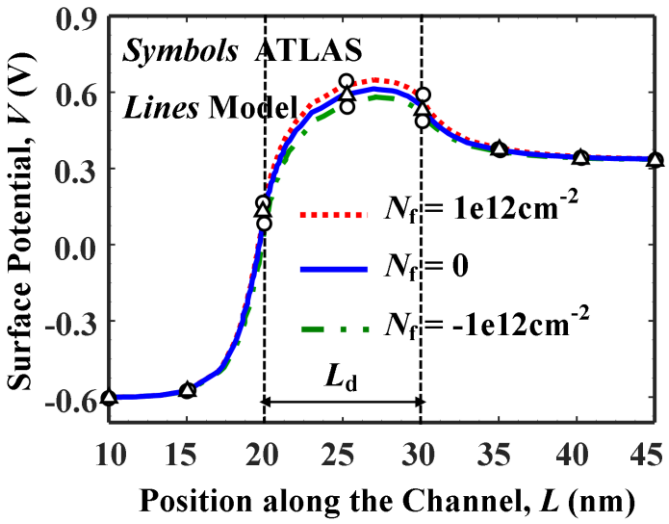

Fig. 4.13: Variation of surface potential along the channel for different N_f of DM-HGD DG TFET at V_{GS} = 0.2V, V_{DS} = 0.5V, $L_2 = L_d$ = 10nm, L_3 = 40nm, L = 50nm

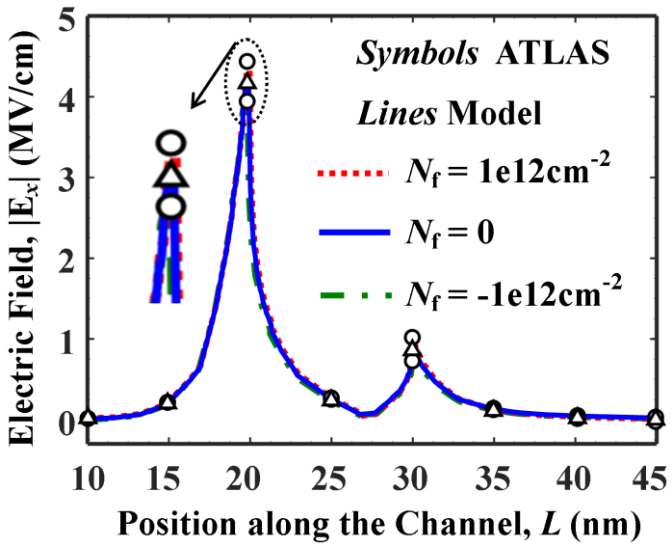

Fig. 4.14: Variation of amplitude of lateral electric field along the channel for different N_f of DM-HGD DG TFET at V_{GS} = 0.2V , V_{DS} = 0.5V, L_2 = 10nm, L_3 = 40nm, L_d = 10nm, L = 50nm, t_{si} = 12nm

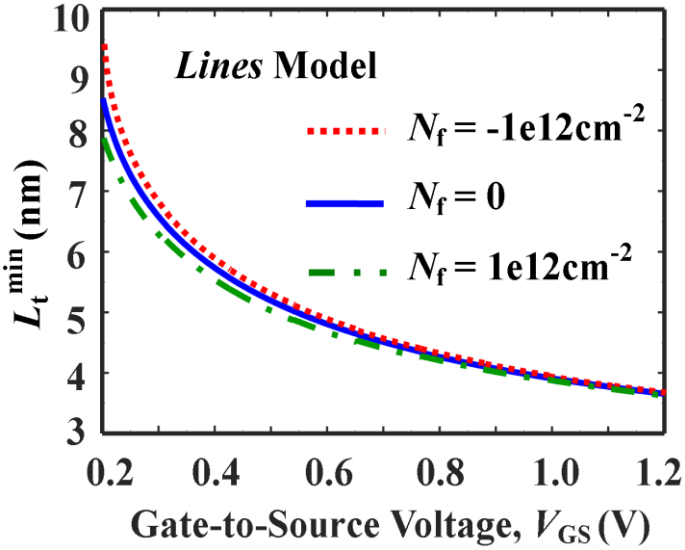

Fig. 4.15: Variation of L_t^{min} with V_{GS} for different N_f of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L_d = 10nm, L = 50nm, t_{Si} = 12nm, V_{DS} = 0.5V

Now, Fig. 4.15 shows the variation of $L_t^{\min}$ against V_{GS} for different N_f of DM-HGD DG TFET. It is observed from the figure that $L_t^{\min}$ changes with N_f at low V_{GS} (*i.e.*, $V_{GS} < 0.4\text{V}$) but becomes independent of N_f with the increase of V_{GS} due to the negligible localized interface potential, qN_f/C_k in the effective gate voltage of the devices (see Eq. (4.1)).

Fig. 4.16 shows the comparison of I_d versus V_{GS} plots for different DG TFET device structures for a fixed $V_{DS} = 0.5\text{V}$ where $\text{D(I)}, \text{D(II)}$ and D(III) represents the DM DG-TFET with HfO_2 as the only gate oxide (*i.e.*, with no SiO_2 region), single metal (with $\varphi_{\text{M}} = 4.2\text{eV}$) gate based HGD DG TFET, and DM-HGD DG TFET structures, respectively. The ambipolar drain current (due to negative V_{GS}) is observed to be the smallest in our proposed DM-HGD DG TFET structure. We have compared various electrical parameters such as I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, I_{AMB} and SS for the above mentioned three different DG TFETs devices in Table-4.1. It is observed that the ON current of DM DG TFET device with only HfO_2 as gate oxide (*i.e.*, D-I) is the highest while the other performance parameters (*i.e.*, ambipolar current I_{AMB}, I_{ON}/I_{OFF} and SS) of the proposed DM-HGD DG TFET device are the best among the three structures considered in Fig. 4.16. Note that I_{ON}, I_{OFF} and I_{AMB} have been extracted from the $I_d - V_{GS}$ curves for $V_{GS} = 1\,\text{V}$, $V_{GS} = 0\,\text{V}$ and $V_{GS} = -0.8\,\text{V}$ but with a fixed $V_{DS} = 0.5\,\text{V}$. The point SS is obtained from the TCAD simulation following the method of [Boucart and Ionescu (2007)].

The variation of I_d with V_{GS} for different tunneling gate lengths of the DM-HGD DG TFET is shown in Fig. 4.17 for a fixed channel length $L = 50\text{nm}$. It is observed that $L_2 = 10\text{nm}$ is possibly the best value for getting the maximum ON-to-OFF drain current

ratio. That is why we have used $L_2 = 10\text{nm}$ for calculating the model results of DM-HGD DG TFET in the present manuscript.

TABLE 4.1

COMPARISONS OF DEVICE PARAMETERS FOR DIFFERENT DG-TFET BASED DEVICE STRUCTURES

DG-TFET Device	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}	I_{AMB} (A/μm)	*SS* (mV/dec)
D (I)	3.9E-5	6.5E-16	5.1E09	2.1E-09	21
D (II)	1.6E-5	8.8E-14	1.8E08	8.5E-11	31
D (III)	3.6E-5	2.5E-16	1.1E10	2.0E-13	20

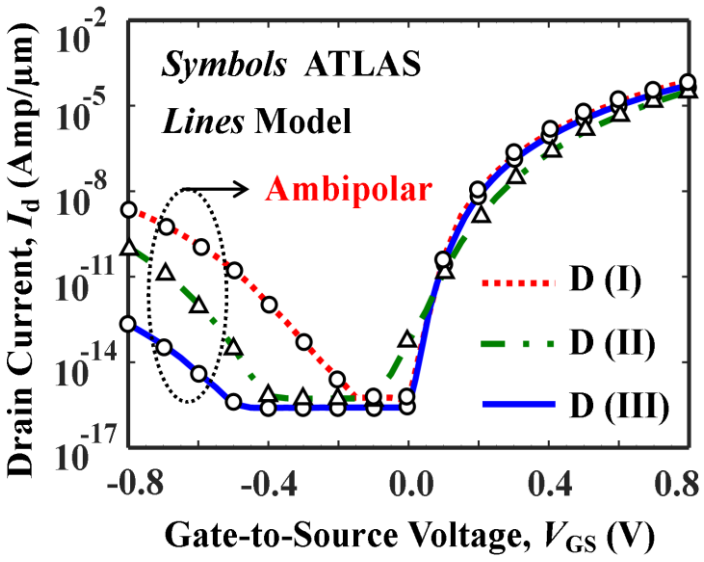

Fig. 4.16: Comparisons of I_d against V_{GS} for different combinations of DM-HGD DG TFET structures at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm , V_{DS} = 0.5V

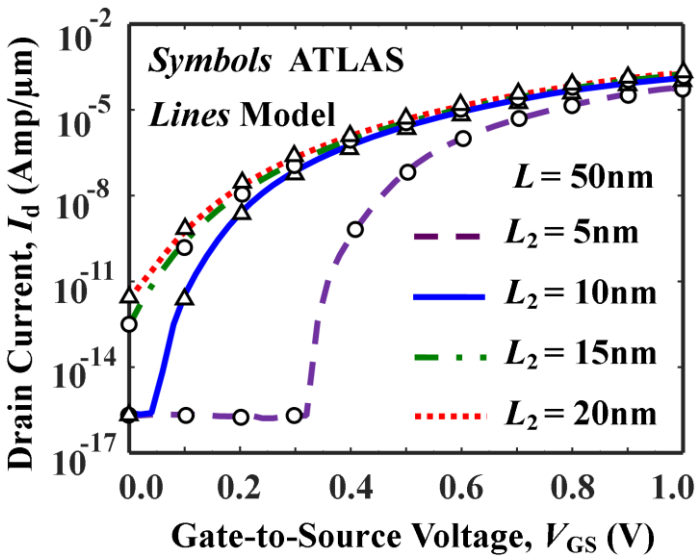

Fig. 4.17: Comparisons of I_d against V_{GS} for different L_2 of DM-HGD DG TFET structures at L = 50nm, t_{si} = 12nm , V_{DS} = 0.5V

In Fig. 4.18, we plotted I_d -V_{GS} characteristics of the DM-HGD DG TFET for different values of N_f. The drain current (I_d) is observed to be more sensitive to N_f for low V_{GS} (*i.e.*, $V_{GS} < 0.4\text{V}$) due to localize interface charge, which is more effective at low V_{GS} (as seen in Fig. 4.15).

The output characteristics of DM-HGD DG TFET structures for different N_f is shown in Fig. 4.19. From the figure, it is observed that initially I_d increases with the increase of V_{DS}; on further increasing of V_{DS}, I_d become independent of V_{DS}. It is basically due to channel resistance decreases with the increase of V_{DS} (*i.e.*, $V_{DS} < 0.3\text{V}$); but at higher V_{DS}, channel resistance becomes very low and all V_{DS} drops along the channel; so, I_d is saturated with high V_{DS} of the device. From the figure, it is also observed that I_d increases with positive N_f and vice versa; due to lowering the shortest tunneling path with positive N_f and vice versa (See Fig. 4.15), resulting maximum number of charge

carriers can tunnel from valance band to conduction band of the device; resulting I_d increases with positive N_f and vice versa.

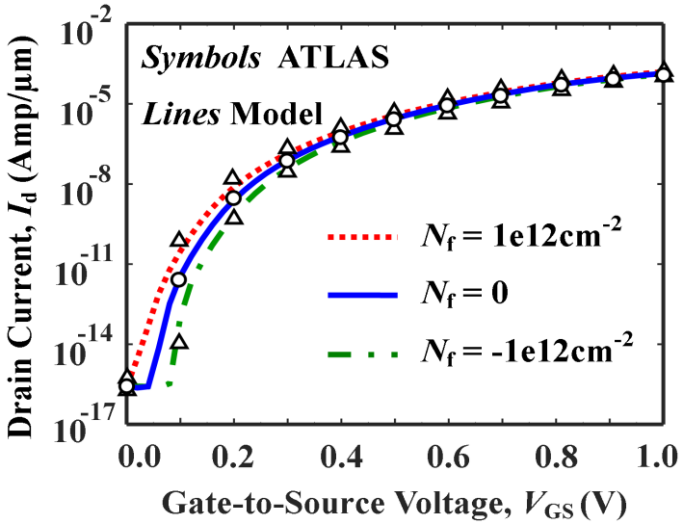

Fig. 4.18: Variation of I_d against V_{GS} for different N_f of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L_d = 10nm, L = 50nm, t_{si} = 12nm , V_{DS} = 0.5V

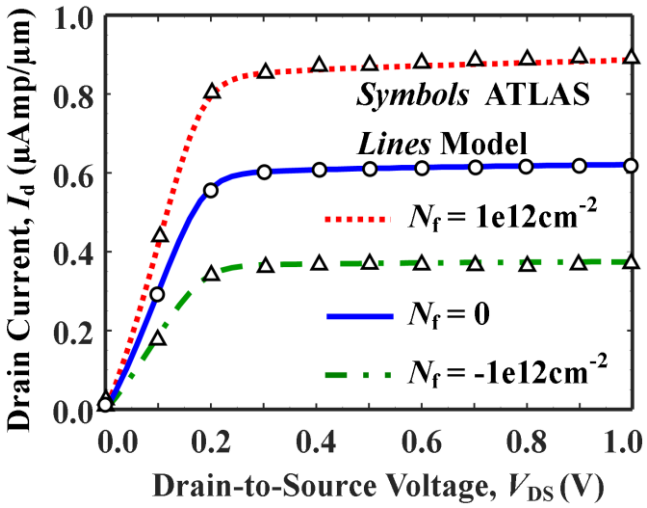

Fig. 4.19: Variation of I_d against V_{DS} for different N_f of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L_d = 10nm, L = 50nm, t_{si} = 12nm , V_{GS} = 0.4V

Fig. 4.20 plots V_{th} of the DM-HGD DG TFET under study by using TC method. In this (*i.e.*, TC) method, V_{th} is defined as the gate voltage, V_{GS} for which $\partial g_m / \partial V_{GS}$ is the maximum where, g_m is the transconductance of the device. The variation of V_{th} with V_{DS} for different N_f is shown in Fig. 4.21. It is seen that V_{th} varies linearly with low V_{DS} (*i.e.*, $V_{DS} < 0.6\text{V}$) but becomes independent of V_{DS} due to saturation of I_d for high V_{DS} values of DM-HGD DG TFET. Fig. 4.22 shows the variation of V_{th} with N_f for different combinations of dielectrics in the localized charge region of the DM-HGD DG TFET. The threshold voltage, V_{th} is decreased for higher dielectric constant based oxides due to the increased electric field at the source/channel junction. So, less V_{GS} is required for obtaining ON-state current; resulting V_{th} decreases with high-*k* dielectric constant of the device. The change in threshold voltage (ΔV_{th}) with t_{si} for different values of N_f is shown in Fig. 4.23 to note that ΔV_{th} is independent of t_{si} but it is affected by N_f mainly for low V_{DS} values (see Fig. 4.21).

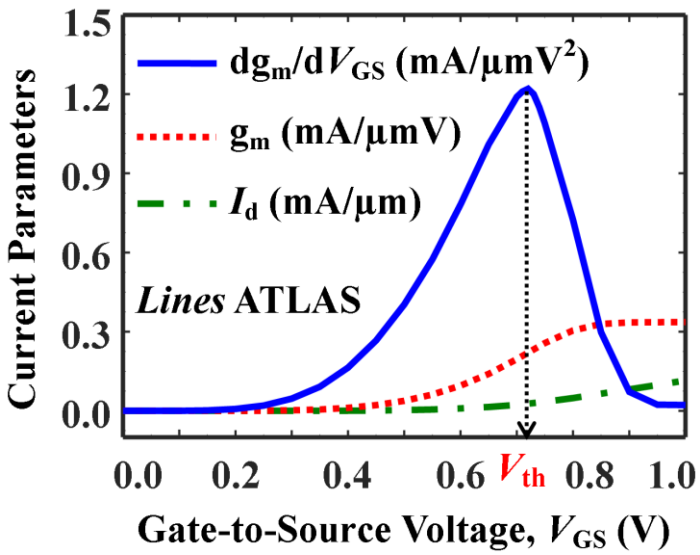

Fig. 4.20: Extraction of V_{th} from simulated current parameters by using TC method of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, t_{si} = 12nm , V_{DS} = 0.5V

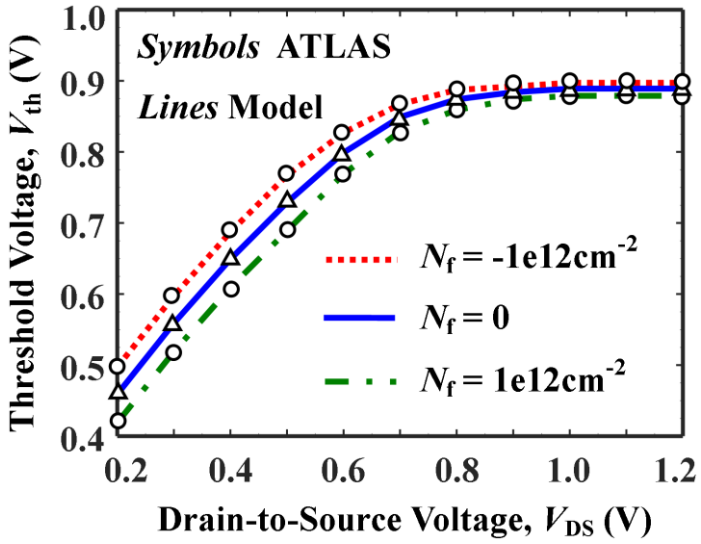

Fig. 4.21: Variation of V_{th} against V_{DS} for different N_f of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L_d = 10nm, L = 50nm, t_{si} = 12nm

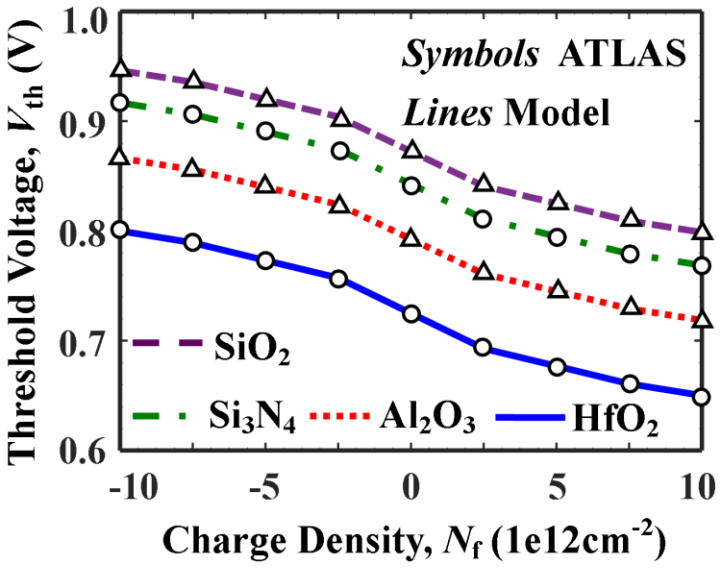

Fig. 4.22: Variation of V_{th} against N_f for different combinations of gate dielectric constant (localized region) of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L = 50nm, L_d = 10nm, t_{si} = 12nm , V_{DS} = 0.5V

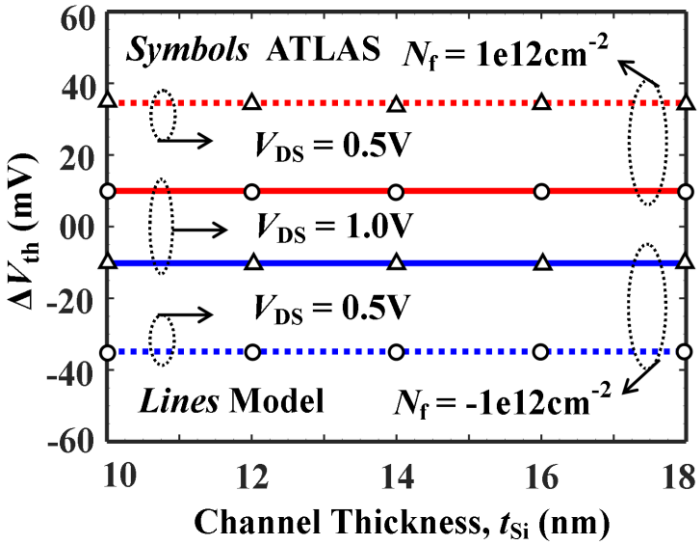

Fig. 4.23: Comparisons of ΔV_{th} against t_{si} for different N_f of DM-HGD DG TFET at L_2 = 10nm, L_3 = 40nm, L_d = 10nm, L = 50nm, t_{si} = 12nm , V_{DS} = 0.5V

4.4 Conclusion

The 2-D analytical modeling of the surface potential, drain current and threshold voltage characteristics of DM-HGD DG TFET by taking the localized interface charges near the source/channel junction, mobile charges in the channel region and charges in depletion regions at both source/channel and drain/channel junctions has been proposed in this chapter. The TLA method has been used for obtaining the drain current model for both the forward gate bias and reverse gate bias (*i.e.*, the ambipolar regime of operation) of the device. The shortest tunneling path concept has been explored for obtaining the threshold voltage model of the DM-HGD DG TFETs. The impacts of localized trap charges (due to high electric field near the source/channel junction) on the drain current and threshold voltage have been studied. The drain current is observed to be more sensitive to the localized charges at low gate bias while the threshold voltage is more sensitive to the localized charges at low drain bias. The validity of the model is

established by showing a very good matching between the model results and commercially available ATLAS^{TM} TCAD based simulation data of the proposed device.