Chapter 3

Analytical Modeling of the Electrical Characteristics of Dual-Material Double-Gate TFETs with a SiO_2/HfO_2 Stacked Gate-Oxide Structure

3.1 Introduction

We have already discussed in Chapter-1 that the dual materials gate (DMG) based DG TFETs have superior performance characteristics in the form of higher drive current, steeper SS and smaller ambipolar conduction over the single materials gate (SMG) based DG TFETs [Saurabh and Kumar (2011), Prateek Jain *et al.* (2015), Prabhat and Dutta (2016), Gracia *et al.* (2017)]. The DMG structures are obatined by using two metal-like materials in cascaded and non-overlapped manner to form the gate electrode with lower work function based material at the source side (called the tunneling gate) and the higher work function based material at the drain side (called the auxiliary gate) as introduced in Chapter-1 [Saurabh and Kumar (2011), Vishnoi and Kumar (2014)]. We have also observed in Chapter 2 that the electrical characteristics of the TFETs can be improved significantly by replacing the conventional SiO_2 by a stacked SiO_2/high-*k* gate-oxide [Boucart and Ionescu (2007), Kumar and Jit (2015a)] in the DG TFETs. From the above discussions, it is expected that the ON current, subthreshold swing (SS) and ambipolar characteristics of the TFETs can be significantly improved by combining the DMG and SiO_2/high-*k* stacked gate-oxide structures in the DG TFETs. In view of the above, the present chapter is devoted to develop the two-dimensional (2-D)

analytical models for the electrical characteristics such as surface potential, electric-field, drain current and threshold voltage of a newly proposed structure, named as stacked gate SiO_2/high-*k* dual-material (DM) double-gate (DG) TFETs, obtained by incorporating both the gate-electrode engineering and gate-oxide engineering concepts in the DG TFETs structures. The validation of model results has been achieved by comparing them with the simulation data obtained from SILVACO ATLAS^{TM} 2-D device simulator software. The layout of the present chapter is given as follows:

Section 3.2 deals with a physics-based 2-D analytical model for surface potential, electric field, drain current, and the threshold voltage of the proposed device. The parabolic-approximation technique with suitable boundary conditions has been used to solve the Poisson's equation for obtaining the surface potential function. This surface potential model has been used to model the electric field, drain current and the threshold voltage of the proposed DM DG TFET as the same manner as discussed in Chapter 2. The Section 3.3 presents some of our model results and discussions regarding the effects of different device parameters such as the channel length, tunneling-to-auxiliary gate length ratio, channel thickness and doping concentration on the electrical characteristics of of the proposed DM DG TFETs. Finally, Sec. 3.4 includes the summary and conclusion of the present chapter.

3.2 Model Formulation

Fig 3.1 shows the cross-sectional view of a DM DG TFET with a SiO_2/HfO_2 stacked gate oxide structure considered for the modeling and simulation in this chapter. Here, L, L_1, L_2, L_3, L_4, t_{ox}, t_k and t_{si} are the channel length, source depletion length in region R_1, tunneling gate length, auxiliary gate length, drain depletion length in

region R_4, SiO_2 thickness, high-*k* dielectric thickness and channel film thickness of the device, respectively. The proposed device consists of two latterly connected gate electrodes M_1 and M_2 where M_1 (*i.e.*, the gate electrode near to the source side) is termed as the tunneling gate and M_2 (*i.e.*, gate electrode at the drain side) is called the auxiliary gate. The coordinate axis is chosen at the middle of the channel thickness as shown in the Fig. 3.1. The junction potentials at x_0, x_1, x_2 and x_3 are ψ_0, ψ_1, ψ_2 and ψ_3, respectively.

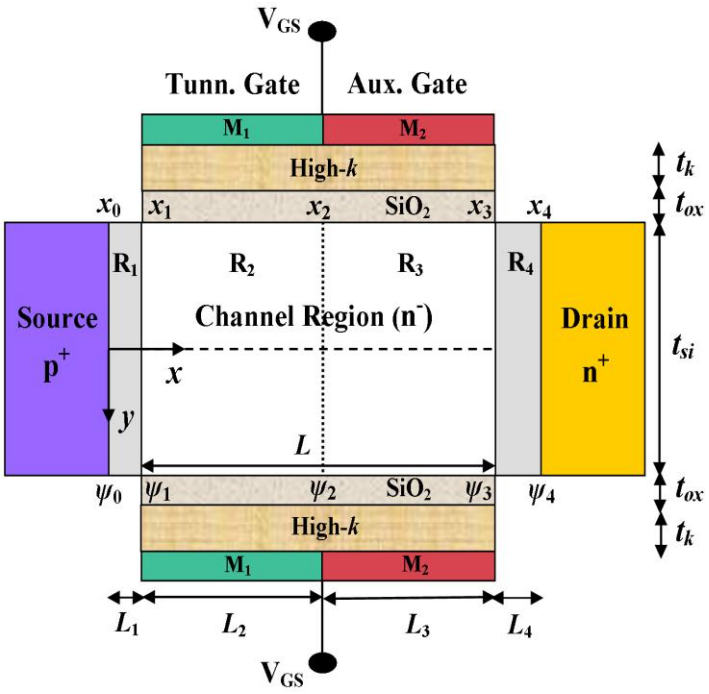

Fig. 3.1: Schematic of DM DG TFET with SiO_2/HfO_2 stacked gate-oxide

3.2.1 Modeling of Surface Potential

The 2-D Poisson equation for different regions of the channel can be written as [Bardon *et al.* (2010)]:

$$\frac{\partial^2 \psi_i(x,y)}{\partial x^2} + \frac{\partial^2 \psi_i(x,y)}{\partial y^2} = \pm \frac{qN_i}{\varepsilon_{si}} \qquad i = 1, 2, 3, 4 \tag{3.1}$$

where $\psi_i(x,y)$ is the 2-D electrostatic potential in the channel region R_i $\{i = 1, 2, 3, 4\}$ measured with respect to Fermi potential; and N_i represents the doping concentration in the R_i. In Eq.(3.1), plus sign is used for $i = 1$ and minus is used for $i = 2, 3, 4$.

Using the parabolic approximation method [Young (1989)] for solving Eq.(3.1), the 2-D electrostatic channel potential $\psi_i(x,y)$ and surface potential $\psi_{s,i}(x)$ can be solved as same manner as privious Chapter 2 and written as:

$$\psi_i(x,y) = \psi_{0i}(x) + \left[V_{G,i}^{eff} - \psi_{0i}(x)\right](y/\lambda_i)^2 \tag{3.2}$$

$$\psi_{s,i}(x) = \psi_i(x, \pm t_{Si}/2) = \psi_{0i}(x) + \left[V_{G,i}^{eff} - \psi_{0i}(x)\right](t_{Si}/2\lambda_i)^2 \tag{3.3}$$

where, $V_{G,i}^{ref} = \left(V_{GS} - \varphi_{M_i} + \chi_{Sub} + E_g/2\right)$ is the gate voltage with respect to the Fermi potential where $(\varphi_{M_1} = \varphi_t)$ and $(\varphi_{M_2} = \varphi_a)$ are the tunneling and auxiliary gate work functions; χ_{Sub} is the electron affinity of Si , and λ_i is the characteristic length of the device associated with the center channel potential $\psi_{0i}(x)$ given by

$$\lambda_i = \sqrt{\left(C_{ch}/C_i + 1/4\right) t_{si}^2} \tag{3.4}$$

where, $C_{ch} = \varepsilon_{si}/t_{si}$ and C_i $\{i = 1, 2, 3, 4\}$ are the channel region capacitance, and equivalent gate-oxide capacitance in the region R_i $\{i = 1, 2, 3, 4\}$ respectively. For R_2 and R_3 regions, $C_2 = C_3 = \varepsilon_{ox}/t_{eq}$; and for the R_1 and R_4 regions, $C_1 = C_4 \cong (2/\pi)\ \varepsilon_{ox}/t_{eq}$ where $t_{eq} = t_{ox}$, $t_{eq} = \varepsilon_{ox} t_k/\varepsilon_k$, and $t_{eq} = t_{ox} + \varepsilon_{ox} t_k/\varepsilon_k$ are the equivalent oxide thicknesses (EOT) [[Lin and Kuo (2003)] when SiO_2 (with thickness t_{ox}), HfO_2 (with

thickness t_k) and stacked SiO_2 (with thickness t_{ox})/HfO_2 (with thickness t_k) structure are used as the gate oxide with same physical thickness of $t_{ox} = t_k = t_{ox} + t_k$ respectively and, ε_{si}, ε_{ox} and ε_k are the permittivities of the Si, SiO_2 and high-*k* dielectric (*i.e.*, HfO_2) respectively.

$$\psi_{0i}(x) = A_i \exp(\beta_i (x - x_{i-1})) + B_i \exp(-\beta_i (x - x_{i-1})) + Q_i \tag{3.5}$$

where,

$$Q_i = V_{G,i}^{ref} + \frac{qN_i}{\varepsilon_{si}\beta_i^2}, \qquad \beta_i^2 = \frac{2}{\lambda_i^2} \tag{3.6}$$

$\psi_{0i}(x)$ is the centre potential in the channel region R_i $\{i = 1, 2, 3, 4\}$ where, A_i and B_i are the constants to be determined by using the following boundary conditions [Bardon *et al*. (2010)]:

$$\psi_0 = \psi_1(0, y) = -V_T \ln(N_1 / n_i) \tag{3.7}$$

$$\psi_1 = \psi_1(L_1, y) = \psi_2(L_1, y) \tag{3.8}$$

$$\psi_2 = \psi_2(L_1 + L_2, y) = \psi_3(L_1 + L_2, y) \tag{3.9}$$

$$\psi_3 = \psi_3(L_1 + L_2 + L_3, y) = \psi_4(L_1 + L_2 + L_3, y) \tag{3.10}$$

$$\psi_4 = \psi_4(L_1 + L_2 + L_3 + L_4, y) = V_T \ln(N_3 / n_i) + V_{DS} \tag{3.11}$$

$$A_i = \frac{-1}{2\sinh(\beta_i L_i)} \left(\psi_{i-1} \exp(-\beta_i L_i) - Q_i (1 + \exp(-\beta_i L_i)) - \psi_i\right) \tag{3.12}$$

$$B_i = \frac{1}{2\sinh(\beta_i L_i)} \left(\psi_{i-1} \exp(\beta_i L_i) - Q_i (1 + \exp(\beta_i L_i)) - \psi_i\right) \tag{3.13}$$

where, $L_i = x_i - x_{i-1}$ is the length of the region R_i $(i = 1, 2, 3)$ and $\psi_i = \psi_{s,i}(x)$ is the

surface junction potential at $x = x_i$ as shown in Fig. 3.1.

Using continuity of electric field at the interface at $x = x_i \quad (i = 1, 2, 3)$, we write

$$\left.\frac{\partial \psi_{s,i}(x)}{\partial x}\right|_{x=x_i} = \left.\frac{\partial \psi_{s,i+1}(x)}{\partial x}\right|_{x=x_i} \quad \text{at } x = x_i \quad (i = 1, 2, 3) \tag{3.14}$$

Note that the surface potential $\psi_{s,i}(x)$ in the i^{th} segment (for $i = 1, 2, 3$) of Fig. 3.1 can be obtained from Eq. (3.3) along with Eq. (3.5). Using the resultant $\psi_{s,1}$, $\psi_{s,2}$ and $\psi_{s,3}$ in the above equation and solving the resultant three equations for $i = 1, 2$ and 3, the junction potentials ψ_1, ψ_2 and, ψ_3 can be expressed as:

$$\psi_1 = \frac{1}{m_1}\left[n_2\psi_2 - n_1 v_1 - n_2 v_2 + n_1\psi_0\right] \tag{3.15}$$

$$\psi_2 = \frac{1}{\eta_2}\left[n_3 v_3(m_1 m_3 + m_1 n_3) + m_1 n_3 n_4(v_4 - \psi_4) + n_2 m_3(n_1 v_1 + n_2 v_2) + n_2 m_3(v_2 m_1 - n_1\psi_0\right] \tag{3.16}$$

$$\psi_3 = \frac{1}{\eta_3}\left[n_1 n_2 n_3(v_1 - \psi_0) + n_3 v_2(n_2^2 + m_1 n_1) - n_3 v_3(\eta_1 + m_1 n_3) - \eta_1 n_4(v_4 - \psi_4)\right] \tag{3.17}$$

where

$$v_i = \left[1 - \cosh(\beta_i L_i)\right] Q_i; \qquad i = 1,2,3 \tag{3.18}$$

$$n_i = \beta_i / \sinh(\beta_i L_i); \qquad i = 1,2,3 \tag{3.19}$$

$$m_i = \beta_i \coth(\beta_i L_i) + \beta_{i+1} \coth(\beta_{i+1} L_{i+1}); \qquad i = 1,2 \tag{3.20}$$

$$\eta_1 = (m_1 m_2 - n_2^2) \tag{3.21}$$

$$\eta_2 = (m_1 n_3^2 + m_3 n_2^2 - m_1 m_2 m_3) \tag{3.22}$$

$$\eta_3 = (m_3 n_2^2 + m_1 n_3^2 - m_1 m_2 m_3) \tag{3.23}$$

The vertical $E_{yi}(x,y)$ and lateral $E_{xi}(x,y)$ electric fields in any region R_i can be obtained by differentiating the channel potential with respect to vertical and lateral axis as:

$$E_{yi}(x,y) = y\left[V_{G,i}^{eff} - \psi_{0i}(x)\right](\beta_i)^2 \tag{3.24}$$

$$E_{xi}(x,y) = = \beta_i\left(1-(y/\lambda_i)^2\right)\left[A_i \exp(\beta_i(x-x_{i-1})) - B_i \exp(-\beta_i(x-x_{i-1}))\right] \tag{3.25}$$

The source-drain depletion lengths L_1 and L_4 can be given by [Bardon *et al.* (2010)]

$$L_1 = f_1\sqrt{2\varepsilon_{Si}(Q_2 - \psi_0)/(qN_1)} \tag{3.26}$$

$$L_4 = f_2\sqrt{2\varepsilon_{Si}(\psi_4 - Q_3)/(qN_3)} \tag{3.27}$$

where f_1 and f_2 are the fitting parameters with the values of 1.2 and 1.1, respectively. Note that L_1 and L_4 are V_{GS} dependent due to the V_{GS} dependency of Q_2 and Q_3.

3.2.2 Modeling of Drain Current

Using Kane's model [Kane (1960)] for the BTBT generation rate of carriers tunneling from the valence band of the source to the conduction band of the channel can be expressed as [Gholizadeh and Hosseini (2014)]:

$$G_{BTBT} = A_{Kane}E^{\alpha}\exp\left(-\frac{B_{Kane}}{E}\right) \tag{3.28}$$

where E is the local electric field; α is a material-dependent constant parameter (whose value is 2 for direct band gap materials (*e.g.*, InAs) and 2.5 for the indirect band gap materials (*e.g.*, Si)) and, A_{Kane} and B_{Kane} are two tunneling process-dependent parameters which can be described for direct bandgap semiconductor as [Kane (1960)]:

$$A_{Kane} = \left(\frac{q^2 m_r^{1/2}}{18\pi\hbar^2 E_g^{1/2}} \right), \quad B_{Kane} = \left(\frac{\pi m_r^{1/2} E_g^{3/2}}{2q\hbar} \right) \tag{3.29}$$

and for the indirect bandgap materials as [Vandenberghe *et al.* (2011)]:

$$A_{Kane} = \left(\frac{D^2 q^{5/2} (1+\exp(\varepsilon_\perp / kT))(m_C m_V)^{3/2}}{\rho \varepsilon_\perp (1+\exp(\varepsilon_\perp / kT)) 2^{27/4} \pi^{5/2} \hbar^{7/2} m_r^{5/4} E_g^{7/4}} \right) \tag{3.30}$$

$$B_{Kane} = \left(\frac{4(2m_r)^{1/2} E_g^{3/2}}{3q\hbar} \right) \tag{3.31}$$

where D is the deformation potential of transverse acoustic phonons; q is the elementary charge; m_r is the reduced tunneling mass; E_g is the energy band gap of the materials; ρ is the mass density; kT is the thermal energy of the transverse acoustic phonon; $\varepsilon_\perp$ is the transverse acoustic phonon energy; m_v (m_c) is the valence (conduction) band density of states effective mass; and $\hbar$ is the reduced Planck's constant, respectively.

The drain current can be expressed as [Gholizadeh and Hosseini (2014)]:

$$I_d = q \iiint A_{Kane} E_{xi}(x,y) E_{avg}^{\alpha-1} \exp\left(-B_{Kane}/E_{avg}\right) dxdydz \tag{3.32}$$

$E_{xi}(x,y)$ is the lateral electric field in the regions (R_i), $E_{avg} = E_g / q l_{path}$ is the average electric field, l_{path} is the tunneling distance lying between the shortest $(L_t^{\min})$ and longest $(L_t^{\max})$ tunneling paths [Gholizadeh and Hosseini (2014)] and E_g is the energy band gap of Si.

The shortest tunneling path $(L_t^{\min})$ and longest tunneling path $(L_t^{\max})$ are defined as the distances from the source-channel junction to the points along the channel direction

where the surface potentials are changed by E_g/q and $(E_g-\Delta\phi)/q$ with $\Delta\phi$ as the energy difference between the conduction band and valance band of the source. Thus, the shortest tunneling path $(L_t^{\min})$ can be obtained by solving

$$\psi_{s,2}(L_t^{\min})-\psi_0 = E_g/q \tag{3.33}$$

which gives

$$L_t^{\min} = \frac{1}{\beta_2}\ln\left(\frac{R+\sqrt{R^2-4A_2B_2}}{2A_2}\right) \tag{3.34}$$

where

$$R=\frac{1}{k}\left(\psi_0 - Q_2 k - V_{G,i}^{eff}(1-k)+E_g/q\right),\quad k=\left(1-\frac{t_{Si}^2}{4\lambda_2^2}\right) \tag{3.35}$$

Similarly, the longest tunneling path can be obtained from Eq. (3.33) by replacing $L_t^{\min}$ by $L_t^{\max}$ and E_g/q by $(E_g-\Delta\phi)/q$.

The drain current per unit channel width (Amp/μm) can be obtained from Eq. (3.32) as:

$$I_d = q\int_{L_t^{\min}}^{L_t^{\max}}\left(\int_{-t_{si}/2}^{t_{si}/2} A_{Kane}E_{xi}(x,y)E_{avg}^{\alpha-1}\exp\left(-B_{Kane}/E_{avg}\right)dy\right)dx \tag{3.36}$$

If we can assume $L_t^{\max} > (L_1+L_2)$, then Eq.(3.36) can be written as

$$I_d = I_0\left[\int_{L_t^{\min}}^{L_1+L_2}\left(\frac{A_2\exp(-\chi_1 x)}{x^{\alpha-1}}-\frac{B_2\exp(-\chi_2 x)}{x^{\alpha-1}}\right)dx+\int_{L_1+L_2}^{L_t^{\max}}\left(\frac{A_3\exp(-\chi_3 x)}{x^{\alpha-1}}-\frac{B_3\exp(-\chi_4 x)}{x^{\alpha-1}}\right)dx\right] \tag{3.37}$$

where,

$$I_0 = A_{Kane}\beta_2 t_{Si} q^{2-\alpha} E_g^{\alpha-1}\left(1-(t_{si}\beta_2/4)^2\right) \tag{3.38}$$

$$\chi_1 = \chi_3 = \left((qB_{kan}/E_g)-\beta_2\right),\ \chi_2 = \chi_4 = \left((qB_{kan}/E_g)+\beta_2\right) \tag{3.39}$$

Neglecting the variation of $1/x^{\alpha-1}$ in the interval $L_t^{\min} \le x \le L_t^{\max}$ [Dash and Mishra (2015)]; Eq.(3.37) can be simplified as:

$$I_d = I_0\left[\frac{A_2}{\chi_1}\left(M_{L_t^{\min}} - M_{L_1+L_2}\right)+\frac{B_2}{\chi_2}\left(N_{L_1+L_2} - N_{L_t^{\min}}\right)+ \frac{A_3}{\chi_3}\left(M_{L_1+L_2} - M_{L_t^{\max}}\right)+\frac{B_3}{\chi_4}\left(N_{L_t^{\max}} - N_{L_1+L_2}\right)\right] \tag{3.40}$$

where,

$$M_x = \left(\frac{\exp(-\chi_1 x)}{x^{\alpha-1}}\right),\quad N_x = \left(\frac{\exp(-\chi_2 x)}{x^{\alpha-1}}\right) \tag{3.41}$$

where, $x \equiv \left\{L_t^{\min}, L_t^{\max} \text{ and } L_1+L_2\right\}$

Note that M_x and N_x are highly exponentially decaying functions of x. Thus $M_{L_t^{\max}} << M_{L_1+L_2}$, and $N_{L_t^{\max}} << N_{L_1+L_2}$ since $(L_1+L_2) < L_t^{\max}$. Using the above facts, the expression of drain current (I_d) can be approximately written as:

$$I_d \cong I_0\left[\frac{A_2 M_{L_t^{\min}}}{\chi_1}+\left(\frac{A_3}{\chi_3}-\frac{A_2}{\chi_1}\right)M_{L_1+L_2}+\left(\frac{B_2}{\chi_2}-\frac{B_3}{\chi_4}\right)N_{L_1+L_2}-\frac{B_2 N_{L_t^{\min}}}{\chi_2}\right] \tag{3.42}$$

3.2.3 Modeling of Threshold Voltage

To model the threshold voltage (V_{th}), we will use the maximum transconductance (TC) method [Boucart and Ionescu (2008)]. In this method, the threshold voltage is defined

as the gate voltage (V_{GS}) at which g_m possesses the maximum value. Thus, V_{th} can be obtained by solving the following equation:

$$g_m = \frac{\partial I_d}{\partial V_{GS}} \tag{3.43}$$

$$g_m = I_0 \left[\left(\frac{1}{\chi_1} \frac{\partial A_2}{\partial V_{GS}} - A_2 \right) M_{L_t^{\min}} + \frac{M_{L_1+L_2}}{\chi_3} \left(\frac{\partial (A_3 - A_2)}{\partial V_{GS}} \right) + \frac{N_{L_1+L_2}}{\chi_2} \left(\frac{\partial (B_2 - B_3)}{\partial V_{GS}} \right) - \left(\frac{1}{\chi_2} \frac{\partial B_2}{\partial V_{GS}} - B_2 \right) N_{L_t^{\min}} \right] \tag{3.44}$$

$$g_m^{/} = \left. \frac{\partial g_m}{\partial V_{GS}} \right|_{V_{GS}=V_{th}} = \left. \frac{\partial^2 I_d}{\partial V_{GS}^2} \right|_{V_{GS}=V_{th}} = 0 \tag{3.45}$$

3.3 Result and Discussion

In this section, we will compare our model results with the ATLAS^{TM} based TCAD simulation data of our proposed DM DG TFET with SiO_2/HfO_2 stacked gate oxide structure. The Auger recombination, bandgap-narrowing (BGN), Shockley-Read-Hall recombination (SRH), concentration, electric field dependent Lombardi (CVT), and nonlocal BTBT models have been used for TCAD simulation of the proposed device. We have used the acronyms "DMG" and "SMG" to represent the DG TFETs with the dual-material gate electrode under consideration and the single material gate electrode, respectively. The doping concentration of source, channel and drain are $N_1 = 1\times10^{20}\text{cm}^{-3}$, $N_2 = N_3 = 1\times10^{16}\text{cm}^{-3}$ and, $N_4 = 5\times10^{18}\text{cm}^{-3}$ with $L_2 = 20\,\text{nm}$, $L_3 = 50\,\text{nm}$, $L = 50\,\text{nm}$, $t_{ox} = 1\,\text{nm}$, $t_k = 2\,\text{nm}$ $t_{si} = 12\,\text{nm}$, respectively. The tunneling and

auxiliary gate work function are $\varphi_{M_1} = \varphi_t = 4.2\,\text{eV}\,(\text{Mo}, \text{IrO}_2)$ and $\varphi_{M_2} = \varphi_a = 4.6\,\text{eV}\,(\text{Ta}, \text{W})$, respectively.

Figure 3.2 compares the surface potential variation along the channel with and without considering source/drain (S/D) depletion regions. It is observed the model results including the effects of S/D depletion regions are better matched with the TCAD simulation data than the results without considering the depletion regions. Thus, the S/D depletion regions have significant effects on the performance characteristics of the device.

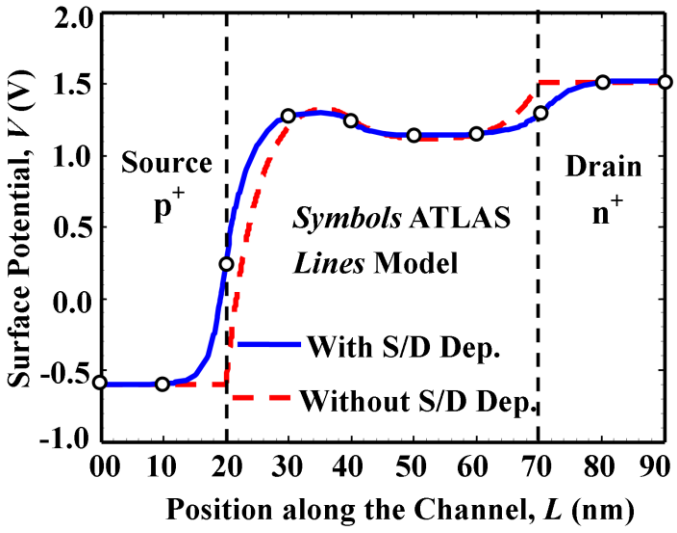

Fig. 3.2: Surface potential along the channel for different models (with S/D Dep. & without S/D Dep.) of DM DG TFET at L_2 = 20nm, L_3 = 30nm, t_{si} = 12nm, V_{DS} = 1V, V_{GS} = 1V, EOT = 1.3nm

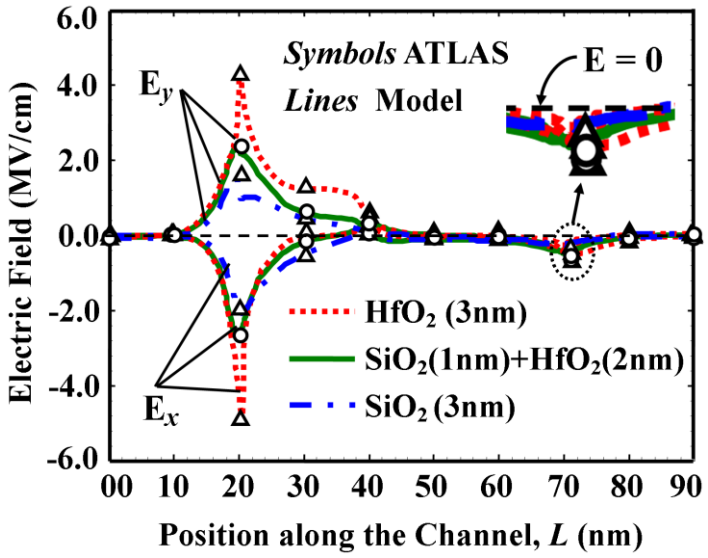

Fig. 3.3: Variation of E_x and E_y along the channel for different combinations of dielectric constant of DM DG TFET at L_2 = 20nm, L_3 = 30nm, t_{si} = 12nm, V_{DS} = 1V, V_{GS} = 1V, EOT = 1.3nm

The variations of lateral (E_x) and vertical (E_y) electric fields with respect to channel position have been plotted in Fig. 3.3 for a fixed gate oxide thickness of 3nm of either HfO_2 or SiO_2 and their combination in the form of a stacked oxide of 3nm. The magnitude of both the electric fields are increased with the increase in the thickness of the high-*k* HfO_2. The negative electric field near the drain side will decelerate the carriers to reduce the ambipolar behavior of the device [Vishnoi and Kumar (2014)].

The energy band diagram along with L_t^{min} and L_t^{max} of our proposed device in its ON-state $(V_{GS} = V_{DS} = 1V)$ of operation obtained from the TCAD simulation has been presented in Fig. 3.4. The plot of L_t^{min} versus V_{GS} in Fig. 3.5 shows a lower value of L_t^{min} in DMG based DG TFET with $\varphi_{M1} = 4.2\,eV$ and $\varphi_{M2} = 4.6\,eV$ than its value in the

SMG based DG TFET with an average work function (~4.4eV) of $\varphi_{M1} = 4.2\,\text{eV}$ and $\varphi_{M2} = 4.6\,\text{eV}$ due to lower the tunneling width resulted from the use of low work function material at the source side in the DMG structure. The transfer characteristics (*i.e.*, I_d vs. V_{GS}) of the DM DG TFET with SiO_2, HfO_2 and SiO_2/HfO_2 stacked gate-oxide of fixed thickness of 3nm shown in Fig. 3.6 confirms the increase in the drain current due to the increase in the high-*k* HfO_2 thickness. This is attributed to the increase in the electric field with the increase in the HfO_2 thickness as demonstrated in Fig. 3.3. The drain current (I_d) versus drain voltage (V_{DS}) graph plotted for different gate voltage (V_{GS}) in Fig. 3.7 shows the increase in I_d with V_{GS} due to the reduction in the source-channel barrier height.

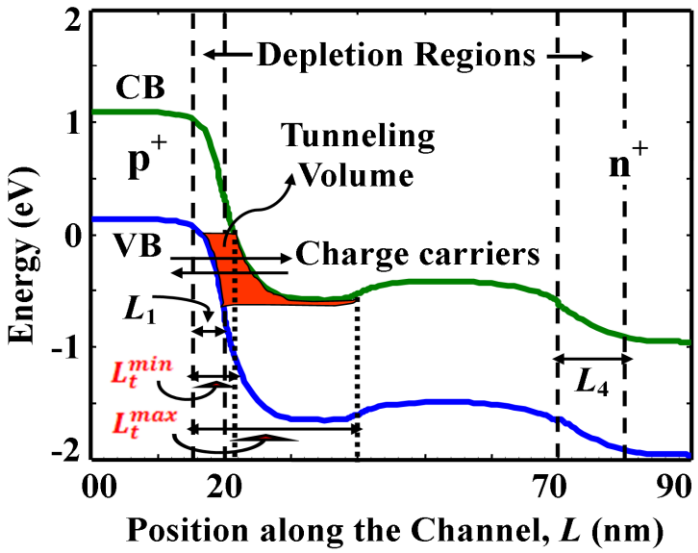

Fig. 3.4: Energy band diagram in ON state (V_{GS} = V_{DS} = 1V) of stacked gate SiO_2/HfO_2 DM DG TFET at L_2 = 20nm, L_3 = 30nm, L = 50nm, t_{si} = 12nm, EOT = 1.3nm

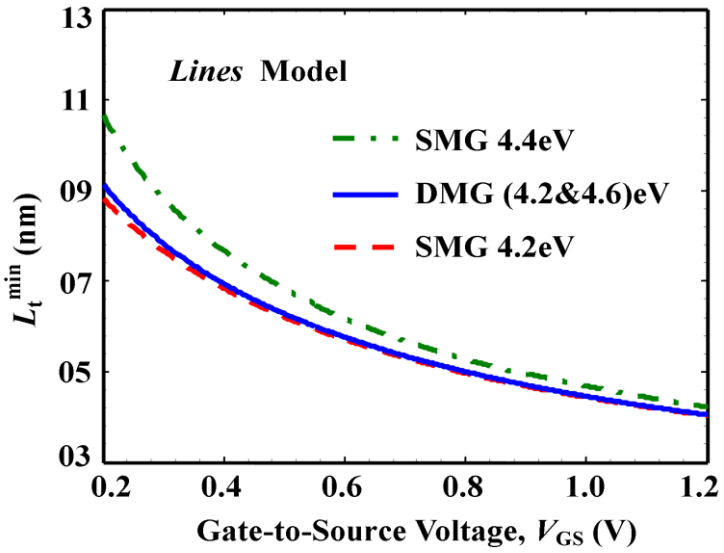

Fig. 3.5: Variation of L_t^{min} against V_{GS} for different combinations of gate work function (φ_M) of stacked gate SiO_2/HfO_2 DG TFET at L = 50nm, t_{Si} = 12nm, V_{DS} = 1V

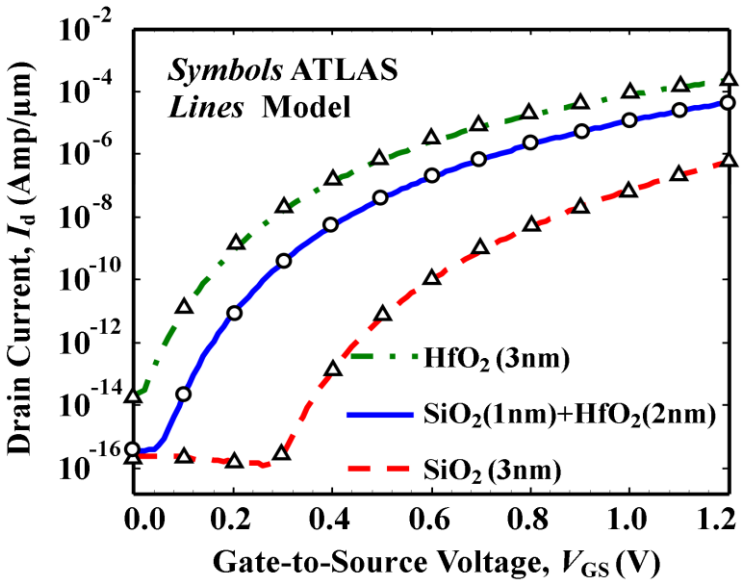

Fig. 3.6: Variation of I_d against V_{GS} for different combinations of dielectric constant of DM DG TFET at L_2 = 20nm, L_3 = 30nm, L = 50nm, t_{si} = 12nm, V_{DS} = 1V

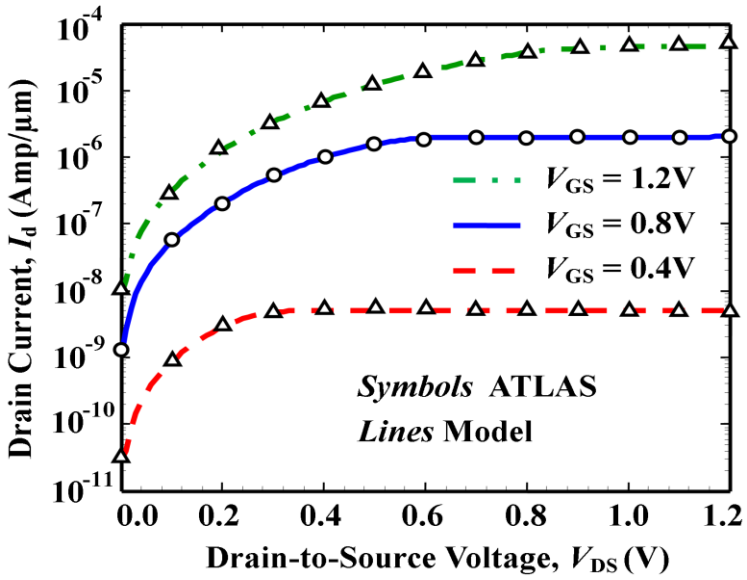

Fig. 3.7: Variation of I_d against V_{DS} for different V_{GS} of stacked gate SiO_2/HfO_2 DM DG TFET at L_2 = 20nm, L_3 = 30nm, L = 50nm, t_{si} = 12nm

The simulated transfer characteristic of the DMG structure with $\varphi_{M1} = 4.2\,\text{eV}$ and $\varphi_{M2} = 4.6\,\text{eV}$ has been compared with that of SMG structures with $\varphi_M = 4.2\,\text{eV}$ and $\varphi_M = 4.4\,\text{eV}$ in Fig. 3.8. It is clearly observed that the ambipolar drain current in the proposed DM DG TFET structure is smaller than the two SMG DG TFET structures under consideration. Further, the ambipolar current is increased with the work function value φ_M in the SMG DG TFETs. On the other hand, the ON current of SMG structure is decreased with the increase in the work function value φ_M. The ON current of the DMG structure is nearly same as that of the SMG structure with $\varphi_M = 4.2\,\text{eV}$ but larger than the SMG structure with gate work function $\varphi_M = 4.4\,\text{eV}$ (*i.e.*, average of $\varphi_{M1} = 4.2\,\text{eV}$ and $\varphi_{M2} = 4.6\,\text{eV}$). The SMG based DG TFETs with φ_{M1} as the gate work function $\varphi_{M1} = 4.2\,\text{eV}$ higher ON current and lower ambipolar current than the corresponding values of SMG structures with the average gate work functions of

$\varphi_{M1} = 4.2$ eV and $\varphi_{M2} = 4.6$ eV. The overall transfer characteristic of the proposed DMG structure is better than SMG structure.

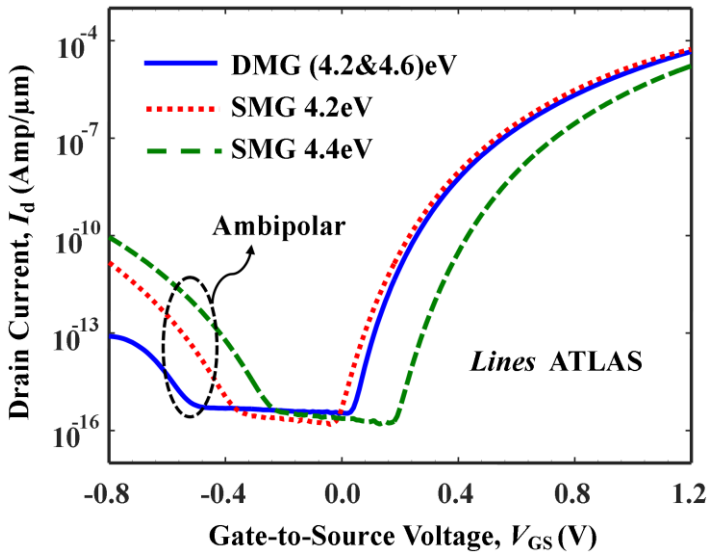

Fig. 3.8: Variation of I_d against V_{GS} for different combinations of gate work function (φ_M) of stacked gate SiO_2/HfO_2 DG TFET at L = 50nm, t_{si} = 12nm, V_{DS} = 1V

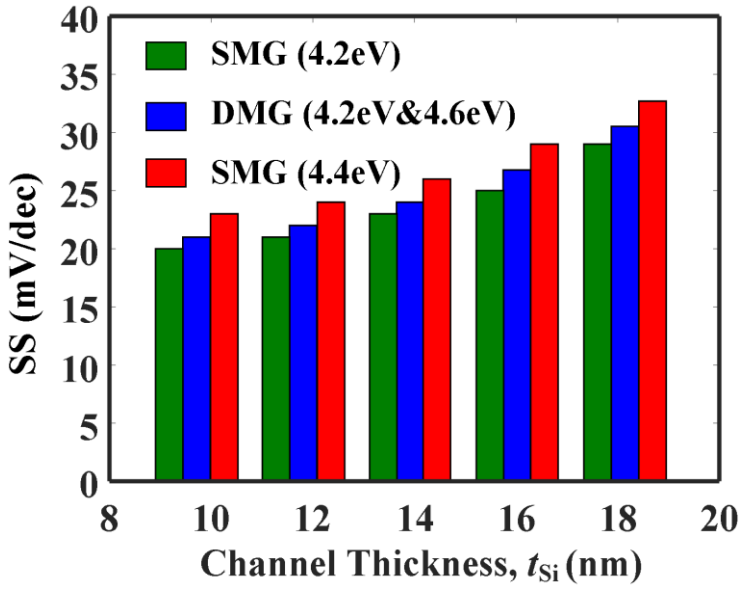

Fig. 3.9: Comparison of point SS against t_{si} for different combinations of gate work function (φ_M) of stacked gate SiO_2/HfO_2 DG TFET at L = 50nm, V_{GS} = V_{DS} = 1V

Fig. 3.9 shows the comparison of the point SS agianst t_{Si} for SMG and DMG based DG TFETs structure. From the figure, it is clear that the DMG based TFETs has lower SS than that of the SMG with work function $\varphi_M = 4.4\,\text{eV}$ and little bit higher SS than the SMG structure with work function $\varphi_M = 4.2\,\text{eV}$. Note that we have obtained point SS from the simulated $I_d - V_{GS}$ curve as the same manner of Boucart and Ionescu [Boucart and Ionescu (2007c)].

Fig. 3.10 and 3.11 show how to find the optimum values of tunneling gate work function (φ_t) and auxiliary gate work function (φ_a) of our proposed device. We have first plotted the transfer characteristics for a fixed work function $(\varphi_a = 4.4\,\text{eV})$ of the auxiliary gate but with different work functions (φ_t) of the tunneling gate as shown in Fig. 3.10. For $\varphi_t < 4.2\text{eV}$, both the ON and OFF currents are observed to be increased with the decrease in φ_t resulting in no significant improvement in the ON/OFF current ratio. However, the improvement in the ON current without degrading the OFF current is observed for $\varphi_t = 4.2\text{eV}$ which gives the optimum value of φ_t. Similarly, following the method suggested by Saurabh and Kumar [Saurabh and Kumar (2011)], we have studied $I_d - V_{GS}$ curve in Fig. 3.11 for the fixed optimum value $\varphi_t = 4.2\text{eV}$ of the tunneling gate but for different values of φ_a. It has been observed that the OFF current increases drastically for $\varphi_a > 4.6\,\text{eV}$ thereby proving the optimum value of φ_a as 4.6eV for obtaining the minimum OFF current due to the minimum ambipolar behavior of the device (see Fig. 3.8). Note that, the main objective of selecting the proper values of φ_t is to maximize the ON current without degrading much the I_{OFF} current. On the other hand, the objective of selecting the proper value of the φ_a is to lower the ambipolar behavior (see Fig. 3.3 & Fig. 3.8) without degrading the I_{ON} current of the device.

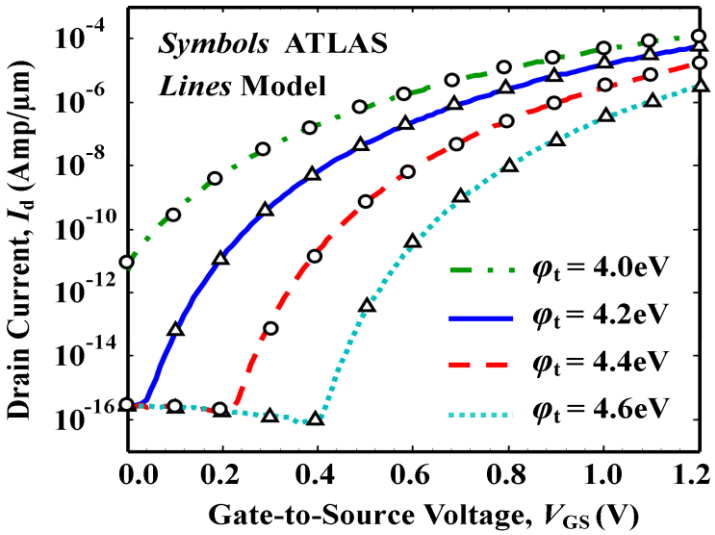

Fig. 3.10: Variation of I_d against V_{GS} for different φ_t of stacked gate SiO_2/HfO_2 DM DG TFET at L_2 = 20nm, L_3 = 30nm, L = 50nm, t_{si} = 12nm, φ_a = 4.4eV, V_{DS} = 1V

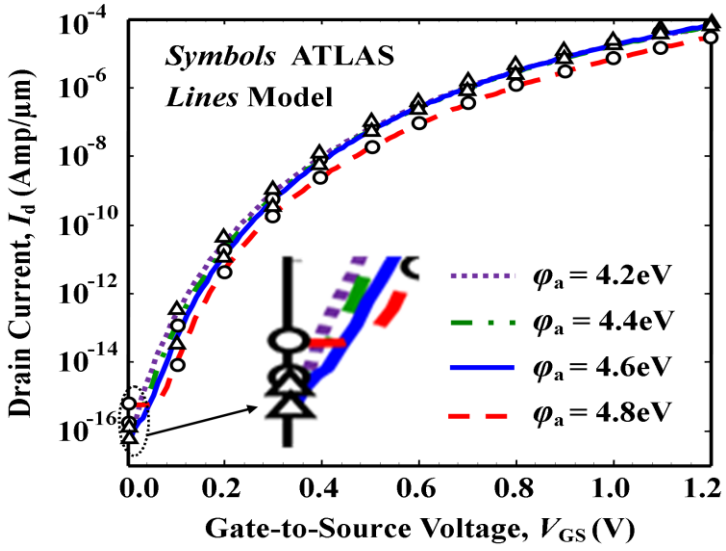

Fig. 3.11: Variation of I_d against V_{GS} for different φ_a of stacked gate SiO_2/HfO_2 DM DG TFET at L_2 = 20nm, L_3 = 30nm, L = 50nm, t_{si} = 12nm, φ_t = 4.2eV, V_{DS} = 1V

Thus, the overall I_{ON}/I_{OFF} ratio of DM DG TFET device is larger than that of the conventional DG TFETs. The transfer characteristics of DM DG TFETs have been shown in Fig. 3.12 for a fixed value of channel length $L = 50\text{nm}$ but for different ratios of tunneling gate length (L_2) and auxiliary gate length (L_3). From the Fig. 3.12, it is observed that the is the best suitable for lowering the OFF current without degrading the ON current. Figure 3.13 represents the transfer characteristics for the fixed $L_2 : L_3 = 2:3$ value but for different channel lengths (L). Note that, unlike the conventional MOSFETs, the OFF current increases with the channel length for $L > 50\text{nm}$. On the other hand, the ON current decreases with the channel length $L = 25\text{nm}$. It is observed that $L = 50\text{nm}$ and $L_2 : L_3 = 2:3$ are the best suitable combination for the higher I_{ON}/I_{OFF} current ratio.

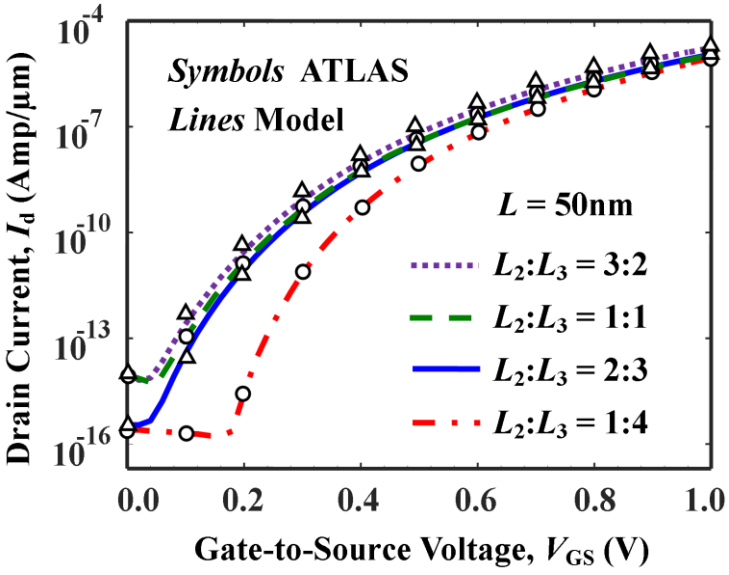

Fig. 3.12: Variation of I_d against V_{GS} for different L_2:L_3 of stacked gate SiO_2/HfO_2 DM DG TFET at L = 50nm, t_{si} = 12nm, EOT = 1.3nm, V_{DS} = 1V

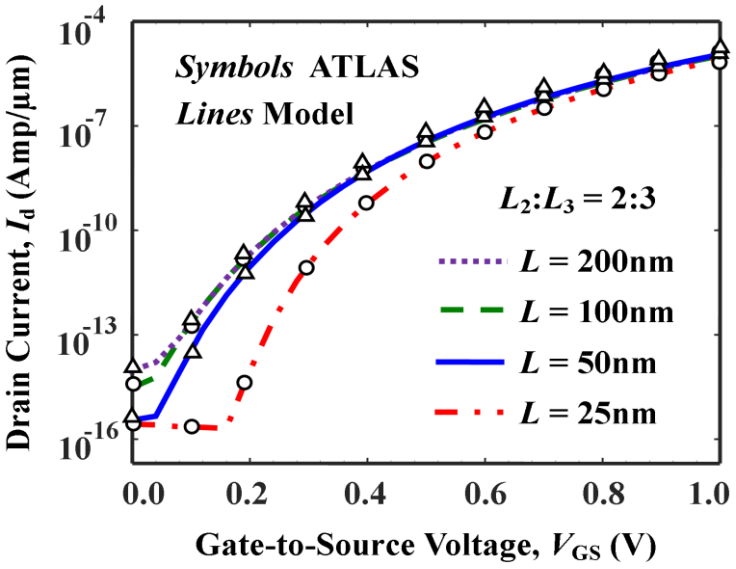

Fig. 3.13: Variation of I_d against V_{DS} for different channel length, L of stacked gate SiO_2/HfO_2 DM DG TFET at $L_2 : L_3$ = 2:3, t_{si} = 12nm, EOT = 1.3nm, V_{DS} = 1V

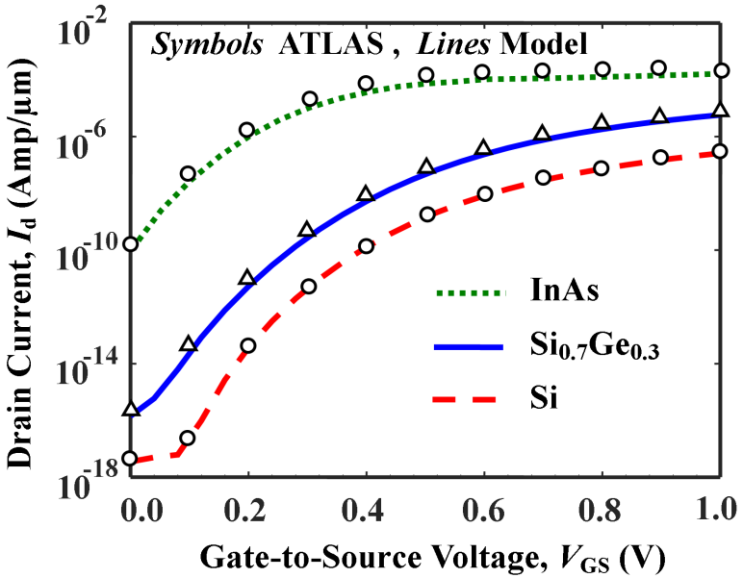

Fig. 3.14: Variation of I_d against V_{GS} for different combinations of energy band gap structures of stacked gate SiO_2/HfO_2 DM DG TFET at L_2 = 20nm, L_3 = 30nm, L = 50nm, EOT = 1.3nm, t_{si} = 12nm, V_{DS} = 1V

TABLE 3.1

TUNNELING PROCESS'S PARAMETERS FOR DIFFERENT BANDGAP MATERIALS OF TFET STRUCTURES

Materials	A_{Kane} $(cm^{-1/2} V^{5/2} s^{-1})$	B_{Kane} **(MV/cm)**	E_g **(eV)**	m_r **(*m*o)**	**Ref.**
Si	4.0×10^{14}	19	1.10	0.087	[ATLAS (2013)]
$Si_{0.7}Ge_{0.3}$	2.6×10^{15}	18	0.96	0.075	[Kao *et al.* (2014)]
InAs	8.1×10^{18}	04	0.36	0.060	[ATLAS (2013)]

TABLE 3.2

KANE'S PARAMETERS FOR TWO DIFFERENT BANDGAP MATERIALS OF TFET STRUCTURES

Materials	m_C (m_o)	m_V (m_o)	***D*** ***e*V/cm**	$\varepsilon_\perp$ ***me*V**	**ρ gm/cm^3**	**Ref.**
Si	0.328	0.549	2.45×10^8	19.0	2.33	[Sze (1981)]
$Si_{0.7}Ge_{0.3}$	0.328	0.485	1.96×10^8	15.9	3.33	[Kao *et al.* (2014)]

We have discussed so far the DM DG TFET structure with Si as the channel materials. The proposed model can also be applied for other materials such as $Si_{0.7}Ge_{0.3}$ (indirect band-gap) and III–V compounds (direct bandgap), and other device structures such as DM SOI TFET. Fig. 3.14 represents the transfer characteristics (*i.e.*, I_d vs. V_{GS}) DM

DG TFET with different materials such as Si, $Si_{0.7}Ge_{0.3}$ and InAs ($\varphi_t = 4.6$eV and $\varphi_a = 4.8$eV, only for InAs). The values of different parameters including A_{Kane} and B_{Kane}, for different materials are given in Table 3.1 and 3.2. The reasonably good matching of the model results with the ATLAS TCAD simulation shows that our model is applicable for direct as well as indirect bandgap materials based-DM DG TFET device.

Fig. 3.15 compares the threshold voltages (V_{th}) of DMG and SMG based DG TFETs. Note that the peak value of the dg_m/dV_{GS} versus V_{GS} curve gives the threshold voltage (V_{th}) of any devices. It is observed that V_{th} of the DMG structure with $\varphi_{M1} = 4.2$ eV and $\varphi_{M2} = 4.6$ eV is lower than the SMG based DG TFETs with the average gate work function (*i.e.*, 4.4eV) of $\varphi_{M1} = 4.2$ eV and $\varphi_{M2} = 4.6$ eV. The variation of V_{th} against t_{si} for different combinations of dielectrics is shown in Fig. 3.16. The V_{th} is increased with t_{si} due to the increase in the lowest tunneling volume.

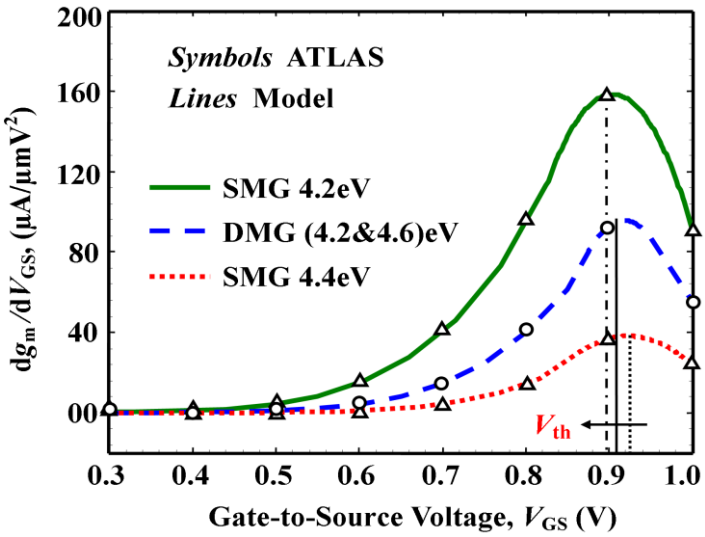

Fig. 3.15: Extraction of V_{th} for different combination of gate work function φ_M by a TC method of stacked gate SiO_2/HfO_2 DG TFET at L = 50nm, t_{si} = 12nm, V_{DS} = 1V

Source doping concentration (N_1) is also an important parameter of any TFET devices. The variation of I_d against V_{GS} for different N_1 is shown in Fig. 3.17. It is observed that the ON current is increased with the increase of source doping concentration $(N_1 > 1\times 20\text{cm}^{-3})$ at the cost of increase in the OFF current, and ON current is decreased with the decrease of source doping concentration $(N_1 < 1\times 20\text{cm}^{-3})$ thereby leading to the deterioration of the overall I_{ON}/I_{OFF} ratio in both cases of the device. However, in case of the DM DG TFETs with $N_1 = 1\times 20\text{cm}^{-3}$ considered in this study, the drain current is improved without deteriorating the OFF state current. Fig. 3.18 shows the variation of V_{th} against N_1 for different combinations of dielectric constant. It is observed that, when N_1 and value of dielectric constant increases, V_{th} decreases. The V_{th} decreases with N_1 and high-*k* dielectrics constant due to the high ON current (see Fig. 3.17) and high electric field (see Fig. 3.3). Thus, our proposed model is more useful for understanding the device physics of any DM TFETs devices.

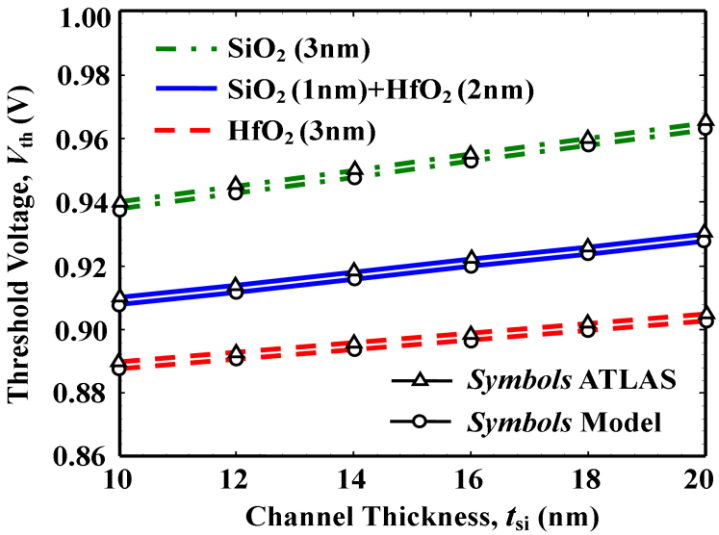

Fig. 3.16: Variation of V_{th} against t_{si} for different combinations of dielectric constant of DM DG TFET at L_2 = 20nm, L_3 = 30nm, L = 50nm, V_{DS} = 1V

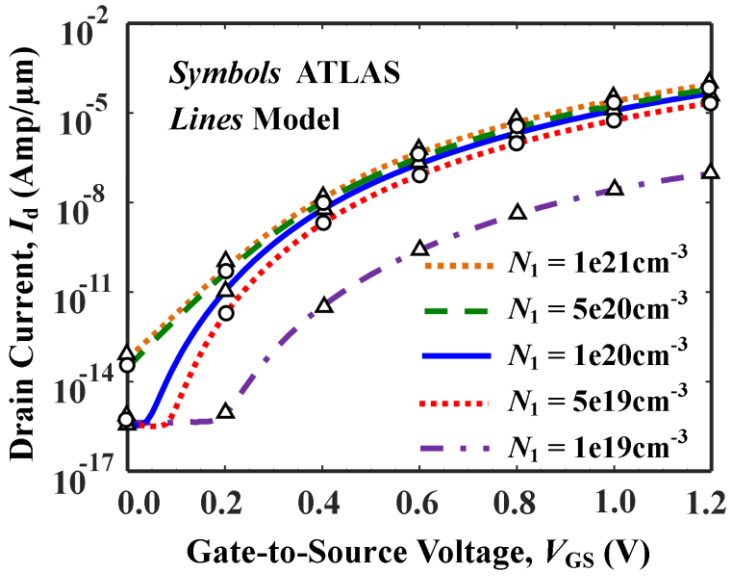

Fig. 3.17: Variation of I_d against V_{GS} for different N_1 of stacked gate SiO_2/HfO_2 DM DG TFET at L_2 = 20nm, L_3 = 30nm, L = 50nm, t_{si} = 12nm, V_{DS} = 1V

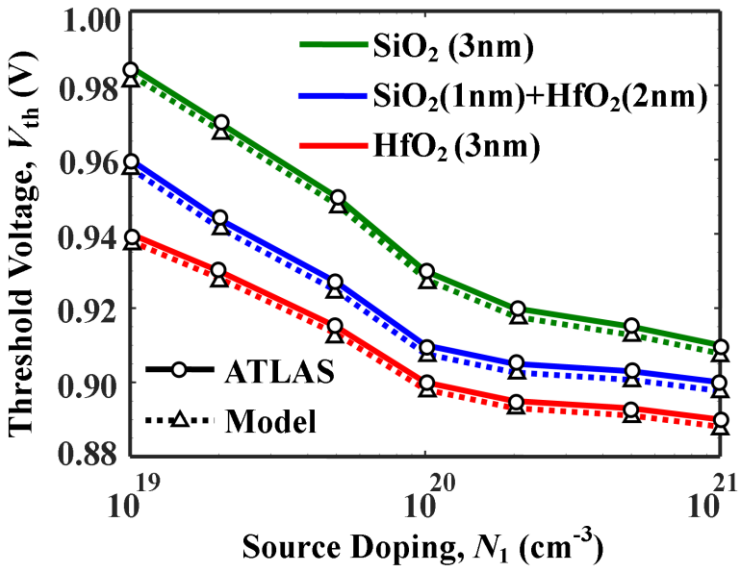

Fig. 3.18: Variation of V_{th} against N_1 for different combinations of dielectric constant of DM DG TFET at L_2 = 20nm, L_3 = 30nm, L = 50nm, t_{si} = 12nm, V_{DS} = 1V

3.4 Conclusion

In this chapter, a 2-D analytical model for surface potential of DM DG TFET with SiO_2/HfO_2 stacked dielectric material has been developed by taking the source/channel and drain/channel depletion regions into consideration. The surface potential model has been developed and used to drive the electric field, drain current model (obtained by analytically integrating the BTBT generation rate over the channel thickness) and threshold voltage model (using the transconductance method). The work functions of the tunneling and auxiliary gates of the DMG structure have been optimized to attain better results in terms of I_{ON}/I_{OFF} ratio, ambipolar effect, and SS of the device. Our proposed model is applicable for both the direct bandgap (*e.g.,* InAs) and indirect bandgap (Si) channel materials. The I_{ON}/I_{OFF} ratio of the SM DG TFET with function 4.2 eV is higher than that of the DM DG TFET and SM DG TFET with work function 4.4 eV. However, the adverse effect due to the ambipolar current of the DM DG structure is the lowest among the above three structures whereas the ambipolar current of the SM DG with work function 4.2eV is lower than that of the SM DG TFET with work function 4.4eV. Model results are found to be in good agreement with the SILVACO ATLAS^{TM} based TCAD simulation data.