Chapter 2

Analytical Modeling for Electrical Characteristics of Double-Gate Tunnel Field-Effect Transistors with a SiO_2/High-k Stacked Gate-Oxide Structure

2.1 Introduction

The tunnel field effect transistors (TFETs), also known as the "Green Transistors" [Hu (2008)], are of great interests for low power digital VLSI applications due to their extremely low OFF-state current and the lowest possible subthreshold swing (SS) even below the minimum SS of 60mV/decade achievable in the conventional MOS transistors [Choi *et al.* (2007), Boucart and Ionescu (2008), Nagavarapu *et al.* (2008), Saurabh and Kumar (2011), Gholizadeh and Hosseini (2014), Kumar and Jit (2015a)] as discussed in Chapter-1. The major drawbacks of the TFETs are their low ON-state current and ambipolar current conduction which restricts the TFETs for inverter based logic circuit applications [Abdi and Kumar (2016)]. The literature survey of Chapter-1 shows that researchers are interested to improve the drain current by replacing the conventional single-gate structure by the double-gate (DG) TFET structures [Boucart and Ionescu (2007c), Bardon *et al.* (2010), Verhulst *et al.,* (2010), Pan and Chui (2012)]. It has been also observed that, instead of using any one of the SiO_2 and high-*k* material as the gate oxide dielectric, the use of a stacked SiO_2/high-*k* gate-oxide structure can significantly improve the SS characteristics of the TFETs [Boucart and Ionescu (2007), Kumar and Jit (2015a), Kumar and Jit (2015b)]. Moreover, the depletion charges of source/channel and drain/channel junctions due to finite doping concentration of source, channel and drain regions play significant roles in determing

the performance characteristics of the TFETs [Bardon *et al.* (2010), Zhang *et al.* (2012), Dutta *et al.* (2016), Dong *et al.* (2016)]. However, to the best of our knowledge, no reported work deals with the analytical modeling of the potential function, electric field, threshold voltage and drain current of the SiO_2/high-*k* stacked gate-oxide based DG TFETs by considering both the effects of depletion charges at the source/channel and drain/channel junctions of the device [Boucart and Ionescu (2007), Kumar and Jit (2015a)]. Thus, the present chapter has been devoted to report a compact analytical model for studying all the major electrical characteristics such as the channel potential, channel electric field, threshold voltage and BTBT current of the SiO_2/high-*k* stacked gate-oxide based DG TFET structures by considering the junction depletion regions for better accuracy.

The surface potential has been obtained by solving the Poisson's equation [Bardon *et al.* (2010)]. The channel electric field is obtained by differentiating the surface potential which has been used for deriving the BTBT drain current by using Kane's model [Kane (1960)]. The concept of shortest tunneling path [Dash and Mishra (2015)] has been used for deriving the drain current of the device. Finally, the threshold voltage characteristics have been modeled from the drain current by the maximum transconductance (TC) method [Booth *et al.* (1987), Chen *et al.* (2015)]. The model results have been compared with the simulation data obtained by commercially available ATLAS™ 2-D device simulator of SILVACO International [ATLAS (2013)] to show the validity of our proposed model. The layout of the present Chapter is given as follows:

Section 2.2 deals with the modeling of the surface potential, channel electric field, drain current and threshold voltage of the SiO_2/high-*k* stacked gate-oxide based DG TFETs under study. Some important model results and related discussions have been

presented in Sec. 2.3. Finally, Sec. 2.4 includes the summary and conclusion of the present chapter.

2.2 Model Formulation

Fig. 2.1 (a) shows the schematic view of DG TFET with SiO_2/High-*k* stacked gate oxide structure considered for our present study. Here L_1, L_2 L_3, t_{ox}, t_k and t_{si} are the length of source/channel depletion region (*i.e.,* R_1 region), the channel length (*i.e.,* R_2 region), drain/channel depletion length (*i.e.,* R_3 region), SiO_2 thickness, high-*k* material thickness and channel thickness of the device, respectively.

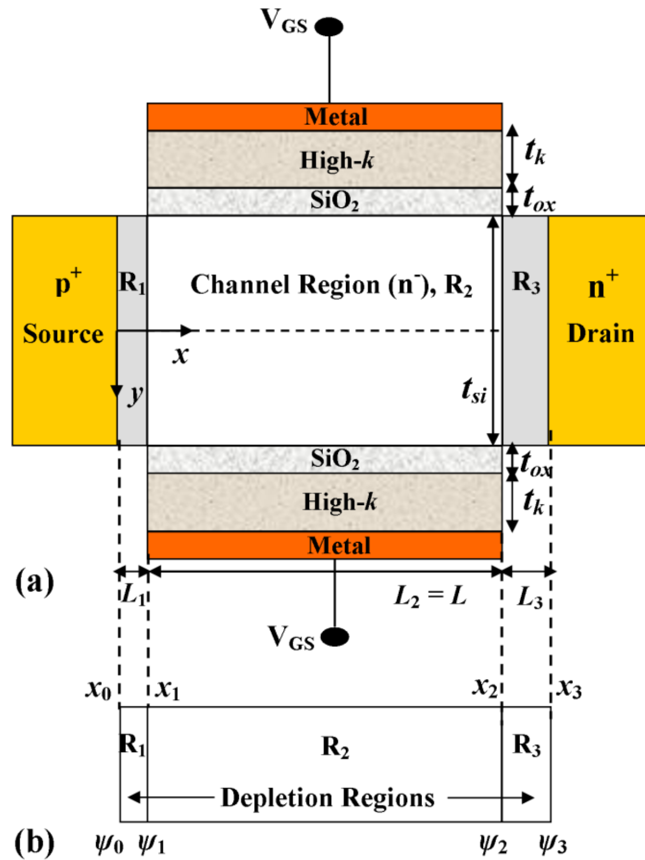

Fig. 2.1: (a) Schematic of high-*k* stacked gate DG TFET and (b) Junction potential of high-*k* stacked gate DG TFET

Note that, in the stacked gate dielectric structure, the high-*k* dielectric has not been used directly on the Si channel to avoid the lattice mismatching related issues in the channel [Boucart and Ionescu (2007)]. The x and y axes have been considered along with the channel length and channel oxide thickness, respectively, as shown in Fig. 2.1 (a). Fig. 2.1 (b) represents the junction potentials, say ψ_0, ψ_1, ψ_2 and ψ_3 at $x_0 = 0$, $x_1 = L_1$, $x_2 = L_1 + L_2$ and $x_3 = L_1 + L_2 + L_3$ respectively, along the channel.

2.2.1 Modeling of Surface Potential

Let $\psi_i(x, y)$ be the 2-D potential distribution function in the channel region R_i for $(i = 1, 2, 3)$ measured with respect to Fermi potential. The 2-D Poisson's equation is given by

$$\frac{\partial^2 \psi_i(x, y)}{\partial x^2} + \frac{\partial^2 \psi_i(x, y)}{\partial y^2} = \frac{-qN_i}{\varepsilon_{si}} \qquad i = 1, 2, 3 \tag{2.1}$$

where $N_1 = 1\times10^{20}\text{cm}^{-3}$, $N_2 = 1\times10^{16}\text{cm}^{-3}$ and $N_3 = 5\times10^{18}\text{cm}^{-3}$ are assumed to be the doping concentrations of the source, channel and drain regions, respectively, to achieve maximum ON-to-OFF current ratio [Wang *et al.* (2004)] and the sign is taken negative for source region and positive for channel and drain regions, respectively.

Using the parabolic potential approximation, the 2-D channel potential function $\psi_i(x, y)$ in the region R_i $(i = 1, 2, 3)$ can be expressed as [Young (1989)]:

$$\psi_i(x, y) = C_{0i}(x) + C_{1i}(x)y + C_{2i}(x)y^2 \tag{2.2}$$

where, $C_{0i}(x)$, $C_{1i}(x)$ and $C_{2i}(x)$ are arbitrary functions of x to be determined by using the following boundary conditions [Bardon *et al.* (2010)]:

$$\left.\frac{\partial \psi_i(x,y)}{\partial y}\right|_{y=\pm t_{Si}/2} = \pm \frac{r_i}{t_{Si}}\left[V_G^{ref} - \psi_{b(f)s}(x)\right] \tag{2.3}$$

$$\psi_0 = \psi_1(0,y) = -V_T \ln(N_1/n_i) \tag{2.4}$$

$$\psi_1 = \psi_2(L_1, y) \tag{2.5}$$

$$\psi_2 = \psi_2(L_1 + L_2, y) \tag{2.6}$$

$$\psi_3 = \psi_3(L_1 + L_2 + L_3, y) = V_T \ln(N_3/n_i) + V_{DS} \tag{2.7}$$

where, $\psi_{bs}(x)$ and $\psi_{fs}(x)$ are the surface potentials under the back gate and front gate of the device, respectively; V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage, $V_G^{ref} = (V_{GS} - \varphi_{MS}) = (V_{GS} - \varphi_M + \chi_{Sub} + E_g/2)$ is the gate voltage with respect to the Fermi potential, $(\varphi_M = 4.4\text{eV})$ (*e.g.*, Mo) is gate metal work function, $(\chi_{Sub} = 4.05\text{eV})$ is the electron affinity of Si , and $r_i = C_i/C_{Ch}$ is the ratio between the equivalent gate-oxide capacitance, say C_i, in the region R_i; and the channel region capacitance $C_{Ch} = \varepsilon_{si}/t_{si}$.

Note that the high-*k* dielectric of thickness t_k can be thought as an equivalent SiO_2 (oxide) layer of thickness $(\varepsilon_{ox} t_k/\varepsilon_k)$ and hence the stacked gate dielectric structure can be assumed to be a single SiO_2 layer with an equivalent oxide capacitance $C_2 = \varepsilon_{ox}/t_{eq}$ where $(t_{eq} = t_{ox} + \varepsilon_{ox} t_k/\varepsilon_k)$ [Chiang and Chen (2007)] is the equivalent oxide thickness (EOT) with ε_{ox} and ε_k representing the permittivities of silicon-dioxide and high-*k* dielectric, respectively. The fringing field effect has been included into account by the conformal mapping techniques in the depletion region R_1 and R_3, as $C_{1,3} \cong (2/\pi)\, \varepsilon_{ox}/t_{eq}$ [Lin and Kuo (2003)].

Using Eq. (2.2) in Eq. (2.3), we obtain $C_{0i}(x)=\psi_{0i}(x)$, $C_{1i}(x)=0$ and $C_{2i}(x)=\left(V_G^{eff}-\psi_{0i}(x)\right)/\lambda_i^2$ where $\psi_{0i}(x)=\psi_i(x,0)$ is the central channel potential in the region R_i and

$$\lambda_i=\sqrt{\frac{(4+r_i)t_{si}^2}{4r_i}} \tag{2.8}$$

is the characteristic length of the device associated with the center channel potential $\psi_{0i}(x)$. Denoting the surface potential in region R_i as $\psi_{s,i}(x)=\psi_i(x,\pm t_{Si}/2)$, 2-D channel potential $\psi_i(x,y)$ and surface potential $\psi_{s,i}(x)$ can be written as:

$$\psi_i(x,y)=\psi_{0i}(x)+\left[V_G^{eff}-\psi_{0i}(x)\right](y/\lambda_i)^2 \tag{2.9}$$

$$\psi_{s,i}(x)=\psi_{0i}(x)+\left[V_G^{eff}-\psi_{0i}(x)\right](t_{Si}/2\lambda_i)^2 \tag{2.10}$$

At the center ($y=0$), the Poisson's equation (2.1) can be written as:

$$\left.\frac{\partial^2\psi_i(x,y)}{\partial x^2}\right|_{y=0}+\left.\frac{\partial^2\psi_i(x,y)}{\partial y^2}\right|_{y=0}=\left.\frac{-qN_i}{\varepsilon_{si}}\right|_{y=0} \tag{2.11}$$

Substituting Eq. (2.2) in Eq. (2.11), we can obtain 1-D differential equation in terms of the center potential $\psi_{0i}(x)$ as:

$$\frac{d^2\psi_{0i}(x)}{dx^2}-\beta_i^2\,\psi_{0i}(x)=-\beta_i^2\,P_i \tag{2.12}$$

where,

$$P_i=V_G^{ref}+\frac{qN_i}{\varepsilon_{si}\beta_i^2},\quad \beta_i^2=\frac{2}{\lambda_i^2} \tag{2.13}$$

The solution of Eq. (2.12) gives the generalized center channel potential $\psi_{0i}(x)$ in the region R_i $(i=1,2,3)$, can be written as

$$\psi_{0i}(x) = A_i \exp(\beta_i (x - x_{i-1})) + B_i \exp(-\beta_i (x - x_{i-1})) + P_i \tag{2.14}$$

where,

$$A_i = \frac{-1}{2\sinh(\beta_i L_i)} \left(\psi_{i-1} \exp(-\beta_i L_i) - P_i (1 + \exp(-\beta_i L_i)) - \psi_i \right) \tag{2.15}$$

$$B_i = \frac{1}{2\sinh(\beta_i L_i)} \left(\psi_{i-1} \exp(\beta_i L_i) - P_i (1 + \exp(\beta_i L_i)) - \psi_i \right) \tag{2.16}$$

where, $L_i = x_i - x_{i-1}$ is the length of region R_i $(i = 1, 2, 3)$ and $\psi_i = \psi_{s,i}(x_i)$ is the surface potential at $x = x_i$ as shown in Fig. 2.1 (b). The intermediate junction potentials ψ_1 and ψ_2 can be obtained by the continuity of lateral electric field at the surface. The intermediate junction potentials ψ_i $(i = 1, 2)$ between the segment i and $(i+1)$ are obtained by the following continuity of electric field property:

$$\left. \frac{\partial \psi_{s,i}}{\partial x} \right|_{x=x_i} = \left. \frac{\partial \psi_{s,(i+1)}}{\partial x} \right|_{x=x_i} \quad \text{at } x = x_i \quad (i = 1, 2) \tag{2.17}$$

Note that the potential $\psi_{s,i}$ in the ith segment (for $i = 1, 2, 3$) of Fig. 2.1 (b) can be obtained from Eq. (2.10) along with Eqs. (2.14)-(2.16). Using the resultant $\psi_{s,1}$, $\psi_{s,2}$ and $\psi_{s,3}$ in the above equation and solving the resultant two equations for $i = 1$ and 2, the junction potentials ψ_1 and ψ_2 can be expressed as:

$$\psi_1 = \frac{1}{\eta} \left[m_2 n_1 (\psi_0 - \varphi_1) - (m_2 + n_2) n_2 \varphi_2 + n_2 n_3 (\psi_3 - \varphi_3) \right] \tag{2.18}$$

$$\psi_2 = \frac{1}{\eta} \left[n_1 n_2 (\psi_0 - \varphi_1) - (m_1 + n_2) n_2 \varphi_2 + m_1 n_3 (\psi_3 - \varphi_3) \right] \tag{2.19}$$

where

$$\varphi_i = \left[1 - \cosh(\beta_i L_i) \right] P_i; \qquad i = 1,2,3 \tag{2.20}$$

$$n_i = \beta_i / \sinh(\beta_i L_i); \qquad i = 1,2,3 \tag{2.21}$$

$$m_i = \beta_i \coth(\beta_i L_i) + \beta_{i+1} \coth(\beta_{i+1} L_{i+1}); \qquad i = 1,2 \tag{2.22}$$

$$\eta = (m_1 m_2 - n_2^2) \tag{2.23}$$

2.2.2 Modeling of Electric Field Intensity

The lateral and vertical electric fields $E_{xi}(x, y)$ and $E_{yi}(x, y)$ in any region R_i can be described as:

$$\begin{aligned} E_{xi}(x, y) &= -\frac{\partial \psi_i(x, y)}{\partial x} \\ &= \beta_i \left(1 - (y/\lambda_i)^2\right)\left[A_i \exp(\beta_i (x - x_{i-1})) - B_i \exp(-\beta_i (x - x_{i-1}))\right] \end{aligned} \tag{2.24}$$

$$E_{yi}(x, y) = 2yC_{2i}(x) \tag{2.25}$$

2.2.3 Length of Junction Depletion Regions

Since the TFET can be viewed as a PIN diode whose body potential can be modulated by the gate voltage [Sze (1981)], the length of the depletion region L_1 of R_1 and L_3 of R_3 can be obtained by considering the two separate junctions (source-channel and drain-channel junction). So, the length of the depletion regions depends on P_2, which is the potential in the channel due to the gates without the influence of the junctions. Then L_1 and L_3 can be written as [Bardon *et al.* (2010)]:

$$L_1 = \sqrt{2\varepsilon_{Si}(P_2 - \psi_0)/(qN_1)} \tag{2.26}$$

$$L_3 = \sqrt{2\varepsilon_{Si}(\psi_3 - P_2)/(qN_3)} \tag{2.27}$$

Note that L_1 and L_3 are V_{GS} dependent due to the V_{GS} dependency of P_2.

2.2.4 Modeling of Drain Current

In this subsection, we will present the analytical expression of the drain current (I_d). Using Kane's model [23] for the BTBT generation rate of carriers tunneling from the valence band of the source to the conduction band of the channel, the drain current (I_d) can be expressed as [Kane (1960)]:

$$I_d = q\int_{TFET-volume} A_{Kane}\, E_{x2}(x, y)\, E_{avg}^{\alpha-1} \exp\left(-\frac{B_{Kane}}{E_{avg}}\right) dV \tag{2.28}$$

where $A_{Kane} = 4\times10^{14}\ \text{cm}^{-1/2}\text{V}^{-5/2}\text{s}^{-1}$ and $B_{Kane} = 1.9\times10^{7}\ \text{V/cm}$ are two tunneling process-dependent parameters [Gholizadeh and Hosseini (2014), ATLAS (2013)]; $E_{x2}(x, y)$ is the lateral electric field in the region R_2 (in which tunneling takes place); α is a material-dependent constant, whose value is 2 for direct band gap material and 2.5 for the indirect band gap material (e.g. Si); $E_{avg} = E_g/(ql_{path})$ is an average electric field [Gholizadeh and Hosseini (2014)] where l_{path} is the tunneling path distance varying from the shortest tunneling path distance, say $L_t^{\min}$ to the largest tunneling path distance, say $L_t^{\max}$. The shortest tunneling path distance $(L_t^{\min})$ of the TFET device is the horizontal distance between $x = 0$ and the point $x = L_t^{\min}$ in the R_2 region where the surface potential is changed by the unit band-gap potential (E_g/q) [Dash and Mishra (2015)]. Thus we can write

$$\psi_{s,2}(L_t^{\min}) - \psi_0 = E_g/q \tag{2.29}$$

which gives

$$\left(A_2 \exp(\beta_2 L_t^{\min}) + B_2 \exp(-\beta_2 L_t^{\min})\right) = S \tag{2.30}$$

where

$$k = \left(1 - \frac{t_{Si}^2}{4\lambda_2^2}\right), \quad S = \frac{1}{k}\left(\psi_0 - P_2 k - V_G^{eff}(1-k) + E_g/q\right) \tag{2.31}$$

Finally, solving the Eq. (2.30) for $L_t^{\min}$, we can write

$$L_t^{\min} = \frac{1}{\beta_2}\ln\left(\frac{S + \sqrt{S^2 - 4A_2B_2}}{2A_2}\right) \tag{2.32}$$

Similarly, the longest tunneling path distance, $(L_t^{\max})$ of the TFET device is defined as the lateral distance between $(x=0)$ to the point where the surface potential is differed by $(E_g + E_{VS} - E_{VC})/q$ [Gholizadeh and Hosseini (2014)]. where, E_{VS} and E_{VC} are the energy of valance band of source and channel regions, respectively.

Assuming a fixed channel width of $1\mu m$, Eq. (2.28) for the drain current (I_d) can now be expressed in the unit of $(\text{Amp}/\mu m)$ as:

$$I_d = q \int_{-t_{Si}/2}^{t_{Si}/2} \left(\int_{L_t^{\min}}^{L_t^{\max}} A_{Kane}\, E_{x2}(x,y)\, E_{avg}^{\alpha-1} \exp\left(-\frac{B_{Kane}}{E_{avg}}\right) dx \right) dy \tag{2.33}$$

Using Eq. (2.24) with $i = 2$ in Eq. (2.33), the drain current (I_d) can be written after integration as:

$$I_d = I_o \left[\int_{L_t^{\min}}^{L_t^{\max}} \left(\frac{A_2 \exp\left(-\left(\left((qB_{kan}/E_g) - \beta_2\right)\right)x\right)}{x^{\alpha-1}} - \frac{B_2 \exp\left(-\left(\left((qB_{kan}/E_g) + \beta_2\right)\right)x\right)}{x^{\alpha-1}} \right) dx \right] \tag{2.34}$$

where I_0 is the dc current which depends only constant parameters and is defined as:

$$I_0 = A_{Kane}\, t_{Si}\, q^{2-\alpha} E_g^{\alpha-1} \beta_2 \left(1 - (t_{si}\beta_2/4)^2\right) \tag{2.35}$$

$$I_d = I_o \left[\int_{L_t^{\min}}^{L_t^{\max}} \left(\frac{A_2 \exp(-\gamma_1 x)}{x^{\alpha-1}} - \frac{B_2 \exp(-\gamma_2 x)}{x^{\alpha-1}} \right) dx \right] \tag{2.36}$$

where,

$$\gamma_1 = \left((qB_{kan}/E_g) - \beta_2\right),\ \ \gamma_2 = \left((qB_{kan}/E_g) + \beta_2\right) \tag{2.37}$$

Note that Eq. (2.36) cannot be represented in a closed form expression. However, assuming that variation of $1/x^{\alpha-1}$ in the interval $L_t^{min} \le x \le L_t^{max}$ is negligible as compared to that of the exponential term [Dash and Mishra (2015)], Eq. (2.36) can be approximated as:

$$I_d \approx I_0\left[-\frac{A_2}{\gamma_1}\left(M_{L_t^{max}} - M_{L_t^{min}}\right) + \frac{B_2}{\gamma_2}\left(N_{L_t^{max}} - N_{L_t^{min}}\right)\right] \tag{2.38}$$

where M_x and N_x are expressed as:

$$M_x = \frac{\exp(-\gamma_1 x)}{x^{\alpha-1}},\ \ N_x = \frac{\exp(-\gamma_2 x)}{x^{\alpha-1}} \tag{2.39}$$

Note that $M_{L_t^{max}} << M_{L_t^{min}}$ and $N_{L_t^{max}} << N_{L_t^{min}}$ since $L_t^{max} > L_t^{min}$. Thus, the drain current can be further approximated as:

$$I_d \approx I_0\left[\frac{A_2 M_{L_t^{min}}}{\gamma_1} - \frac{B_2 N_{L_t^{min}}}{\gamma_2}\right] \tag{2.40}$$

2.2.5 Modeling of Threshold Voltage

Generally, there are two methods to determine the threshold voltage (say, V_{th}) of the TFETs: constant current (CC) [Bhuwalka (2005)] and transconductance (TC) [Booth (1987), Dash and Mishra (2005)] methods. However, the TC method is believed to be more practical than the CC method [Chen *et al.* (2013)]. In this method, the V_{th} is defined as the gate voltage, V_{GS} at which $g_m^{/} = \partial g_m/\partial V_{GS}$ possesses the maximum value [Booth (1987), Dash and Mishra (2005)] where $g_m = \partial I_d/\partial V_{GS}$ is the transconductance

and $g_m^{/}$ is the rate of change of g_m with respect to V_{GS}. Using Eq. (2.40), we can write

$$g_m = I_0\left(\frac{M_{L_t^{\min}}}{\gamma_1}\frac{\partial A_2}{\partial V_{GS}} + \frac{A_2}{\gamma_1}\frac{\partial M_{L_t^{\min}}}{\partial V_{GS}} - \frac{B_2}{\gamma_2}\frac{\partial N_{L_t^{\min}}}{\partial V_{GS}} - \frac{N_{L_t^{\min}}}{\gamma_2}\frac{\partial B_2}{\partial V_{GS}}\right) \tag{2.41}$$

$$g_m^{/} = I_0\left(\frac{2K_1}{\gamma_1}\frac{\partial M_{L_t^{\min}}}{\partial V_{GS}} + \frac{A_2}{\gamma_1}\frac{\partial^2 M_{L_t^{\min}}}{\partial V_{GS}^2} - \frac{2K_2}{\gamma_2}\frac{\partial N_{L_t^{\min}}}{\partial V_{GS}} - \frac{B_2}{\gamma_2}\frac{\partial^2 N_{L_t^{\min}}}{\partial V_{GS}^2}\right) \tag{2.42}$$

where, $K_1 = \dfrac{\partial A_2}{\partial V_{GS}}$ and $K_2 = \dfrac{\partial B_2}{\partial V_{GS}}$ are the constant parameter.

Note that the peak value of the $g_m^{/}$ vs V_{GS} plot gives the threshold voltage of the device. Thus, V_{th} can be obtained by solving the following equation:

$$g_m^{/} = \left.\frac{\partial g_m}{\partial V_{GS}}\right|_{V_{GS}=V_{th}} = \left.\frac{\partial^2 I_d}{\partial V_{GS}^2}\right|_{V_{GS}=V_{th}} = 0 \tag{2.43}$$

2.3 Results and Discussion

In this section, we will present some model results along with their corresponding ATLAS™ TCAD based simulation data to show the validity of our proposed model. The non-local band-to-band tunneling (BTBT), Shockley-Read-Hall recombination (SRH), concentration & electric field dependent Lombardi (CVT), Auger recombination and bandgap-narrowing (BGN) model have been used in the TCAD for the transport behavior of high-*k* DG TFET under consideration. In this chapter, we have used HfO_2 material in the place of high-*k* dielectric constant. We first present the variation of surface potential along the channel for different gate voltage (V_{GS}) in Fig. 2.2. Except the sharp changes at the source/channel and drain/channel junctions, the potential is observed to be nearly constant in the entire channel region for a fixed gate

voltage. However, when V_{GS} is increased, the potential is also increased everywhere in the channel including at the source and drain junctions. Further, for a significant increase in the V_{GS} (*i.e.,* $V_{GS} > 1\,\text{V}$), the source depletion region is extended towards the source whereas the drain depletion region is reduced due to the increase and decrease in the reverse bias voltages at the source/channel and drain-channel junctions. The variation of the surface potential along the channel for different drain voltages (V_{DS}) in Fig. 2.3 clearly shows that the effect of V_{DS} on the entire channel potential of the device is negligible except at the drain depletion region. This implies that the short-channel effects (SCEs) including the drain induced barrier lowering (DIBL) is nearly independent of V_{DS} in our proposed high-k DG TFETs structure.

The variations of the source and drain depletion lengths (*i.e,.* L_1 and L_3 respectively) with V_{GS} compared in Fig. 2.4 shows that the drain depletion length is more sensitive to V_{GS} than source depletion length, especially at low V_{GS} regions. Since L_1 and L_3 are V_{GS} dependent parameters, their effects on the modeling of TFET characteristics can't be neglected. The proposed model is thus believed to provide better accuracy over the many existing models developed by neglecting L_1 and L_3 [Gholizadeh and Hosseini (2014), Dash and Mishra (2015)]. We have now considered the variations of the lateral (E_x) and vertical (E_y) electric fields as a function of channel position in Fig. 2.5 for different combinations of dielectric constant. It is observed that, except near the vicinity of the source/channel junctions, both the electric fields is almost zero in the entire channel region. Further, they are increased in magnitude with the increase in the dielectric constant of the high-k material.

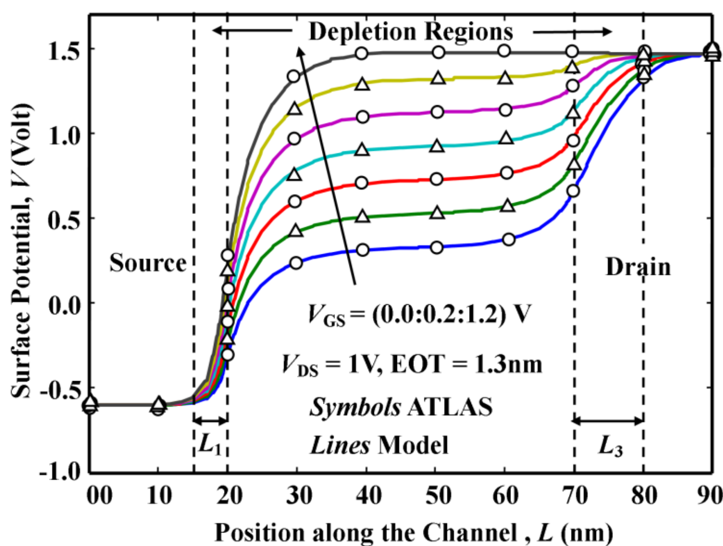

Fig. 2.2: Surface potential along the channel for different V_{GS} of stacked gate SiO_2/HfO_2 DG TFET at $L = 50$nm, $t_{si} = 12$nm, $\varphi_M = 4.4$eV

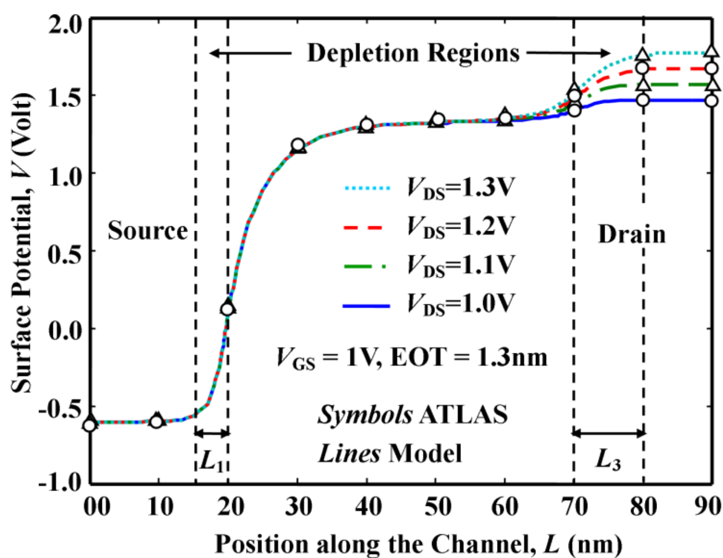

Fig. 2.3: Surface potential along the channel for different V_{DS} of stacked gate SiO_2/HfO_2 DG TFET at $L = 50$nm, $t_{si} = 12$nm, $\varphi_M = 4.4$eV

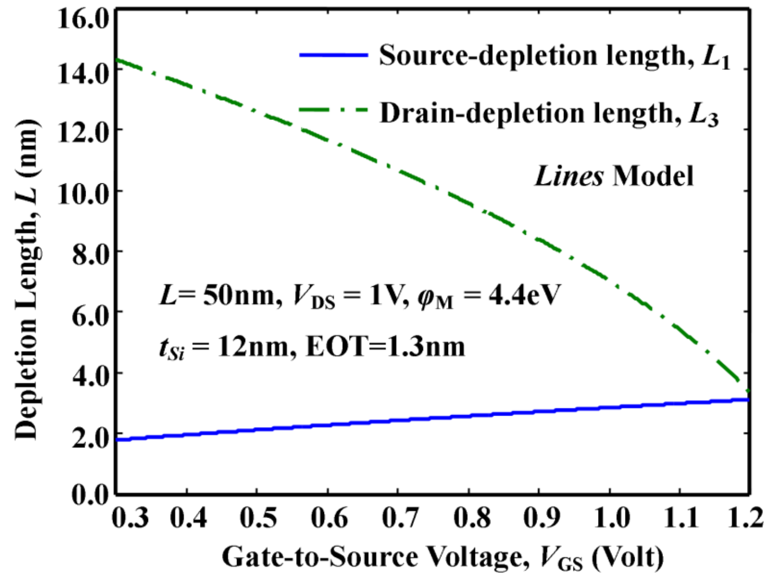

Fig. 2.4: Variation of depletion length against V_{GS} of stacked gate SiO_2/HfO_2 DG TFET at $L = 50\text{nm}$, $t_{si} = 12\text{nm}$, $\varphi_M = 4.4\text{eV}$

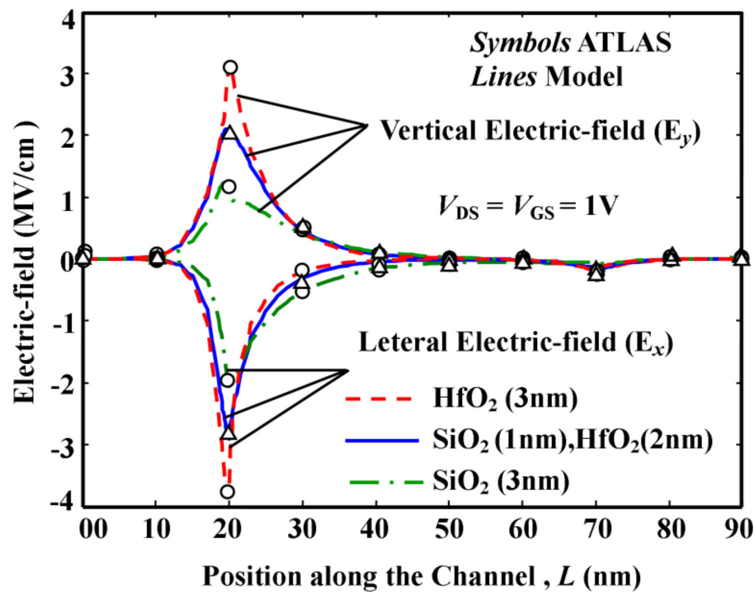

Fig. 2.5: Variation of E_y and E_x along the channel for different combinations of dielectric constant DG TFET at $L = 50\text{nm}$, $t_{si} = 12\text{nm}$, $\varphi_M = 4.4\text{eV}$

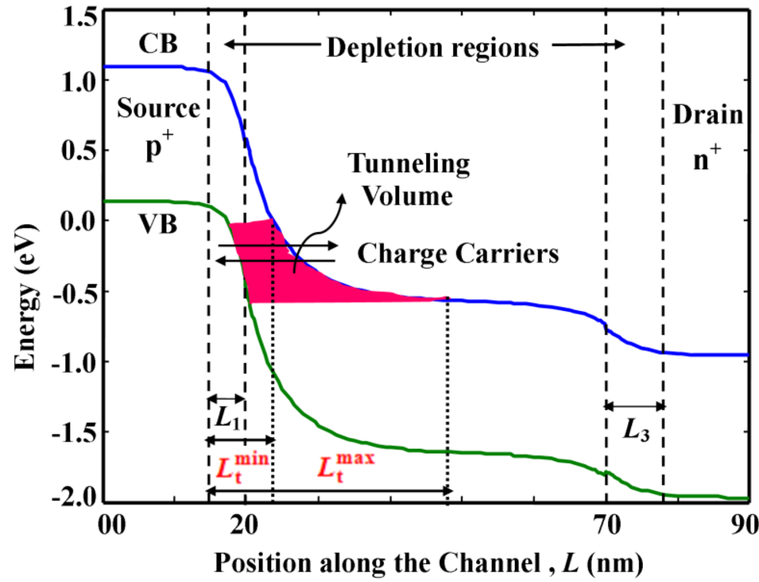

Fig. 2.6: Energy band diagram of stacked gate SiO_2/HfO_2 DG TFET in ON-state $(V_{GS}=V_{DS}=1\text{ V})$ at $L=50$nm, $t_{si}=12$nm, $\varphi_M=4.4$eV

To examine the tunneling mechanism, the ON-state energy band diagram of the proposed structure obtained from the TCAD simulation is shown in Fig. 2.6. Note that no drain current can be achieved unless significant BTBT of electrons from the valence band of the source to the conduction of the intrinsic channel at the source/channel junction occurs.

The shortest $(L_t^{\min})$ and longest $(L_t^{\max})$ tunneling paths under a typical ON-state condition have been shown in Fig. 2.6. The variation of $L_t^{\min}$ as a function of V_{GS} for different combinations of gate dielectric constants is shown in Fig. 2.7.

It is observed that $L_t^{\min}$ is decreased with the increase in V_{GS} as well as the dielectric constant of the high-*k* material. The variation of $L_t^{\min}$ with V_{GS} for different channel thickness (t_{si}) shown in Fig. 2.8 shows that $L_t^{\min}$ is increased with t_{si} due to the increase in the tunneling barrier. Fig. 2.9 shows the drain current (I_d) variation as a function of

V_{GS} for different combination of SiO_2 and HfO_2 at gate dielectric layer. The increase in I_d in Fig. 2.9 with the introduction of HfO_2 may be attributed to the increased tunneling owing to the increased E_x at the source/channel junction (see Fig. 2.5).

The plot of I_d versus V_{GS} for different channel thickness (t_{si}) is shown in Fig. 2.10. The decrease in I_d with increase in t_{si} is due to the decrease in the non-local BTBT volume resulted from the decreased value of $L_t^{\min}$. Fig. 2.11 shows the variation of drain current (I_d) as a function of V_{DS} for different channel thickness (t_{si}) and V_{GS}. It is observed from the fig. 2.11 that the drain current decreases with increasing t_{si} due to the decrease in the tunneling volume. Since the barrier height decreases with the increase in V_{GS}, more number of electrons can enter from the source to the channel region; thereby increasing the resulting drain current as shown in the figure.

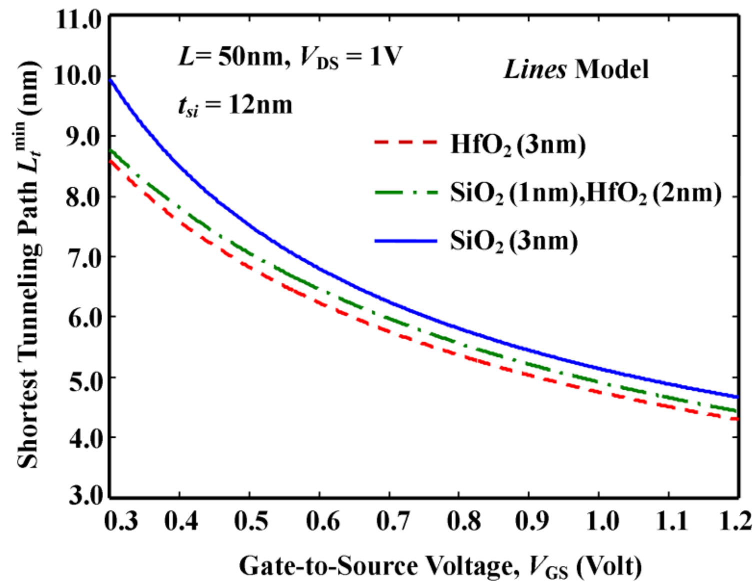

Fig. 2.7: Variation of L_t against V_{GS} for different combination of dielectric constant of DG TFET

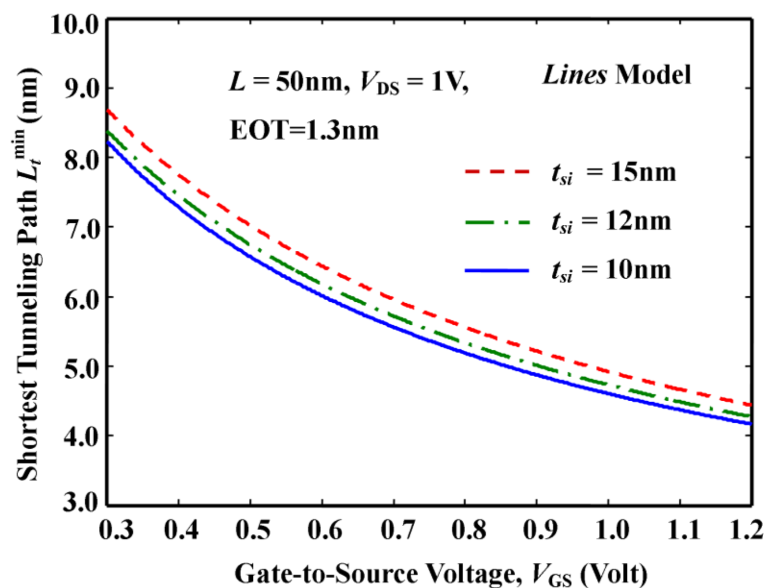

Fig. 2.8: Variation of L_t against V_{GS} for different t_{Si} of stacked gate SiO_2/HfO_2 DG TFET

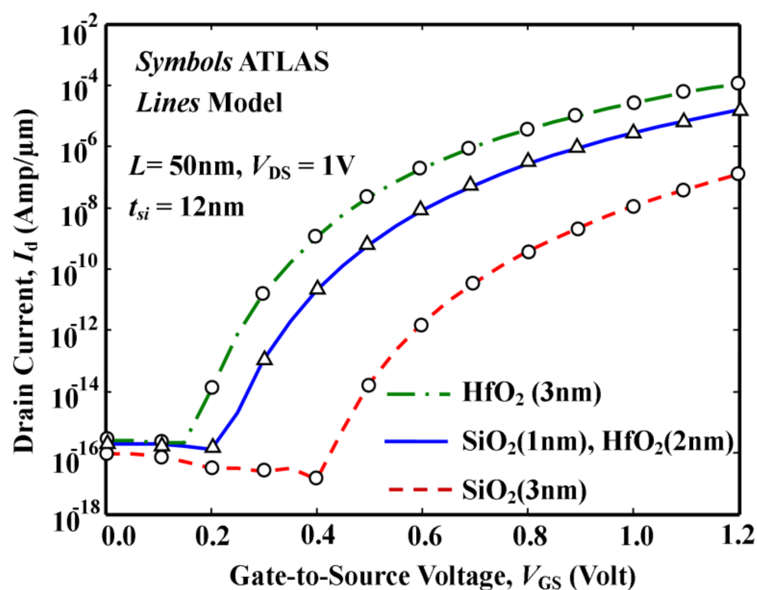

Fig. 2.9: Variation of I_d against V_{GS} for different combination of dielectric constant of DG TFET

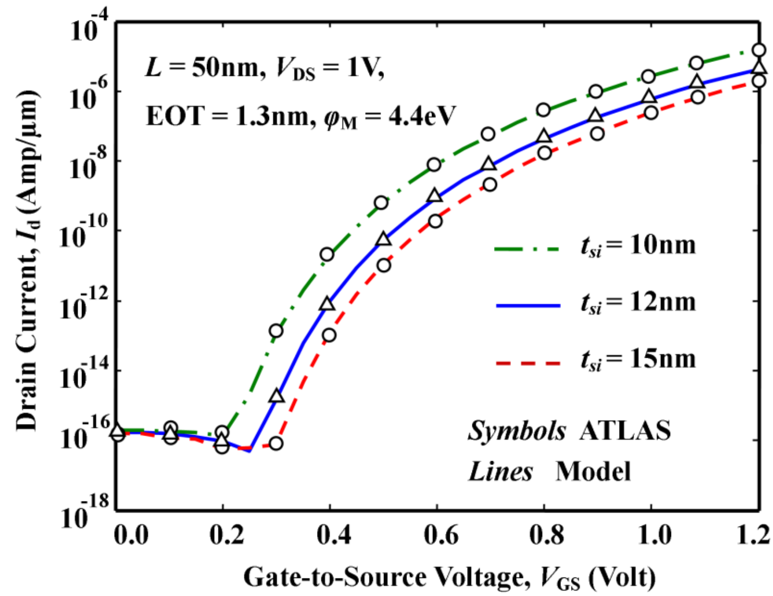

Fig. 2.10: Variation of I_d against V_{GS} for different t_{Si} of stacked gate SiO_2/HfO_2 DG TFET

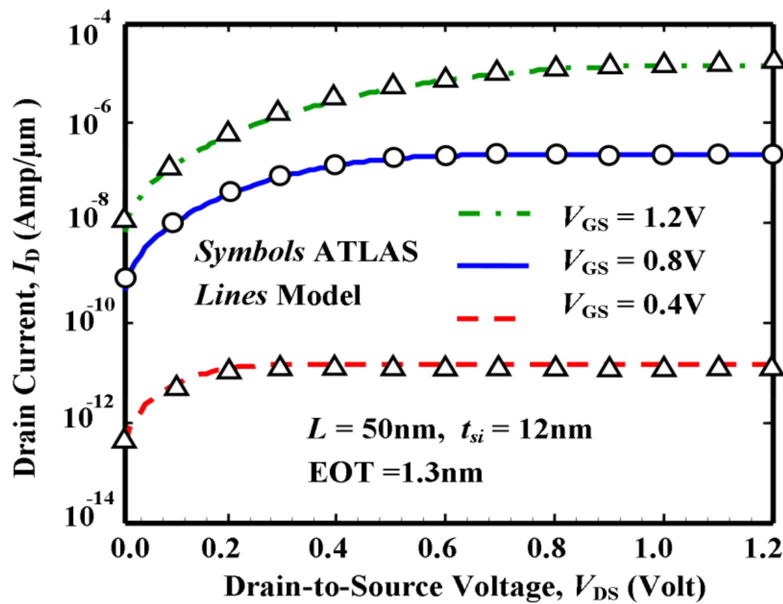

Fig. 2.11: Variation of I_d against V_{DS} for different V_{GS} of stacked gate SiO_2/HfO_2 DG TFET

The variation of point subthreshold swing (SS) against channel thickness (t_{si}) for different combinations of dielectric constant as illustrated in Fig. 2.12, signifies that SS increases with an increase of channel thickness while decreases, due to decreasing the drain current with channel thickness (see Fig. 2.10). From the figure, it is also observed that SS decreases with an increase of dielectric constant, because of drain current increases with dielectric constant (see Fig. 2.9).

The variations of I_d, g_m and dg_m/dV_{GS} with V_{GS} have been plotted in Fig. 2.13 for drain voltage of 1V. Note that the peak value of the dg_m/dV_{GS} versus V_{GS} curve gives the threshold voltage (V_{th}) as shown in Fig. 2.13. The dg_m/dV_{GS} versus V_{GS} plots for different channel thickness (t_{si}) shown in Fig. 2.14 demonstrate the increase in V_{th} with t_{si} due to reduction in the tunneling volume owing to the increase in $L_t^{\min}$.

The variation of V_{th} with L for different combinations of SiO_2 and HfO_2 plotted in Fig. 2.15 shows that V_{th} is nearly independent of L (*i.e.,* threshold voltage roll-off is almost zero) due to the dependency of tunneling on the source-channel junction characteristics only, not on the entire channel region. It is further observed from the Fig. 2.15 that, for a constant combined thickness of the stacked gate oxide structure, V_{th} is decreased with the increase in the thickness of the high-*k* dielectric due to the lowering of the energy barrier at the source/channel interface region.

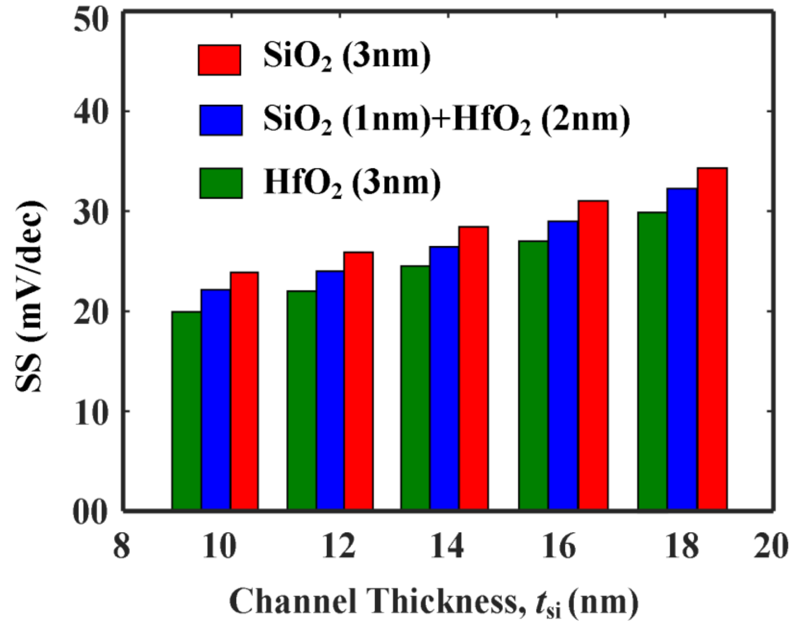

Fig. 2.12: Variation of point SS against t_{Si} for different combinations of dielectric constant for DG TFET at V_{GS} = 1V, V_{DS} = 1V, L = 50nm, t_{si} = 12nm

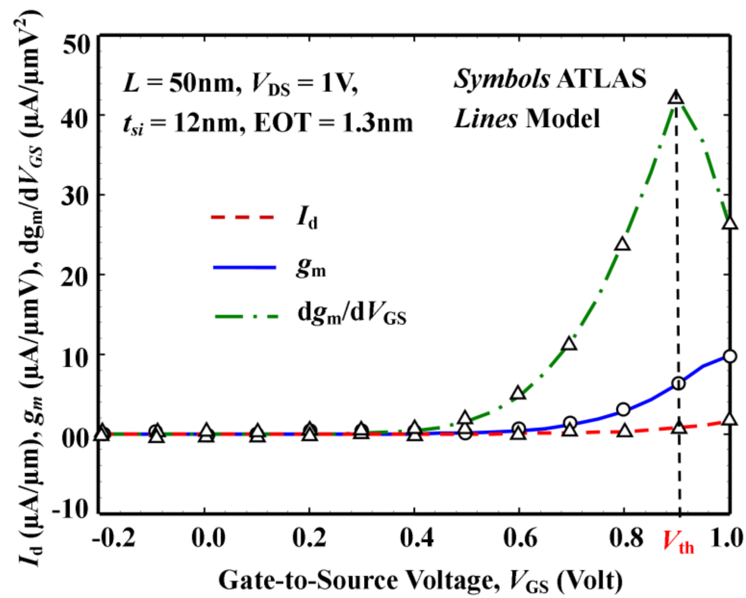

Fig. 2.13: Extraction of V_{th} from current parameters of stacked gate SiO_2/HfO_2 DG TFET by TC method

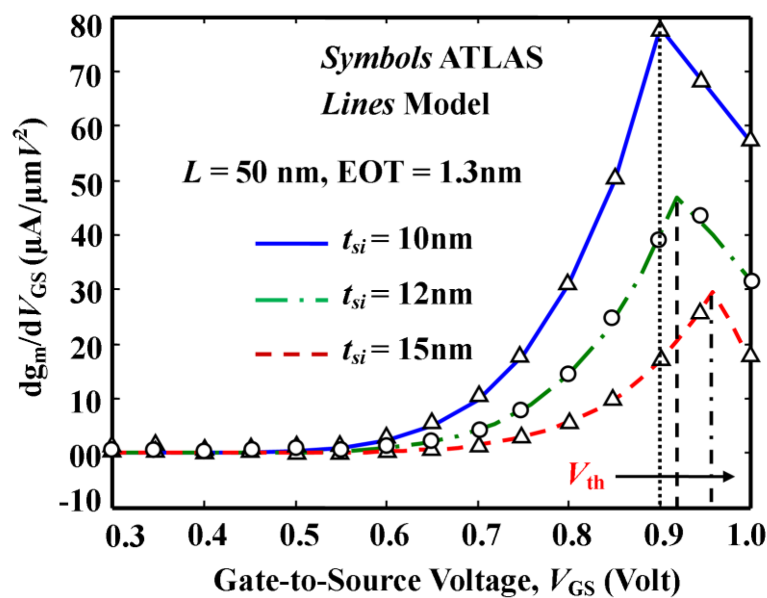

Fig. 2.14: Extraction of V_{th} of stacked gate SiO_2/HfO_2 DG TFET by TC method for different t_{Si}

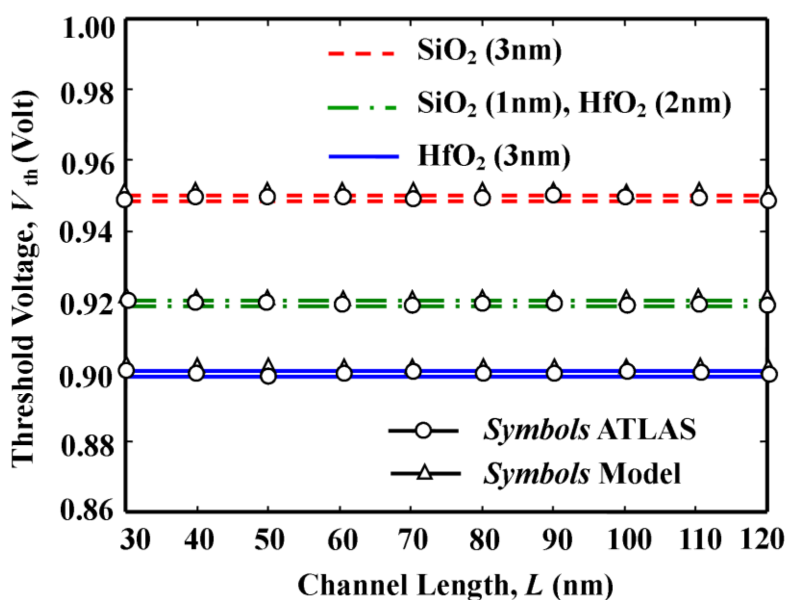

Fig. 2.15: Variation of V_{th} against L for different combinations of dielectric constant for DG TFET at $V_{DS} = 1$V, $t_{si} = 12$nm, $\varphi_M = 4.4$eV

2.4 Conclusion

In this chapter, a compact 2-D analytical model has been developed for studying all the major electrical characteristics such as the channel potential, electric field, threshold voltage and drain current of a SiO_2/HfO_2 stacked gate-oxide structure based DG TFET with finite concentration of the source and drain doping for the first time. The electric field dependent BTBT generation rate has been modeled by considering the source and drain junction depletion regions. The tunneling current has been modeled by exploring the concept of the shortest tunneling path (L_t^{min}). Finally, the threshold voltage model has been derived from the drain current using the transconductance method. While the threshold voltage is observed to be increased with the Si channel thickness, it decreased with the increase in the high-*k* dielectric thickness. Further, the threshold voltage is observed to be nearly independent of the channel length which implies a nearly zero threshold voltage roll-off in our proposed structure. A good agreement between the model results and ATLAS™ based simulation data shows the validity of our proposed model.