Chapter 1

Introduction and Scope of the Thesis

1.1 Introduction

A revolution in the semiconductor industry was started with the invention of the bipolar junction transistors (BJT) by William Shockley, John Bardeen, and Walter Brattain in 1947 at the Bell Laboratory. This discovery had stimulated the desire of electronics engineers to design more and more complex electronic circuits and systems by interconnecting hundreds or thousands of discrete electronic components such as transistors, diodes, rectifiers and capacitors. Jack Kilby (along with Robert Noyce) had realized the practical difficulties in interconnecting these thousands of components to thousands of bits of wire by the then existing expensive, time-consuming and unreliable hand-soldering method. To overcome the problem, Kilby (along with Robert Noyce) then discovered the concept of the Integrated Circuit (IC) technology in 1958 for which he was awarded the Nobel Prize in Physics on December 10, 2000. However, the main growth and development in the IC technology was boosted up with the practical realization and characterization of another low-power high-speed transistor, called the metal-oxide-semiconductor field effect transistor (MOSFET), by Kahng and Atalla in 1960 [Kahng and Atalla (1960)]. Since then, the MOSFETs have been the more preferred active component than the BJT for the high performance IC technology due to their possibility of having higher drive current [Streetman and Banerjee (2006)], smaller

transit time for the charge carriers, higher speed of operation, better switching characteristics and better feasibility of their size miniaturization through scaling [Sviličić and Kraš (2006)]. The use of a combination of p-type and n-type MOSFETs in the form of the well-known complementary metal–oxide–semiconductor, abbreviated as CMOS, in the ICs has given the birth of a new technology called the "CMOS technology" which is extensively explored for constructing the modern microprocessors, microcontrollers, static RAM, and other digital logic circuits. The everlasting desire of developing complex multifunctional microprocessor systems by integrating billions of CMOS circuits on a single wafer of particular size for the high performance computing and communication applications have led to the miniaturization of the MOSFETs through scaling.

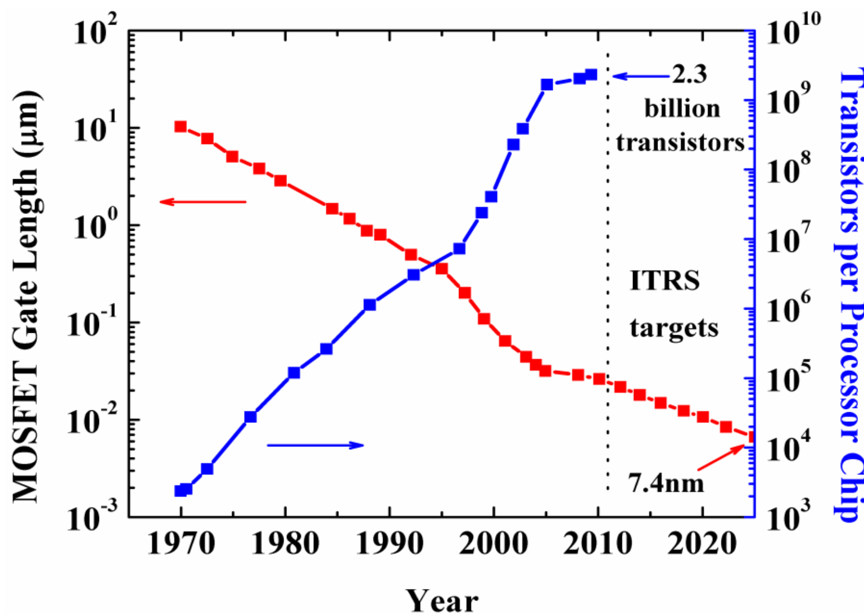

Fig. 1.1: The ITRS roadmap of transistor development [Internet resource (IR1)]

Gordon E. Moore, the co-founder of the *Fairchild Semiconductor* and *Intel*, observed in 1965 that the number of components per integrated circuit (IC) had doubled every year since the invention of the IC technology and predicted that this rate of growth would

continue for at least another decade [G. E. Moore (1965)]. In 1975, he revised his forecast to doubling every two years for the next decade [G. E. Moore (1975)]. This prediction of G. E. Moore, commonly known as *Moore's law*, has become the guiding principle behind the tremendous growth and development of the IC technology in the microelectronics industry which is still valid even after more than four decades. As a consequence to the Moore's law, the number of transistors in the ICs of different generations of microprocessors has increased from a few to the billions during last more than four decades as described in Fig. 1.1 [Internet resource (IR1)]. In order to accommodate more and more number of CMOS circuits in the given area of an IC, there is a natural demand for reducing the device dimensions through scaling. Figure 1.1 also illustrates the variation of MOSFET gate length (in μm) from 10 μm in 1970 to a predicted value of 7.4 nm in 2025.

Ideally, scaling of MOSFET transistors is basically the miniaturization of the device geometry without deteriorating the device performance. Thus, along with the reduction in the gate length of the MOSFETs, the values of other device parameters such as the oxide thickness, channel thickness, applied bias voltages, threshold voltages, doping concentration etc., are also required to be modified to achieve the optimum performance. In this direction, two types of primary scaling rules have been proposed in the literature: constant electric field scaling [Dennard *et al.* (1974)] and constant voltage scaling [Taur and Ning (1998)]. Under constant electric field scaling proposed by Dennard *et al.* [Dennard *et al.* (1974), the main objective was fixed to maintain the electric fields everywhere within the miniaturized device same as the corresponding electric fields of the original device before scaling. According to this scaling principle, if the channel length of a MOS device is scaled by a factor 'α', then the supply voltages,

source/drain channel junction depth, channel thickness, gate-oxide thickness, and the threshold voltage are also scaled by the same factor 'α' while the substrate doping is increased by the factor 'α'. The major drawback of this scaling theory is the requirement of different supply voltages for differently scaled transistors. Further, the reduction in the supply voltage below a certain value is not feasible for practical operation of the transistors. Thus, the constant voltage scaling was introduced by Taur and Ning [Taur and Ning (1998)] where the objective was to reduce device dimensions by a factor 'α' and increase the doping concentration by the same factor 'α' while maintaining the same supply voltage for different versions of scaling. The major drawback of this constant voltage scaling is the increase in the electric fields with the scaling generations which may result in the velocity saturation of carriers in the channel [Zhou and Long (1998)], hot carrier effects [Long *et al.,* (1999), Zhou (2000)] avalanche breakdown [Taur and Ning (1998)] etc. Thus, the scaling of the supply voltage (V_{DD}) and the threshold voltage (V_{th}) of the MOS transistors is also required along with the reduction in the device dimensions. To create bridge between the constant field and constant voltage scaling rules discussed above, several generalized scaling rules have been proposed in the literature [Arora (1993)]. One of the alternatives is the *quasi-constant voltage scaling* in which the supply voltage does not scale as fast as the device dimensions. In this scheme, the supply voltage is reduced by a different factor smaller than α used for scaling the device dimensions [Arora (1993)]. Figure 1.2 shows the reduction in the supply voltage (V_{DD}) and threshold voltage (V_{th}) by approximately one-fifth and half of their corresponding original values due to scaling of CMOS from 1.4μm to 65nm technology node [Packan (2007)]. Further, the figure also shows the decrease in the gate overdrive voltage with the technology generation nodes which, in

turn, may degrade the switching performance of the MOS transistors due to the deterioration of the ratios of I_{ON}/I_{OFF} and $C_g V_{DD}/I_{ON}$ where C_g, I_{ON} and I_{OFF} are the gate capacitance, ON-state and OFF-state current of the MOSFET, respectively. Since the supply voltage (V_{DD}) can be allowed to decrease beyond a certain limit, it has been fixed at approximately 1V for 90 nm technology node and beyond [Nilsson (2006)].

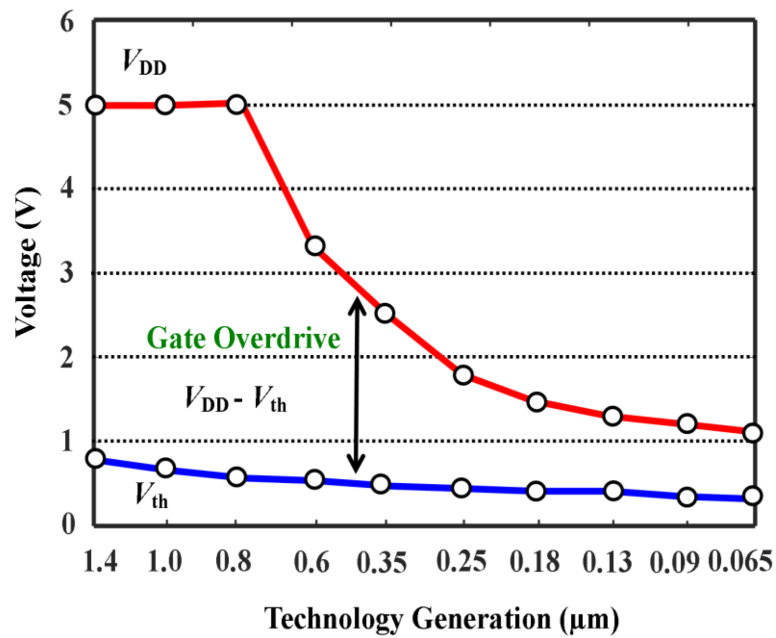

Fig. 1.2: Variation of supply voltage and threshold voltage against technology generation [Packan (2007)]

It is clear that the CMOS technology scaling is a result of the increased demand for transistor density (*i.e.,* number of transistors per unit area) in the modern multifunctional complex IC technology. However, the scaling has imposed the serious threat to the power management of the ICs due to the increase in the active power ($P_{Activec}$) and subthreshold power (P_{Sub}) losses described by [Nilsson (2006)]

$$P_{Activec} = fC_{load}V_{DD}^2 \quad (1.1)$$

$$P_{Sub} = V_{DD} I_{OFF} \tag{1.2}$$

where, C_{load} is the load capacitance; f is the frequency; and I_{OFF} is the OFF-state current of MOS device.

The increase in the power loss density with the decrease in the gate lengths with the technology scaling is shown in Fig. 1.3. The active power loss is mainly increased due to the increase in the operating frequency while the subthreshold power loss is increased with the increase in the subthreshold leakage current due to degradation in the threshold voltage with decreased gate lengths. Since high-frequency operation is an utmost requirement for the high-performance ICs, we can optimize the active power loss by reducing the supply voltage. The increase in subthreshold leakage or OFF-state current can also be managed to some extent by reducing the supply voltage.

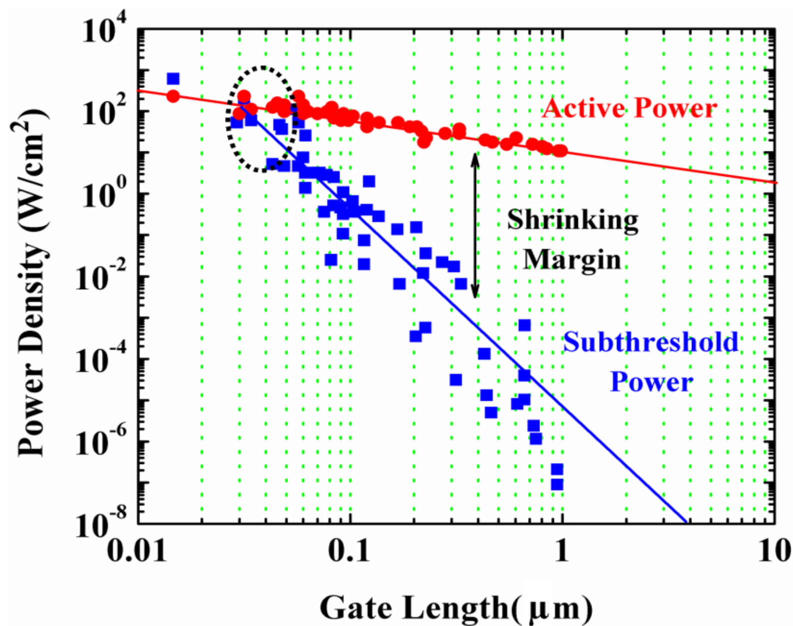

Fig. 1.3: Variation of power density against gate length scaling of MOS device [Meyerson (2004)]

The typical drain current (I_d) versus gate-source voltage (V_{GS}) characteristics of three different MOSFETs of different threshold voltages but with an ideal subthreshold swing (SS) of 60 mV/decade has been shown in Fig. 1.4. The OFF-state current (I_{OFF}) is increased with the decrease in the threshold voltage due to decreased gate lengths as already discussed in Fig. 1.2. Since the increase in I_{OFF} increases the subthreshold power loss (see Eq.(1.2)) due to decrease in the threshold voltage, we can't use aggressive scaling of the threshold voltage parameter of the MOSFETs. On the other hand, we can't scale MOSFETs with a high threshold voltage since larger threshold voltage (due to larger gate lengths) results in the smaller ON-state drain current (see Fig. 1.4) and hence smaller operating speed of the device [C. C. Hu (2010)]. The subthreshold swing (SS) of the MOSFETs considered in Fig. 1.4 is defined as the minimum gate voltage required to change the drive current of the MOS transistor by one decade. The SS is an important parameter to determine the switching characteristics of the MOSFETs which can be mathematically expressed as [Kumar and Jit (2015a)]:

$$SS = \frac{\partial V_{GS}}{\partial(\log I_d)} = \frac{\partial V_{GS}}{\partial \psi_S}\frac{\partial \psi_S}{\partial(\log I_d)} = \underbrace{\left(1+\frac{C_{Dep}}{C_{ox}}\right)}_{m}\underbrace{\left(V_T \ln 10\right)}_{n} \tag{1.3}$$

where, $V_T = kT/q$ is the thermal voltage, V_{GS} is the gate-to-source voltage; I_d is the drain current; ψ_S is the surface potential; C_{Dep} is the depletion capacitance and C_{ox} is the gate-oxide capacitance of the MOSFET.

It may be noted that $m = (1 + C_{Dep}/C_{ox}) \geq 1$ represents the coupling efficiency of the gate voltage to the channel potential while the value of the factor $n = V_T \ln 10 = 60$ mV/decade at room temperature is associated with the thermal

distribution of mobile charge carriers at room temperature [Kim and Fossum (2001)]. Thus, $SS \geq 60$ mV/decade at room temperature for conventional bulk MOSFETs, is known as the Boltzmann's limit of the SS. It may be mentioned that for ideal switching performance of any device, its SS should be zero. However, the above discussion clearly shows that we can't get the SS below 60 mV/decade.

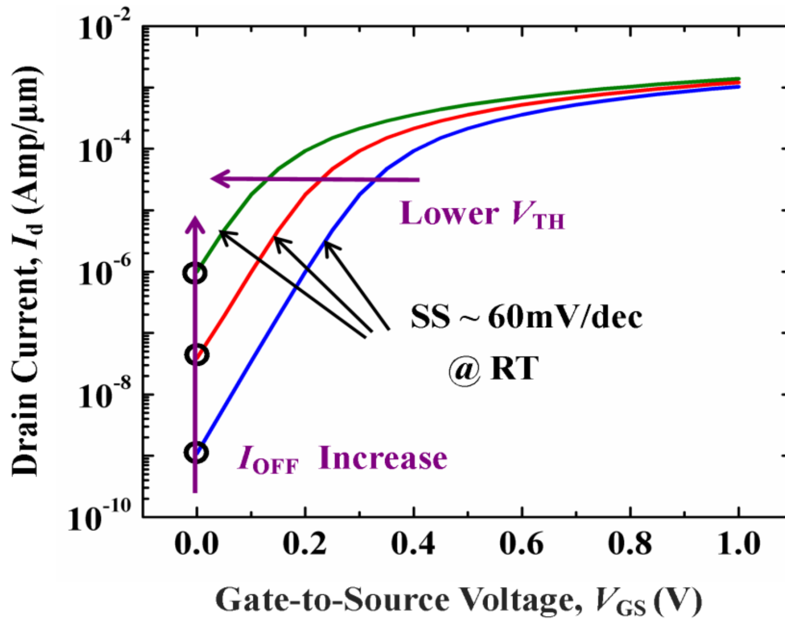

Fig. 1.4: Variation of drain current against gate-to-source voltage of MOS device [Internet resource (IR2)]

1.2 Design Requirements for a New Device

The above discussions clearly show that the decreased gate lengths of the MOSFETs through technology scaling has enabled us to integrate billions of transistors in the ICs at the cost of excessive increase in the static or subthreshold power loss due to the deterioration of the threshold voltage (*i.e.,* the smaller increase in the I_{OFF}). Further, $SS \geq 60$ mV/decade of the conventional bulk MOSFETs at room temperature has also put serious challenge in improving the switching performance of the modern high-speed

CMOS circuits. Thus, it is necessary to think for non-conventional MOSFET structures which can provide lesser degradation in the threshold voltage (*i.e.,* smaller increase in I_{OFF} to lead to smaller P_{Sub}) with the decrease in the gate lengths through scaling. Further, the MOS devices must have the features of achieving $SS < 60$ mV/decade and, high I_{ON}/I_{OFF} as well as $C_g V_{DD}/I_{ON}$ ratios through their structural or materials modifications. The tunnel field effect transistor (TFETs) is such a non-conventional MOS device which has an inherent feature of achieving $SS < 60$ mV/decade [Choi *et al.,* (2007), Boucart and Ionescu (2007), Ionescu and Riel (2011)]. Unlike the conventional bulk MOSFETs (where the current is contributed by the transport of carriers through thermionic emission from the source to the channel formed between source and drain regions by surface inversion), the current in the TFETs is contributed by the tunneling of the carriers from the valence band of the source to conduction band of the channel. In other words, the source-channel junction behaves as the p-n junction of a tunnel diode. By exploring the negative gate capacitance concept [Salahuddin and Datta (2008), Kumar and Jit (2015a), Kumar and Jit (2015b)], the SS of such type of MOS devices can be designed for $SS < 60$ mV/decade by making $m = (1 + C_{Dep}/C_{ox}) < 1$ (see Eq.(1.3)). The present thesis has been developed to theoretically investigate the electrical performance optimization of some novel gate-structure and channel material engineered TFETs.

1.3 Introduction to Tunnel Field Effect Transistor (TFET)

Tunnel field effect transistor (TFET), also known as “Green Transistor” [Hu (2008)], is a good potential candidate to replace the conventional MOSFETs for achieving a very low subthreshold swing (SS) much below the Boltzmann limit of 60mV/decade, the

minimum achievable limit of SS for the conventional MOS transistors [Choi *et al.,* (2007), Boucart and Ionescu (2007c), Nagavarapu *et al.*., (2008), Kumar and Jit (2015a)]. Further, the device has extremely low OFF-current which may make it a better option for the low-power VLSI applications than the conventional MOSFETs [Bhuwalka *et al.,* (2005)]. However, the major drawbacks of the TFETs are its low ON-state current and ambipolarity in current conduction nature due to the band-to-band tunneling based carrier transport from the source to channel in the device [Bhuwalka *et al*. (2005), Boucart and Ionescu (2007a)].

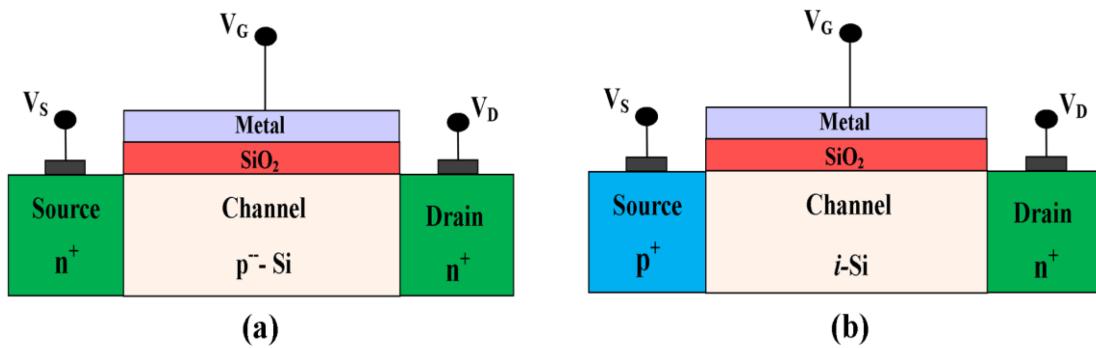

Fig. 1.5: 2-D cross-sectional view of an n-channel (a) MOS device and (b) TFET

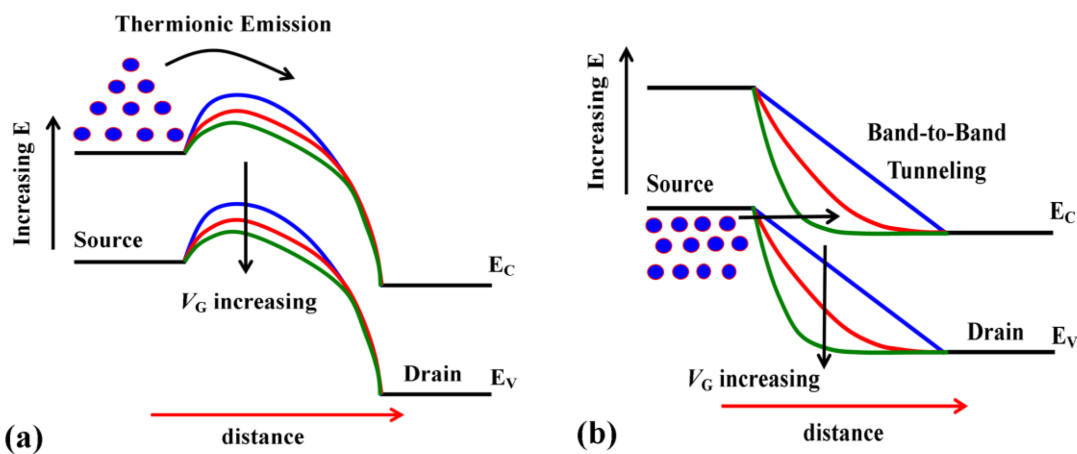

Fig. 1.6: The current mechanism of (a) MOS device and (b) Tunnel FET [Kim (2012)]

The schematic structures of the basic n-channel MOSFET and TFET are shown in Fig. 1.5(a) and (b) respectively. The basic structural difference between n-MOSFET and n-TFET is the use of a lateral n^+-p^--n^+ transistor for source-channel-drain regions in the MOSFETs while a p^+-i-n^+ diode structure is used in the TFET device. The current conduction mechanism of TFETs are entirely different from the conventional MOSFETs. The basic carrier transport mechanisms of the MOSFETs and TFETs can be understood from Figures 1.6(a) and (b) respectively. Figure 1.6(a) shows the energy band diagram of the lateral n^+-p^--n^+ transistor structure of the MOS device shown in Fig.1.5(a) whereas Fig. 1.6(b) shows the energy diagram of the p^+-i-n^+ structure of the TFET device considered in Fig.1.5 (b). In the conventional MOSFETs, the energy barrier at the source-channel junction is required to be reduced by applying a gate voltage to enhance the number of carriers entering from the source into the channel region by the thermionic emission mechanism. However, in the case of TFET device, the gate voltage is applied to create a condition for carrier tunneling the valence band of the source to vacant energy states of the conduction band of the channel region by reducing tunneling energy barrier at the source-channel junction. The two different carrier transport mechanisms result in a much larger drain current (I_{ON} ~ mA/µm & I_{OFF} ~ nA/µm) of the conventional MOSFETs than that of the TFETs (I_{ON} ~ µA/µm & I_{OFF} ~ fA/µm) [Taur and Ning (1998), Seabaugh *et al.* (2010)]. A brief detail of the working principle of the TFETs can be described in the following subsection.

1.3.1 Working Principle of a TFET

As shown in Fig. 1.7, n-channel TFET is nothing but a gated p-i-n diode in which the drain current is resulted from the tunneling of carriers from the source to channel controlled by the applied bias voltage to the gate electrode placed over the intrinsic (*i.e.,*

i-region) of the device [Kane (1960), Sze (1981), Banerjee *et al.,* (1987)]. In case of n-type TFETs, the source, channel and drain are heavily doped p^+, intrinsic or lightly doped p^- and heavily n^+ regions respectively as shown in Fig.1.7(a). On the other hand, in p-type TFETs, the source, channel and drain are heavily doped n^+, intrinsic or lightly doped p^- and heavily p^+ regions respectively as shown in Fig. 1.7(b). The tunneling phenomenon in the p-i-n diode was first proposed by Clarence Melvin Zener in 1934. For both the n-channel MOSFETs and TFETs, positive bias voltage are applied to the gate and drain terminals to make the channel-drain junction reverse biased in both the devices. However, the source-channel junction is forward biased in MOSFETs while it is reverse biased with respect to the source in case of TFET device.

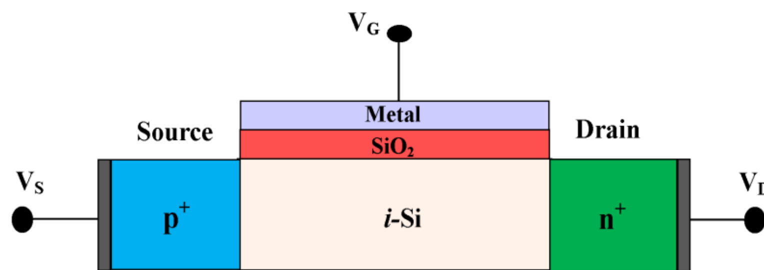

Fig. 1.7 (a): Conventional structure of n-TFET device

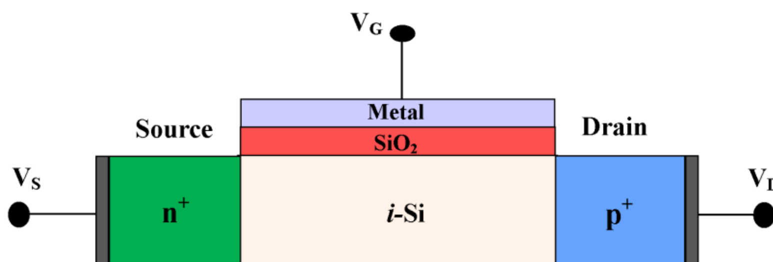

Fig. 1.7 (b): Conventional structure of p-TFET device

The basic working principle of the conventional n-TFET device of Fig. 1.7(a) can be explained by the energy band diagrams of the p-i-n diode under the OFF-state (*i.e.,* with negligible drain current) and ON-state (*i.e.,* with a significant drain current) conditions of the device shown in Fig. 1.8(a) and (b) respectively. In OFF-state condition, the gate and source terminals are kept grounded while the positive voltage is applied to the drain terminal of the device. Under this bias condition of the TFET, tunneling barrier width is thicker and electrons in the valence band of the source do not find empty states in the conduction band. As a result, no electrons can tunnel from the valance band of the source to the conduction band of the channel region to result in a significant amount of drain current in the device. In the OFF-state, the drain current is extremely low, in the order of femto ampere (fA) range. However, when a positive gate voltage is applied, the energy tunneling barrier width is decreased due to the reverse source/channel junction. In this case, valance band of the source is aligned with the conduction band of the channel region so that valance band electrons of the source can easily tunnel to channel region to result in a significant amount of drive current. This condition is called the ON-state of the TFETs. Thus, the operating principle of TFET is based on the modulation of the tunneling barrier width due to the applying the gate bias voltage. Figure 1.9 shows the typical variation of tunneling energy barrier width with the gate voltage of a typical TFET device. The energy barrier width has been extracted from the simulated energy band diagram shown in the inset of Fig. 1.9 by the narrowest tunneling width concept [Boucart and Ionescu (2007c)]. It is observed from the figure that the tunneling barrier width is decreased with the increase in the gate voltage for the relevant TFET operation.

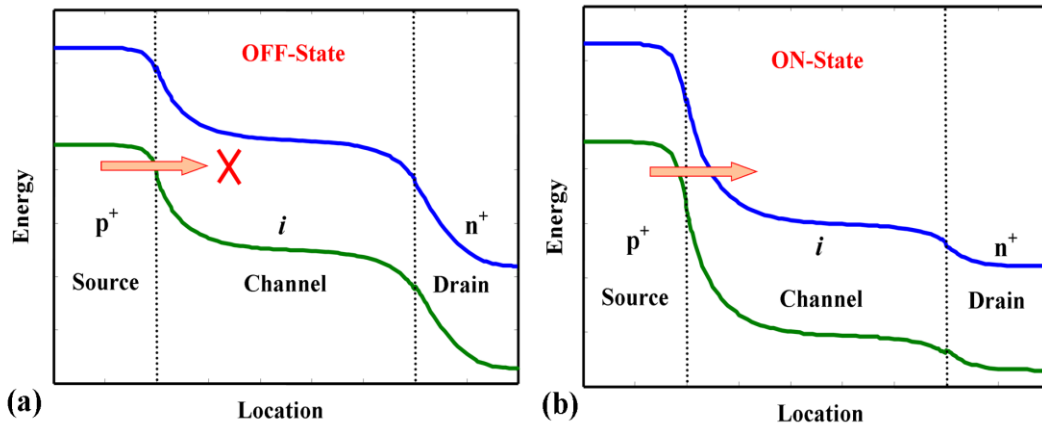

Fig. 1.8: Energy band diagram of typical Tunnel FET device (a) OFF-state (b) ON-state

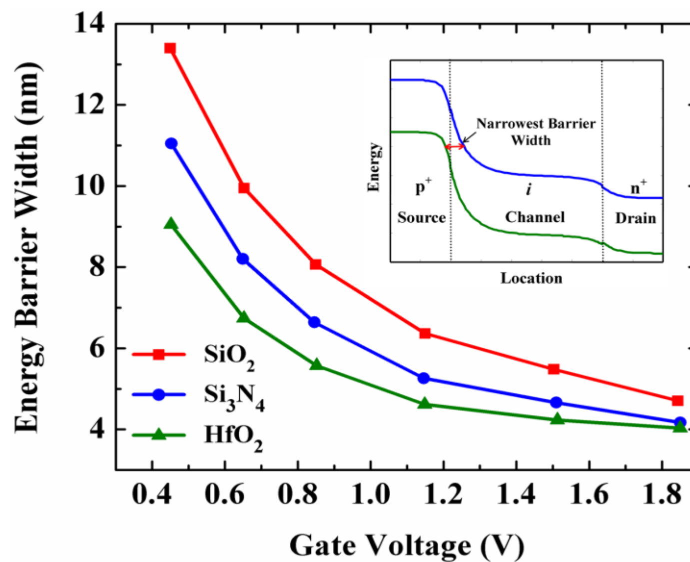

Fig. 1.9: Variation of energy barrier width against gate voltage of typical Tunnel FET Boucart and Ionescu (2007c)]

1.3.2 Basic Expression for Band-to-Band Tunneling Current in the TFETs

It is clear from the above discussions that the drain current in the TFET results from the band-to-band tunneling (BTBT), which is a quantum-mechanical phenomenon for transporting charge carriers from the valance band of the source to conduction band of the channel through the energy band gap existing at the source/channel junction. If the energy barrier is thick enough to prevent the quantum tunneling of the carriers, we say that the device is under the OFF state. The ON-state energy band diagram and corresponding triangular potential barrier for a typical TFET are shown in Fig. 1.10(a) and (b) [Boucart and Ionescu (2007c)].

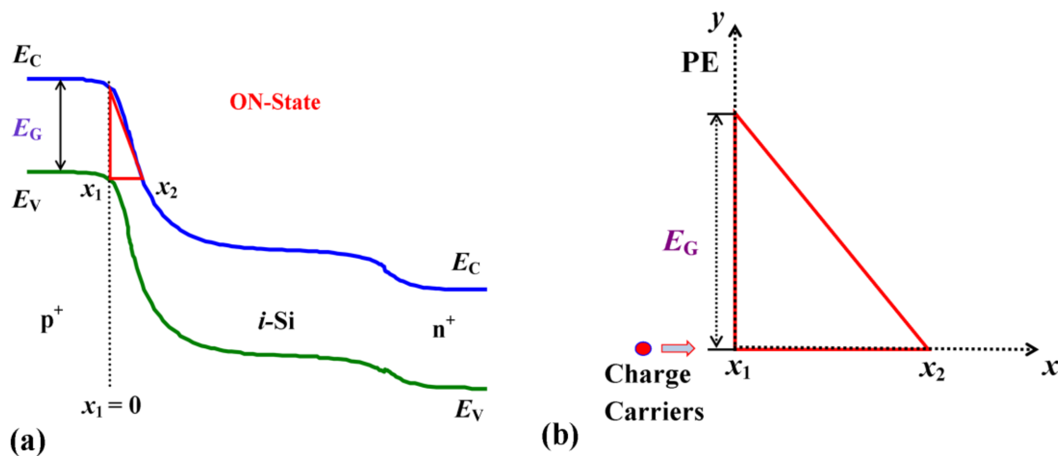

Fig. 1.10: (a) The ON-state energy band diagram and, (b) its corresponding triangular potential barrier for typical Tunnel FET

Figure 1.10(a) shows that the charge carriers can tunnel from x_1 point to x_2 through a triangular energy barrier shown in Fig. 1.10(b). The probability of tunneling (T_P) of the charge carriers through an energy barrier of finite height and width can be obtained from the Wentzel-Kramers- Brillouin (WKB) approximation technique as [Kane (1960), Sze (1981)]:

$$T_p \approx \exp\left[-2\int_{x_1}^{x_2} |k(x)|dx\right] \tag{1.4}$$

where, $k(x)$ is the wave vector of the charge carriers inside the barrier; x_1 and x_2 are the classical turning points as shown in Fig. 1.10(a). From the E-k relationship, $k(x)$ can be written as [Sze (1981)]:

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}(PE - E)} \tag{1.5}$$

where, PE and E are the potential energy and the incoming energy of the charge carriers. It is seen from the figure that the potential energy at the coordinate axis x_2 is equal to zero *i.e.,* $E = 0$ and the incoming energy of charge carriers (PE) is replaced by $E_g/2 - qFx$, where F and E_g are the electric field at the tunneling junction and energy band gap of the substrate material respectively. Then, the wave vector can be expressed as [Sze (1981)]:

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}\left(\frac{E_g}{2} - qFx\right)} \tag{1.6}$$

Putting the wave vector in tunneling probability equation (1.4), we get

$$T_p \approx \exp\left[-2\int_{x_1}^{x_2} \sqrt{\frac{2m^*}{\hbar^2}\left(\frac{E_g}{2} - qFx\right)}dx\right] \tag{1.7}$$

which can be further simplified as

$$T_p \approx \exp\left[\frac{4}{3}\frac{\sqrt{2m^*}}{q\varepsilon\hbar}\left(\frac{E_g}{2} - qFx\right)^{3/2}\right]_{x_1}^{x_2} \tag{1.8}$$

From the triangular shape of energy barrier shown in Fig. 1.10(b), we can write $(E_g/2 - qFx) = E_g$ and $(E_g/2 - qFx) = 0$ at $x = x_2$. Thus, tunneling probability (T_P) can be written as [Sze (1981), Boucart (2010)]:

$$T_p \approx \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar F}\right) \tag{1.9}$$

Since the band-to-band tunneling current (I_d) is directly proportional to the tunneling probability (*i.e.,* $I_d \propto T_p$), we can write [Kane (1960)]:

$$I_d \propto \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar F}\right) \tag{1.10}$$

Using the Kane's model, Eq.(1.10) can be expressed as [Kane (1960)]:

$$I_d = A_{Kane}F^{\alpha} \exp\left(-\frac{B_{Kane}}{F}\right) \tag{1.11}$$

where, $A_{Kane} = q^3\sqrt{2m^*/E_g}\Big/4\pi^2\hbar^2$, and $B_{Kane} = 4\sqrt{2m^*}E_g^{3/2}\Big/3q\hbar$ are known as the Kane's parameters and "α" is a material dependent constant parameter; q is the elementary charge; m^* is the reduced tunneling mass of the charge carriers; and $\hbar$ is the reduced Planck's constant [Kane (1960), Sze (1981)].

The BTBT phenomenon results in a much lower ON-state current in the TFET than the conventional MOSFETs. The typical transfer characteristics for an ideal switching device, bulk n-MOSFET and n-TFET have been compared in Fig. 1.11. It is clearly observed that while the much smaller OFF-state current of the TFET than that of the MOSFET is an important merit of the device, the smaller drain current of the TFET over the bulk MOSFET is a matter of great concern for their practical switching

applications. Thus, to make the TFET as a potential substitute for high speed switching applications, attempt needs to be made for improving the ON-state current of TFET devices as per ITRS requirement.

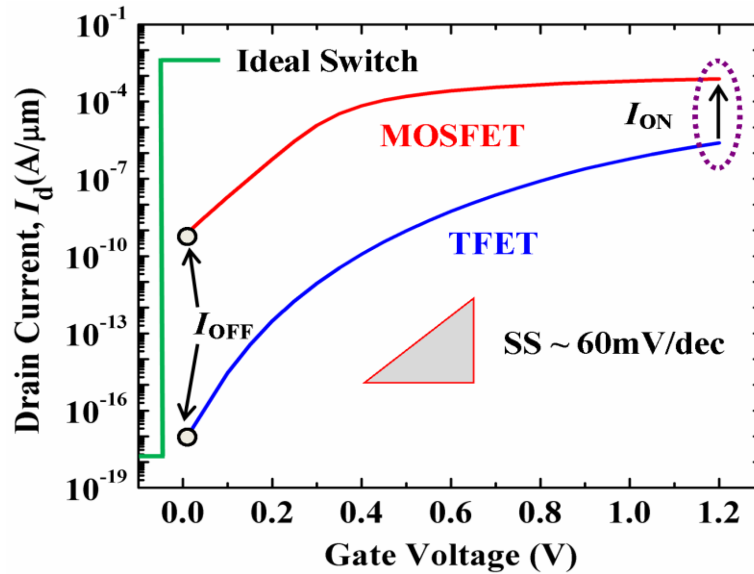

Fig. 1.11: Transfer characteristics for Ideal device, Bulk MOSFET and Tunnel FET [Kim and Fossum (2001)]

1.4 Possible Techniques to Improve the Performance of TFETs

The major drawbacks of the TFET are the low ON-state current and ambipolar conduction mechanisms which makes the TFET difficult for inverter-based logic circuit applications [Khatami and Banerjee (2009), Abdi and Kumar, (2016)]. The poor ON-state current of the device reduces the speed of operation of the logic circuits by affecting the charging and discharging times. The ambipolar conduction in the TFET results in the drain current for both the positive and negative gate voltages which leads to malfunctioning inverter based logic circuits [Salahuddin and Datta (2008), Abdi and Kumar (2016)]. Researchers have explored a number of different techniques such as

gate engineering, channel material engineering and source/drain material engineering for improving the ON-state current and suppressing the ambipolar conduction in the TFETs. The following subsections have been devoted to introduce some of the important techniques for improving the ON current with optimizing ambipolar current characteristics of the TFETs.

1.4.1 Gate Engineering Techniques

The gate engineering techniques are basically the modifications in the gate structure to enhance the ON-state current of the TFETs with minimized ambipolarity effect. Anyone or the combination of more than one of the following gate engineering techniques may be employed for improving the performance of the TFETs.

1.4.1.1 Multi-Gate Structure Engineering

The conventional use of a single gate can be replaced by the multi-gate structure to enhance the ON-state current. The multiple-gate TFET device structures include double-gate TFET [Boucart and Ionescu (2007), Saurabh and Kumar (2011)], Fin-TFETs [Biswas and Ionescu (2014), Hemanjaneyulu and Shrivastava (2015)], tri-gate TFET [Navlakha and Krant (2017)], quadruple gate TFETs [Sharma and Vishvakarma (2013)], and gate-all-around (GAA)/cylindrical Gate TFETs [Narang *et al.* (2013), Xu *et al.* (2015)]. Among the above, the double-gate (DG) TFETs are the most widely explored Tunnel FET structure for future generation IC technology. It can be a planar or vertical depending upon the way of tunneling the charge carriers from the source to the channel through the gate region [Saurabh and Kumar (2011), Agrawal *et al*. (2015)]. In DG planar TFET structure, the tunneling is controlled by the gate electrodes placed

on the top and bottom sides of the channel as shown in Fig. 1.12(a) [Boucart and Ionescu (2007c), Ionescu and Riel (2011)]. On the other hand, the tunneling rate is controlled by the left and right sides of the channel in the vertical DG TFET structure as shown in Fig. 1.12(b). Here the control of tunneling is exerted by the vertical gates on the source/channel junction from the lateral sides of the device. The vertical DG TFET is also known as DG Fin-TFET structure [Biswas and Ionescu (2014), Hemanjaneyulu and Shrivastava (2015)]. The large thickness of the dielectric placed under the top gate of the channel in Fig. 1.12(b) is used to make the effect of the top gate negligible on the tunneling of carriers from the source to the channel thereby making the device effectively a double-gate structure.

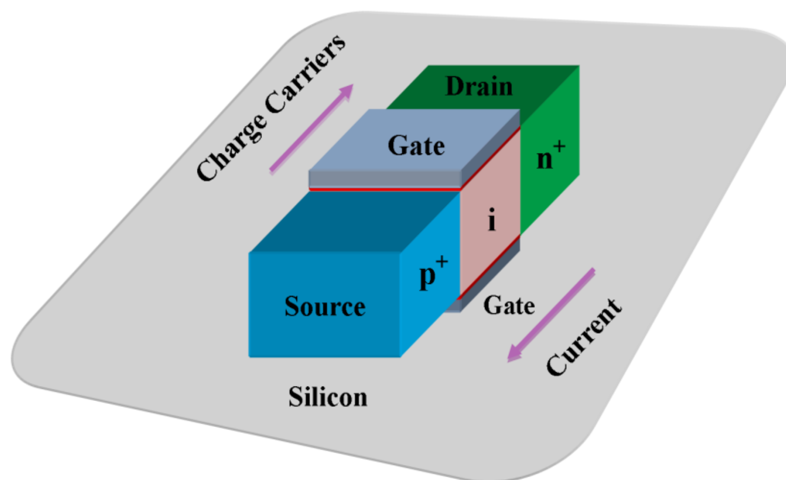

Fig. 1.12(a): Planar Double-Gate Tunnel FET Structure

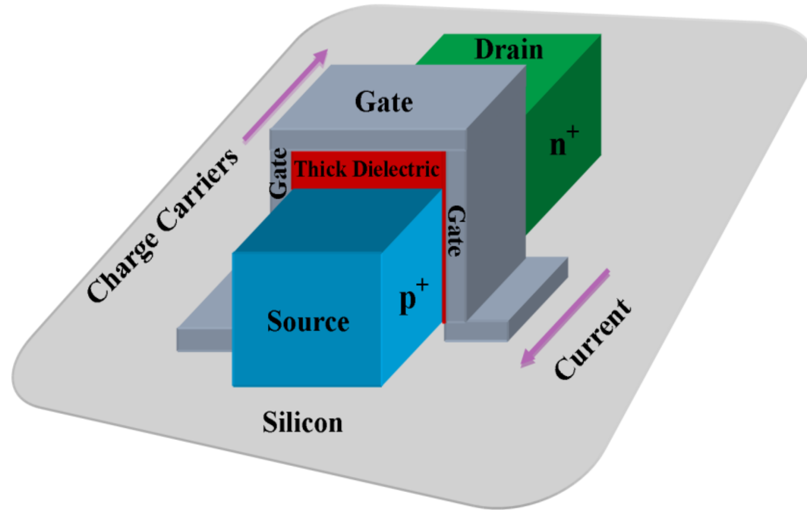

Fig. 1.12(b): FinFET (Double-Gate) Tunnel FET Structure

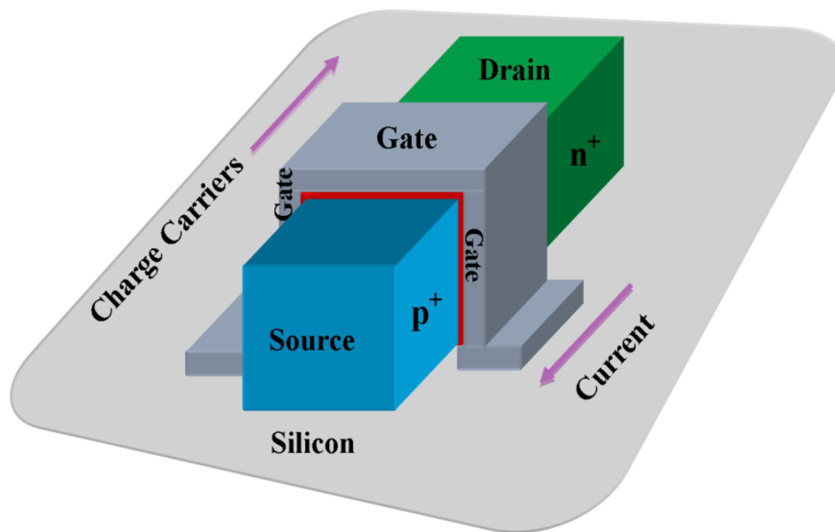

Fig. 1.12(c): Tri-gate Tunnel FET Structure

The tri-gate TFET configuration can be achieved by simply replacing the thick dielectric by a thin dielectric in Fig. 1.12(b) as shown in Fig. 1.12(c) [Navlakha and Krant (2017)]. In other words, in addition to the vertical two gate, the top gate is also used to control the tunneling mechanism in the tri-gate TFET structure. The quadruple-gate TFET structure is shown in Fig.1.12(d) to introduce the gate control from all sides of the channel [Sharma and Vishvakarma (2013)]. Figure 1.12 (d) shows the cylindrical TFET structure [Appenzeller *et al.* (2004), Appenzeller *et al.* (2005), Rakhi Narang *et al.* (2013), Wanjie Xu *et al*. (2017)] in which the gate electrode is wrapped around the channel region to exhibit excellent control of the gate on the tunneling in the device. The cylindrical gate TFET structure is expected to have better scalability with higher ON current, better I_{ON}/I_{OFF} current ratio and steeper SS over other multi-gate TFET structures [Rakhi Narang *et al*. (2013)]. However, the fabrication complexities of such non-planner TFET structures are the major limitation for the large-scale IC applications.

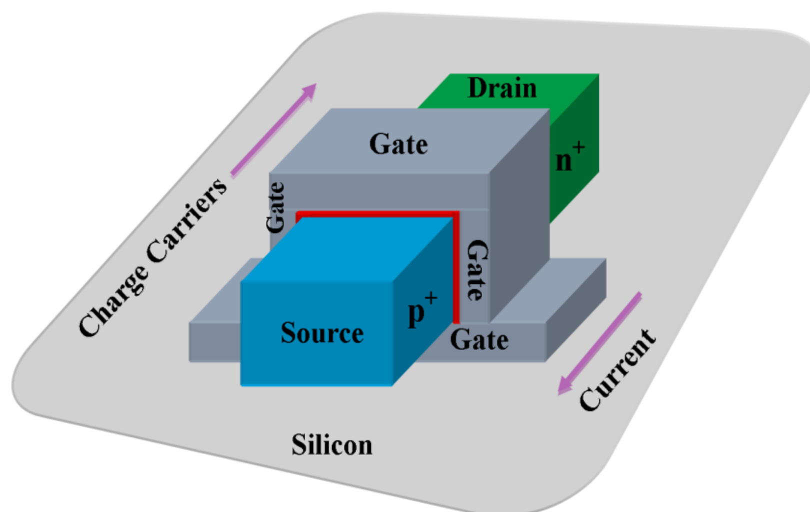

Fig. 1.12(d): Quadruple Gate Tunnel FET Structure

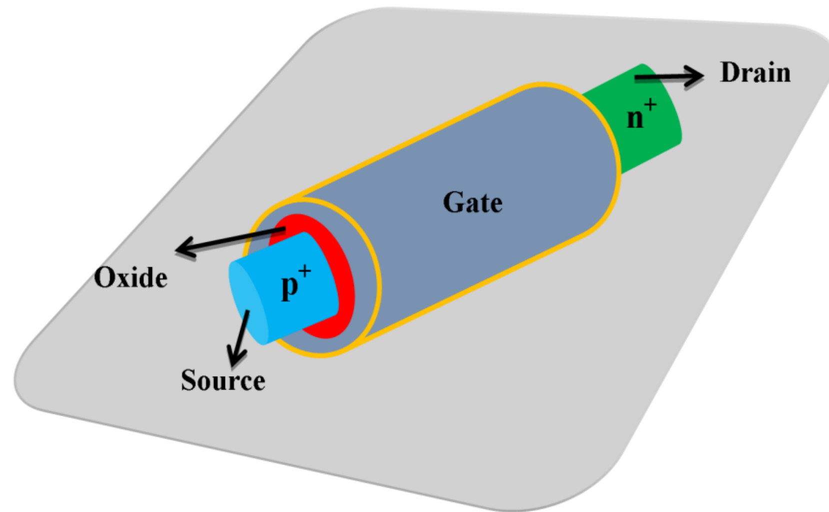

Fig. 1.12(e): Cylindrical Gate Tunnel FET Structure

1.4.1.2 Gate-Electrode Engineering

The main objective of using the gate-electrode engineering technique is to tune the channel electric-field profile in such a manner that it becomes very large at the source/channel junction to accelerate the tunneling probability of charge carriers towards the channel while maintaining a very small electric at the drain/channel junction to minimize the ambipolar conduction in the TFET device [Jain *et al.* (2015), Navjeet Bagga *et al*. (2016), Prabhat and Dutta (2016), Gracia *et al.* (2017)]. This can be achieved by replacing the single work-function based metal gate-electrode in conventional TFETs by the non-overlapped cascade connection of more than one metal-like materials with different work functions in the ascending order of their work functions starting from the source to the drain side so that the material with the lowest

work function exists at the source side while the material with the highest work function is placed at the drain side to form the resultant gate electrode contact of the TFETs [Saurabh and Kumar (2011), Safa *et al*. (2017)]. The material with the lowest work function placed at the source side is called the tunneling gate while the material with the largest work function at the drain side is called the auxiliary gate of the TFET device [Saurabh and Kumar (2011)]. The 2-D cross-sectional view of dual-material-gate (DMG) and triple-material-gate (TMG) based TFET structures have been shown in Fig. 1.13 and 1.14 respectively.

In principle, any number of metal-like materials can be used for forming the gate-electrode contact in the TFETs. The triple-material-gate (TMG) based-DG TFET shown in Fig. 1.14 has been investigated to achieve improved performance of the TFET [Navjeet Bagga *et al*. (2016)]. It has been demonstrated that the TMG DG TFET structure provides larger ON-state current with reduced ambipolar conduction than the convention DG TFET structures. However, the major limitation is involved in fabricating multiple metal-like materials over nano-scale gate-length region to form the gate-electrode contact in the device. In this point of view, the dual-material gate (DMG) is the simplest gate-electrode material engineered TFET structure which can be obtained by placing only two different gate-electrode materials in the cascaded and non-overlapped manner to form the gate electrode of the TFET [Zhou (2000), Kumar and Chaudhry (2004), Reddy and Kumar (2005)]. Such type of gate-electrode structure enhances the tunneling rate by creating high electric field at the source/channel junction while reducing the ambipolarity effect by maintaining a low electric field at drain/channel junction [Saurabh and Kumar (2011)].

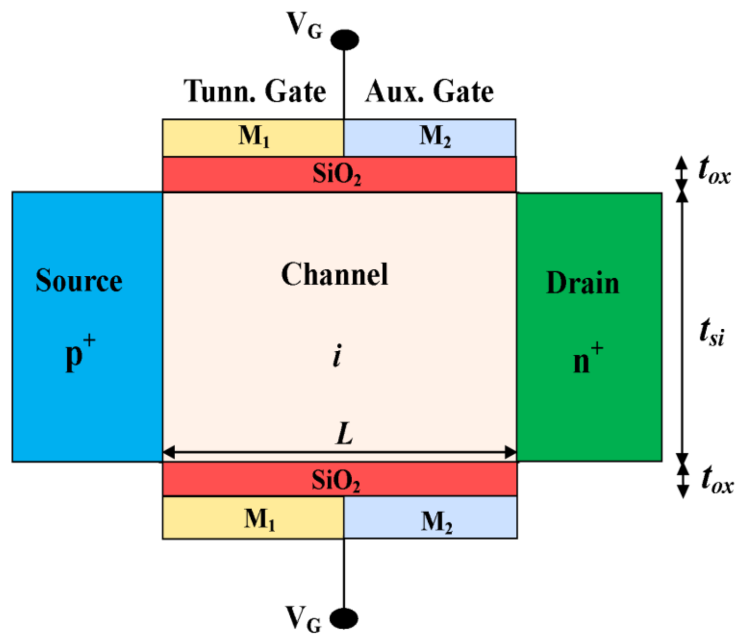

Fig. 1.13: Dual Material Gate Tunnel FET Structure

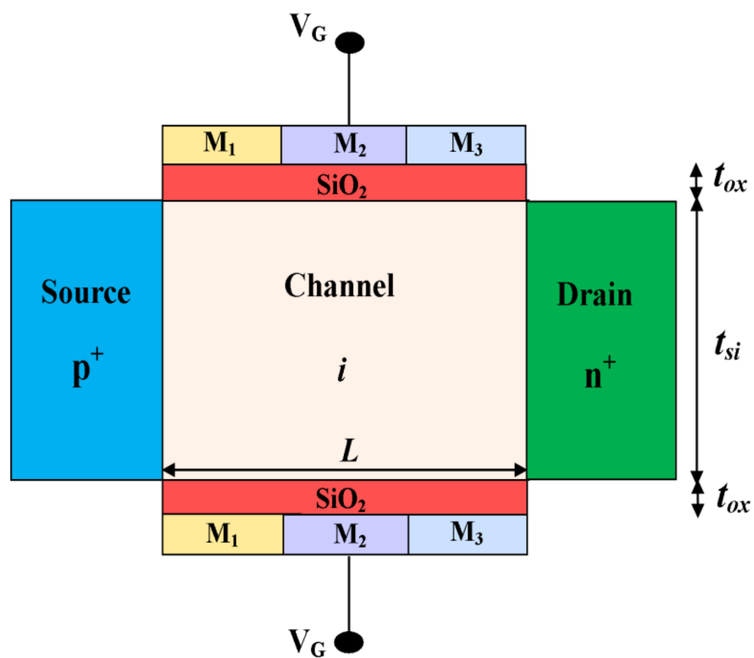

Fig. 1.14: Triple Material Gate Tunnel FET Structure

1.4.1.3 Gate-Oxide Engineering

In gate-oxide engineering technique, the conventional SiO_2 is replaced by a high-*k* dielectric for enhancing the scalability of gate oxide thickness [Boucart and Ionescu (2007c)]. A combination of SiO_2 and high-*k* dielectric in the form of either a vertical or a lateral stacked gate-oxide structure [Choi and Lee (2010)] can also be explored as demonstrated in Fig. 1.15 and Fig.1.16 respectively. In vertically stacked gate structures, the high-*k* is normally placed over the SiO_2 to form the effective gate-oxide structure while in the lateral configuration, the cascade of SiO_2 and high-*k* (*e.g.,* HfO_2) is used to form the resultant gate-oxide in TFETs. The basic idea behind using a high-*k* gate oxide is to enhance the drive current of the device without disturbing the leakage current [Choi and Lee (2010), Wang *et al.* (2016), Choi and Lee (2016), and Gracia *et al*. (2017)]. Based on the simulation study, Choi and Lee [Choi and Lee (2010)] have reported the gate-oxide engineering technique in the form of the hetero dielectric gate based DG TFET structure to demonstrate its higher ON-current, steeper SS and smaller ambipolar behavior than the conventional DG TFET structures. Jain *et al.* [Jain *et al.* (2015)] have reported the application of gate-oxide engineering technique in the DG TFET to show a significant improvement in the switching characteristics (*i.e.,* $I_{ON}/I_{OFF} \sim 10^9$) and average SS over the single-dielectric based-DG TFETs. Wang *et al.* [Wang *et al.* (2016)] have proposed the application of hetero-gate-dielectric (HGD) on DG TFET with source pocket to demonstrate the enhancement in the ON-current with suppressed ambipolar conduction in the device.

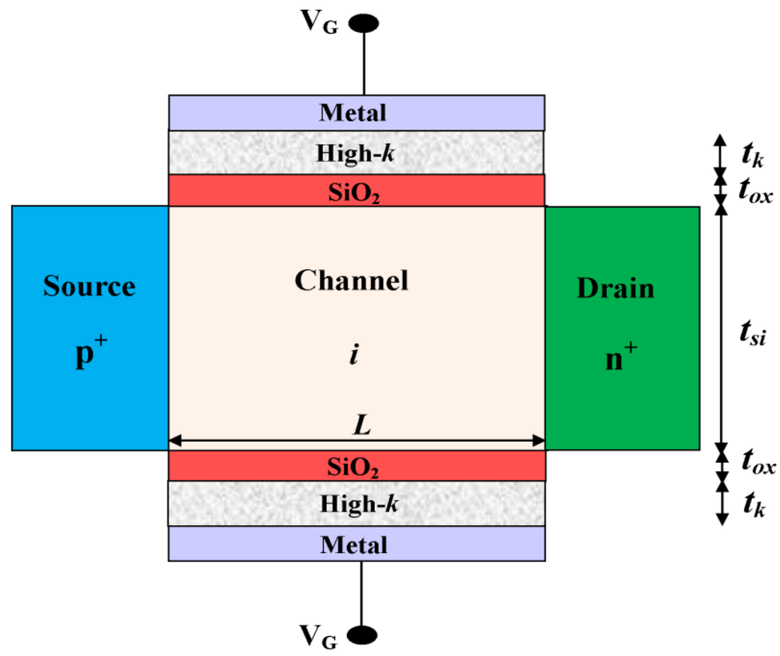

Fig. 1.15: Vertical Stacked Gate SiO_2/high-*k* DG TFET Structure

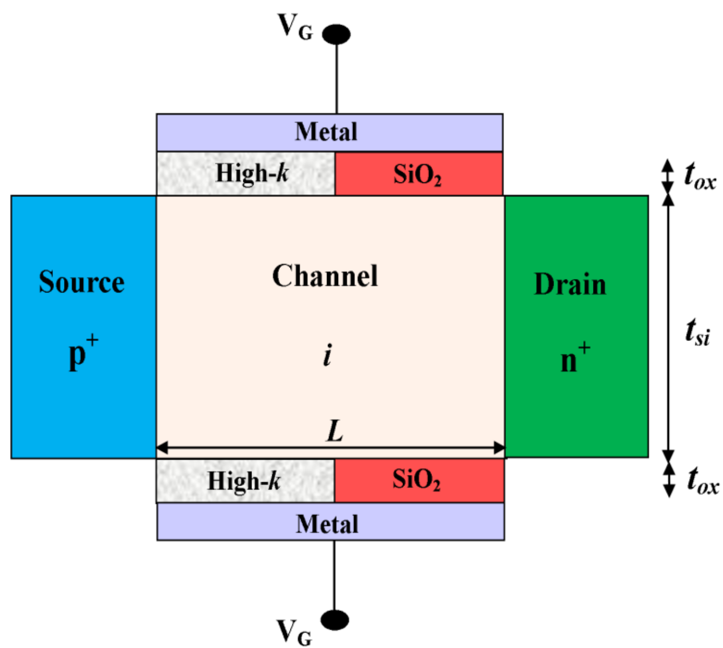

Fig. 1.16: Lateral Stacked Gate SiO_2/high-*k* DG TFET Structure

1.4.2 Materials Engineering Techniques

In this technique, either Si in conventional TFET is completely replaced by a different material in the TFETs or the replacement of Si from any one or more than one of the source, drain and channel regions of the device by another material to enhance the ON-state current and minimize the ambipolarity effect. The TFETs using a single material for its source, channel and drain regions are called homojunction based-TFET device. However, when two different materials are used for the source and channel regions of the TFETs, they are called heterojunction based-TFET device. The heterojunction TFETs is always superior to homojunction TFETs in terms of higher drive current, better switching performance and lower SS [Michael Graef *et al.* (2014), Chander and Baishya (2015), Chander and Baishya (2016)] due to the increase in the BTBT probability resulted from the decrease in the effective energy band gap at the tunnel junction of the device. Thus, materials engineering techniques may include any one or the combination of more than one of the following material replacement techniques explored in the TFETs.

1.4.2.1 Source Materials Engineering

The source materials engineering techniques can be used for improving the drive current and subthreshold swing characteristics of the device. In this technique, the source region of the TFET uses a low band gap material such as Ge and InAs while the channel and drain regions are of Si material to form a heterojunction based source/channel junction [Michael Graef *et al.* (2014), Chander and Baishya (2015), Ahish *et al*. (2016), Dong *et al.* (2016), Ahish *et al*. (2016)]. The schematic of a Ge(source)/Si (channel) heterojunction based DG TFET structure is shown in Fig.1.17.

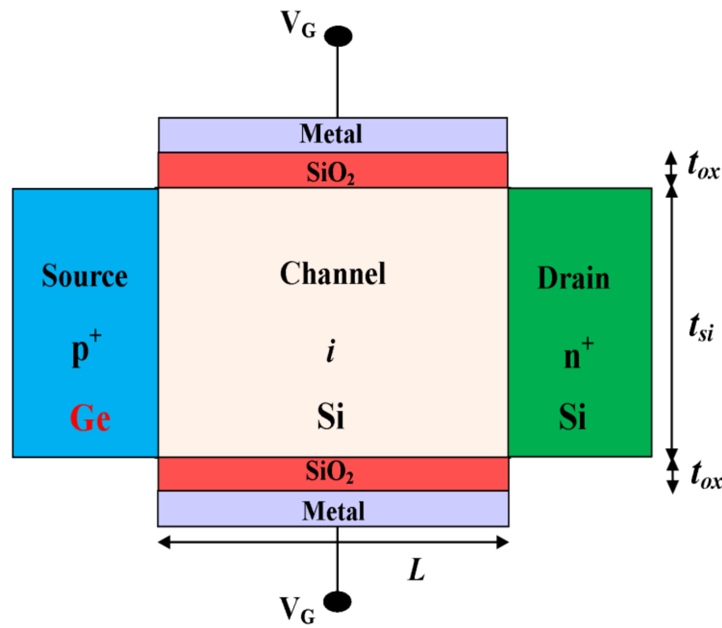

Fig. 1.17: Heterojunction Ge/Si DG TFET Structure

Other source/channel heterojunctions such as InGaAs/GaAsP [Ahish *et al.* (2017)], InGaAs/InP [Dong *et al.* (2016)], and GaAsSb/InGaAs [Guan *et al.* (2017)] have also been reported in the literature. In general, such type of source material engineering provides better analog/RF performance in addition to improving the ON-state current with optimized ambipolar current of the TFETs [Krishnamohan *et al*. (2008)].

1.4.2.2 Channel Materials Engineering

In this technique, the conventional Si-based channel is replaced by the strained-silicon material in the TFETs to enhance the ON current and hence the speed of operation of the TFET by enhancing the mobility of the channel carriers of the device. Figure 1.18 demonstrates the systemic picture of a strained-Si channel based-DG TFET structure.

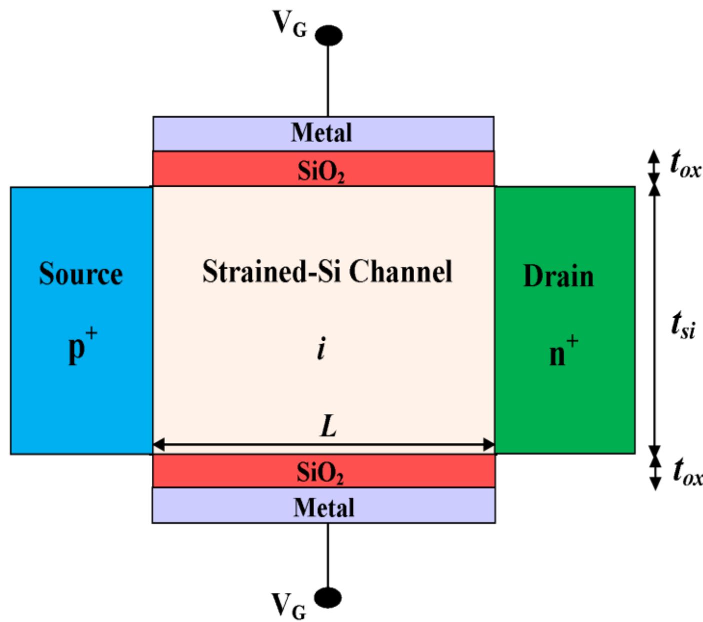

Fig. 1.18: Strained-Si channel based DG TFET structure

A working strained-Si based n-channel TFET was first reported by Krishnamohan *et al.* [Krishnamohan *et al.* (2008)] to demonstrate a record high drive current of $I_d \sim 300\,\mu\text{A}/\mu\text{m}$ with a $SS \sim 50\,\text{mV/dec}$. Nayfeh *et al.* [Nayfeh *et al.* (2009)] have demonstrated experimentally that the switching characteristics of TFETs can be dramatically improved by using a $\text{Si}-\text{Si}_{1-x}\text{Ge}_x-\text{Si}$ based-TFET. They [Nayfeh *et al.* (2009)] have found an improvement in the ON-current by 10^5 times over the conventional Si TFETs. Based on the simulation study, Saurabh and Kumar [Saurabh and Kumar (2011)] have observed significant improvement in the switching characteristics of the stained-Si channel based DG TFET.

1.4.2.3 Low Band-Gap Materials Engineering

The tunneling probability of charge carriers in the TFETs is inversely proportional to energy band gap of the substrate materials [Luisier and Klimeck (2009), Kao *et al.* (2012)]. Clearly, higher BTBT rate can be achieved by a using lower band gap material (*e.g.,* Ge, InAs etc.) than Si in the TFETs. Figure 1.18 illustrates the systemic picture of a low-band gap materials based-DG TFET structure.

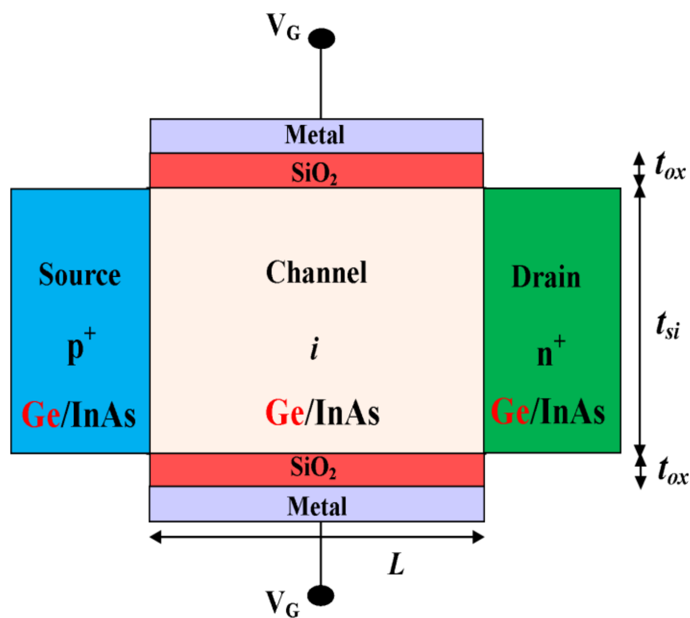

Fig. 1.19: Low-band gap materials based DG TFET structure

The lower band gap materials than the Si in TFETs can provide improved drive current and frequency characteristics of the device [Gopi and Chauhan (2016)]. The enhancement in the analog/RF performances such as the transconductance, intrinsic gain, total gate capacitance and unity gain cut-off frequency in the InAs-based TFETs have been reported in the literature [Anand and Sarin (2016), Mohan Biswal *et al.* (2016)]. However, the major drawback of such TFETs is its increased the leakage current (*i.e.,* OFF-current) at the benefit of the improved ON-current and analog/RF performances.

1.5 Review of Some State-of-the-Art Research Works on TFETs

The first TFET as a gated p-i-n diode structure was fabricated by Quinn *et al.* [Quinn *et al.* (1978)] at the Brown University in 1978. Banerjee *et al*. [Banerjee *et al.* (1987)] reported a closed-form analytical model for the drive current of three-terminal tunnel device by using a p-region instead of an *i*-region under the gate. In this direction, Toshio Baba [Baba (1992)] fabricated the surface tunnel transistors (STT) by using molecular beam epitaxy (MBE) technique to mesa structures. At the Cambridge University, Reddick and Amaratungaa [Reddick and Amaratungaa (1995)] proposed an experimental study of silicon surface tunnel transistor (STT) working on the principle of band-to-band tunneling phenomenon. The proposed STT device was reported to have no punch-through related limitations and hence was considered as improved version of the existing FETs. The STT has been using as a high-frequency gate controlled detector and oscillator in a conventional Si integrated circuits. Kogaa and Toriumi [Kogaa and Toriumi (1996)] reported a three-terminal Si tunneling device based on negative differential conductance in which the drive current was mostly controlled by the applied gate bias.

For the first time, Hansch *et al.* [Hansch *et al.* (2000)] fabricated a vertical Esaki tunneling transistor using abrupt doping by MBE technique and illustrated the saturation behavior of the transfer characteristics of the device. Aydin *et al.* [Aydin *et al.* (2004)] fabricated a lateral interband tunneling transistor on a SOI substrate using heavily doped source and drain regions. Appenzeller *et al.* [Appenzeller *et al.* (2004)] fabricated a carbon nanotube based TFET with a dual gate (*i.e.,* a back and top gate) structure and demonstrated that the band-to-band tunneling (BTBT) of the charge carriers from the valence band of the source into the conduction band of the channel could be enabled or

disabled by changing the applied gate bias of the device. In the same year, Wang *et al.* [Wang *et al.* (2004)] fabricated a complementary Si-TFET structure with ultra-low leakage currents by using a reverse biased p-i-n diode structure. Bhuwalka *et al.* [Bhuwalka *et al.* (2004)] of German Federal Armed Forces University fabricated a vertical Si-TFET with a SiGe delta layer at the source junction grown by MBE technique. They demonstrated that the ON-current could be improved drastically by the SiGe delta layer used for reducing the tunnel barrier width of the device.

Based on both the experimental and simulation studies, Nirschl *et al.* [Nirschl *et al.* (2006)] investigated scaling properties of TFETs with 65nm, 90 nm, and 130 nm gate lengths and observed much smaller static leakage current and smaller short-channel effects (SCEs) than the bulk MOSFETs. Verhulst *et al.* [Verhulst *et al.* (2007)] considered the TFETs without using gate-drain overlapping to shorten the gate length of the device and observed a reduced ambipolar effect without affecting the DC performances of the device. Boucart and Ionescu [Boucart and Ionescu (2007a)] simulated a DG TFET for the first time and observed a better performance of the DG structure over the single gate TFET device. They [Boucart and Ionescu (2007a)] obtained a high ON-current of ~0.23mA and a low OFF-current in the range of fAmp with the average and point SS of $SS_{Avg} = 57\text{mV/dec}$ and $SS_{Poi.} = 11\text{mV/dec}$ respectively. In another work, Boucart and Ionescu [Boucart and Ionescu (2007b)] have reported that the scaling limit of the DG TFET with a high-*k* gate oxide has better scalability over the DG TFET with conventional SiO_2 gate oxide without affecting the SS and threshold voltage of the device.

Toh *et al.* [Toh *et al.* (2007)] simulated a DG TFET to demonstrate that majority portion of the drain current is contributed by a strong BTBT phenomenon existing at the surface of the device. Based on the experimental as well as theoretical investigations, Nagavarapu *et al.* [Nagavarapu *et al.* (2008)] observed that the SOI-based PNPN TFET structures possess higher ON-current, I_{ON}/I_{OFF} current ratio, and smaller SS over the conventional SOI-TFET structures. Krishnamohan *et al.* [Krishnamohan *et al.* (2008)] have reported a record high ON current in the order of ~ 300μA/μm with a low SS in the order of ~50mV/dec in the stained-Ge based DG TFET structures. They [Krishnamohan *et al.* (2008)] have also illustrated that the lateral heterostructure is the most effective approach to reduce the ambipolar conduction in the TFETs.

Schlosser *et al.* [Schlosser *et al.* (2009)] reported that the fringing field effects in high-*k* dielectric oxide based TFETs could lead to a much higher ON-current and a steeper SS below the Boltzmann limit of 60 mV/decade over the conventional MOS devices. Sandow *et al.* [Sandow *et al.* (2009)] fabricated an ultra-thin body SOI TFETs and observed that the electrical characteristics was independent of the channel length but was found to have a strong dependence on the source/drain doping concentration and gate oxide thickness of the device. Kazazis *et al.* [Kazazis *et al.* (2009)] reported the fabrication and electrical characterization of Ge-on-insulator (GOI) TFETs with heavily p^+ doped source and n^+ doped drain regions. They [Kazazis *et al.* (2009)] observed a smaller ambipolar conduction, higher ON current and reasonable I_{ON}/I_{OFF} current ratio over the conventional SOI-based TFET structures. Agopian *et al.* [Agopian *et al.* (2013)] have experimentally investigated the analog performances of Trigate p-TFET. They have observed higher intrinsic voltage gain of p-TFET devices than that of the p-FinFETs due to high output conductance at same bias conditions.

1.5.1 Review of Some Simulation-Based Studies on TFETs

In this subsection, we will review some selected simulation-based studies on the TFETs. In this regard, Saurabh and Kumar [Saurabh and Kumar (2009)] have simulated a strained-Si based DG TFET to show the device structure has inherent capability to provide better reliability by minimizing the effect of process-induced variations on the ON-current, threshold voltage, and SS characteristics of the TFETs. Choi and Lee [Choi and Lee (2010)] have simulated a hetero dielectric gate (HfO_2/SiO_2) DG TFET to demonstrate its higher ON-current, steeper subthreshold swing and smaller ambipolar effects over conventional DG TFETs. In another report, Saurabh and Kumar [Saurabh and Kumar (2011)] have simulated a dual-material-gate (DMG) DG TFET to demonstrate a drastic improvement in the ON-current, transfer characteristics and SS of the device over the conventional DG TFETs. A non-local BTBT algorithm has been proposed by Shen *et al.* [Shen *et al.* (2011)] for accurate calculation of the drain current of any TFET using any TCAD simulator. Jain *et al.* [Jain *et al.* (2015)] have carried out the 2-D simulation for the surface potential, electric field, and drain current of dual-materials hetero-dielectric DG TFET. They [Jain *et al.* (2015)] have reported higher I_{ON}/I_{OFF} current ratio (~2×10^9) and better SS (48mV/dec) of the dual-materials hetero-dielectric DG TFET over the conventional DG TFETs. Based on 3-D simulation of Fin-TFET, Hemanjaneyulu and Shrivastava [Hemanjaneyulu and Shrivastava (2015)] have observed that the Fin-TFET with 10-nm gate length has higher ON-current, reduced OFF-current, enhanced transconductance, lower output resistance, higher unity gain frequency than the conventional vertical TFET structures. Ahish *et al.* [Ahish *et al.* (2016)] have investigated the impact of drain doping profile on the transconductance, parasitic capacitances, cut-off frequency, gain bandwidth product) and circuit

performance of InAs/Si heterojunction DG TFET. The influence of oxide interface charges on the electrical characteristics of DG TFETs with a source pocket has been investigated by Mishra *et al.* [Mishra *et al.* (2016)]. They have reported that DG TFET structures are relatively less sensitive towards the fixed charges (positive/negative) at the interface as compared the bulk MOSFETs. Gracia *et al.* [Gracia *et al.* (2017)] proposed a simulation-based study for electrical characteristics of dual materials hetero dielectric DG TFET with different materials such as Si and Ge. They [Gracia *et al.* (2017)] have observed that Ge based DG TFETs have higher drive current and smaller SS than the conventional Si-based DG TFETs.

1.5.2 Review of Some Analytical Models of TFETs

After investigating some selected literature related the TCAD simulation based studies on TFETs, we will now survey some important literatures on the analytical modeling of TFETs. The 2-D analytical modeling of surface potential and electric field of symmetric and asymmetric DG TFETs without considering the accumulation/inversion charges in the channel region have been reported by Yadav *et al.* [Yadav *et al.* (2011)]. Zhang *et al.* [Zhang *et al.* (2012)] have proposed a 2-D analytical charge-based model for the electrical characteristics of DG TFETs by including the effects of source depletion region as well as mobile charges in the channel region. They [Zhang *et al.* (2012)] have concluded that the DG TFET can be viewed as the series combination of a gated tunnel diode and a DG MOSFET. The quantum confinement effects on the subthreshold swing and threshold voltage of DG TFETs have been analytically investigated by Padilla *et al.* [Padilla *et al.* (2012)]. Narang *et al.* [Narang *et al.* (2013)] have modelled surface potential, electric field and drain current of a gate-all-around (GAA) p-n-p-n TFET by including the effect of drain voltage and source/drain depletion region. The surface

potential, electric field, and drain current of DG TFETs have modelled by Gholizadeh and Hosseini [Gholizadeh and Hosseini (2014)] by including the effect of mobile charge carriers in the channel. Assuming the DG TFETs as a DG MOSFET in series with the ideal TFET, Zhang and Chan [Zhang and Chan (2014)] have developed the modeling of electrical characteristics of DG TFETs including channel transport for SPICE applications. Graef *et al.* [Graef *et al.* (2014)] have developed a physics-based 2-D analytical model for the BTBT current of heterojunction DG TFET by conformal mapping techniques.

Now we will investigate some recent literatures of last three years. An universal analytical model of InAs based DG TFETs have been proposed by Lu *et al.* [Lu *et al.* (2015)] for circuit simulation applications. The drain current model is shown to be applicable for both the subthreshold to superthreshold regions, and extendable for the broken-gap AlGaSb/InAs DG TFETs [Lu *et al.* (2015)].

The modeling of surface potential, electric field, and drain current of cylindrical gate (CG) TFETs have been proposed by Dash and Mishra [Dash and Mishra (2015a)]. Using the concept of the shortest tunneling path, they [Dash and Mishra (2015a)] have modeled the drive current of CG TFETs. Finally, the threshold voltage model of the device is developed using the maximum transconductance method [Dash and Mishra (2015b)].

Villani *et al.* [Villani *et al.* (2015)] have proposed a quasi 2-D analytical surface potential model for the homo-/hetero-junction the cylindrical gate (CG) TFETs. They have validated their model results by showing a good matching match with TCAD simulation data at high V_{DS}. However, a little mismatching between the simulation and model results at low V_{DS} is attributed to mobile charge carriers in the channel region.

The analytical drain current modeling of cylindrical surrounded gate based p-n-i-n TFET structure have been proposed by Xu *et al.* [Xu *et al.* (2015)] by including the effects of both the depletion regions at source/channel and drain/channel junctions. The drain current has been modelled by integrating the BTBT generation rate over the entire volume of the CG p-n-i-n TFET structures.

Wu *et al.* [Wu *et al.* (2015)] have reported a 2-D analytical model of the DG TFETs by taking the effect of source depletion region into consideration to investigate short channel effects (SCEs) on the transfer characteristics of the device. It is shown that the OFF-state current becomes significantly large for channel lengths below twice of the scale length.

Taur *et al.* [Taur *et al.* (2015)] have reported a 2-D analytical model for the drain current of heterojunction DG TFET by assuming an exponential barrier height. They have used the closed form approximation of the Wentzel-Kramer-Brillouin integral to model the I-V in terms of a single integral of a continuous function with respect to energy [Taur *et al.* (2015)]. They have shown that source degeneracy helps the linear region of the $I_d - V_{DS}$ characteristics while the source degeneracy degrades the saturation current. The role of the effective density of states on the debasing of V_{GS} due to channel inversion charge at low V_{DS} is also investigated by them [Taur *et al.* (2015)].

Prabhat and Dutta [Prabhat and Dutta (2016)] have proposed a 2-D analytical model for the surface potential and drain current of dual-metal-gate (DMG) DG TFETs by taking the effects of depletion regions at source/channel and drain/channel junctions into consideration. Their proposed analytical drain current model is claimed to be valid for both the positive and negative gate bias voltages of the device.

Bagga and Sarkar [Bagga and Sarkar (2016)] reported 2-D analytical model for surface potential, electric field, and drain current of the triple-material-gate (TMG) DG TFETs by using tunnel barrier modulation concept. They have shown that the ON and OFF currents can be optimized by selecting proper work functions of the three gate-electrode materials of the device.

Dash *et al.* [Dash *et al.* (2016)] have proposed a 2-D analytical model for the drain current of cylindrical-gate (CG) TFET by using a linearly graded binary metal alloy gate. The proposed TFET structure is reported to have better performance in terms of SS and figure of merits than the conventional CG TFET device.

Wang *et al.* [Wang *et al.* (2016)] have proposed an analytical model for including the combined effects of hetero-gate-dielectric and source pocket on the drain current of DG TFETs. Their proposed device structure is shown to provide larger ON current with smaller ambipolar conduction than the hetero-gate-dielectric DG TFETs and DG TFETs with a source-pocket.

The channel potential and drain current of cylindrical gate-all-around (GAA) TFETs are analytically modeled by Khaveh and Mohammadi [Khaveh and Mohammadi (2016)]. They have included the effects of mobile charge carriers in the channel region and depletion regions at both the source/channel and drain/channel junctions for improving the accuracy of their model.

Dutta *et al.* [Dutta *et al.* (2016)] have proposed an analytical BTBT current model of symmetric/asymmetric DG TFETs of sub-45-nm gate lengths. They used a high doping in the source and drain regions while keeping a low doping in the channel region. The tunneling current of the DG TFETs is analyzed using Kane's model. Their proposed

model is used to explain the effects of oxide thickness on tunneling current under the symmetric front and back gate bias voltages.

Dash *et al.* [Dash *et al.* (2016)] have analytically modeled the surface potential, electric field, drain current and the threshold voltage of the cylindrical gate (CG) TFETs with δ-doping profile based source region. The introduction of the δ-doping in the source is found to improve drain current, I_{ON}/I_{OFF} current ratio, and subthreshold swing characteristics over the conventional CG TFETs.

Dong *et al.* [Dong *et al.* (2016)] have reported a compact analytical model for the electrical characteristics of heterojunction DG TFETs by taking the effects of source depletion region for a better accuracy. They have observed that the shortest tunneling path severely affect the electrostatics of the proposed device.

A 3-D analytical electrostatic surface potential based drain current model of tri-gate (TG) TFETs have been reported by Marjani *et al.* [Marjani *et al.* (2016)] by using the perimeter-weighted-sum approach. They have modeled the drain current by integrating the BTBT generation rate over the volume of the device.

Upasana *et al.* [Upasana *et al.* (2017)] have proposed the drain current model of a DG p-n-p-n TFET structure using the Lambert-W function. The model is shown to be valid from the accumulation to inversion region of operation of the device. The Poisson's equation is solved for obtaining the surface potential of their proposed device structure by including mobile charge carriers. The various figure of merits (FOMs) of their proposed DG p-n-p-n TFET structure has also been analyzed for better understanding of circuit design applications.

The 2-D analytical modeling of the surface potential, electric field and drain current of

DG TFET is proposed by Lu *et al.* [Lu *et al.* (2017)]. For a better accuracy of their model, they have considered the effects of source/channel and drain/channel depletion regions on the characteristics of the device. They have also developed the threshold voltage model by using the concept of maximum transconductance method.

Xu *et al.* [Xu *et al.* (2017)] have proposed the analytical modeling of surface potential and drain current of gate-all-around (GAA) TFETs by considering the depletion charges at source/channel as well as drain/channel junctions.

Guan *et al.* [Guan *et al.* (2017)] have proposed a 2-D analytical model for the drain current of DG heterojunction TFET by considering the inversion charges in the channel region. The tangent line approximation (TLA) method has been used to derive the BTB tunneling current of the device.

Safa *et al.* [Safa *et al.* (2017)] have developed a generalized 2-D analytical threshold voltage model for triple-material gate (TMG) DG TFETs. The proposed threshold voltage model is also shown to be applicable for the single-material gate and double-material gate based DG TFETs.

1.6 Summary of the Literature Review: Motivation behind the Present Thesis

We have already reviewed some important state-of-the-art research works related to experimental and theoretical studies of various conventional TFETs structures obtained by employing multi-gate engineering (double-gate, tri-gate, cylindrical gate), gate-electrode material engineering (dual/triple materials gate), gate-oxide engineering (high-*k* dielectric, vertical or horizontal SiO_2/high-*k* stacked oxide etc.), source material engineering (*i.e.,* use of a low band gap material in the source region) and channel

material engineering (*i.e.,* of a different material other than Si or use of a strained-Si channel) in above section. The major observations of the literature survey may be outlined in the following.

- As compared to the conventional TFETs devices, the gate electrode engineered (*i.e.,* dual/triple materials gate) TFETs [Boucart and Ionescu (2007), Padilla *et al.* (2012), Yadav *et al.* (2013), Navjeet Bagga *et al.* (2015), Ambika *et al.* (2017)] are better with respect to the suppression capability of the ambipolar current conduction due to the reduced longitudinal electric field near the drain side. Further, the gate-electrode engineered TFETs have higher ON current, better I_{ON}/I_{OFF} current ratio and steeper SS [Saurabh and Kumar (2011), Kumar and Raj (2015), Pandey *et al.,* (2015)] than the conventional TFETs.
- Gate-oxide engineered TFETs with stacked vertical/lateral SiO_2/HfO_2 structures [Choi and Lee (2010), Jain *et al*. (2015), Choi and Lee (2016), Ping Wang *et al*. (2016), Gracia *et al.* (2017)] have larger ON-current, better transconductance, reduced ambipolar current and lower SS characteristics over the conventional TFETs due to the decreased tunneling barrier width of the device. However, the ambipolar current of the TFETs with only high-*k* (HfO_2) as gate oxide is observed to be larger than the conventional TFETs with SiO_2 as gate oxide [Choi and Lee (2010)].
- The heterojunction TFET structures [Kane (1960), Sze (1981)] may provide better flexibility for enhancing the electrical characteristics (*i.e.,* ambipolarity effect, drive current, I_{ON}/I_{OFF} current ratio and subthreshold swing) [Graef *et al.* (2014), Villani *et al.* (2015), Ahish *et al*. (2016), Mehta *et al.,* (2016), Guan *et al.* (2017), Graef *et al.* (2018)] than the conventional homojunction TFETs. The

heterojunction TFET devices have major advantages: (i) They have larger tunneling probability of charge carriers from the valence band of the source to conduction band of the channel due to lowering of tunneling barrier width owing to the decreased energy band gap of the source [Taur et al., (2015), Ashis et al., (2016)]; (ii) they have reduced ambipolar conduction current due to lower electric field at the drain/channel junction [Krishnamohan *et al.,* (2008), Kim et al., (2010)]. However, the analytical modeling of the electrical characteristics of hetero-junction TFETs by including the effects of depletion charges at the source/channel and drain/channel junctions are very difficult due to the complexities in the heterojunction physics [Taur *et al.* (2015), Dong *et al.* (2016), Ahish *et al.* (2016)].

- Although a large number of models for surface potential, electric field and drain current of the TFETs devices have been reported by excluding the depletion charges at source/channel and drain/channel junctions [Gholizadeh and Hosseini (2014), Dash and Mishra (2015), Safa *et al.* (2017)]. However, due to finite doping concentrations of source and drain regions, it is necessary to include the effects of depletion charges for improving the accuracy of models [Bardon *et al.* (2010), Zhang *et al.* (2012), Dutta *et al.* (2016), Dong *et al.* (2016)]. Further, the effect of mobile charge carriers on the electrical characteristics of the TFETs must be taken into consideration for improving the accuracy of the models.

It is observed that there are ample opportunities for investigating the performance characteristics of some gate-electrode and gate-oxide engineered home-/hetero-junction DG TFETs. The compact models of such advanced TFET structures by considering the effects of depletion charges at the source/channel junction and drain/channel junctions

as well as mobiles charges in the channel could be great interests to the researchers working in the modeling and simulation of advanced TFETs for future generation CMOS technology. Based on the above observations from the literature, we will now define the scopes of the present thesis in the following section.

1.7 Scopes of the Thesis

The basic objective of this thesis is to carry out some theoretical and simulation based investigations of some gate-electrode and gate-oxide engineered home/heterojunction double-gate (DG) TFETs. Under gate-electrode engineering, the dual-material gate (DMG) electrode structure has been explored for enhancing the drive current and reducing the ambipolarity effect in the TFET devices. In DMG structure, the gate electrode material over the gate-oxide consists of two metal-like materials of different work functions connected in cascade in non-overlapped manner so that material near the source side (called tunneling gate) has lower work function than that of the gate-electrode material near the drain side (*i.e.,* auxiliary gate) of the device. The sum of the tunneling and auxiliary gate lengths equals to the total gate length of the device. Under gate-oxide engineering, instead of using the conventional SiO_2 as the gate oxide, we have used a vertical/lateral stacked gate-oxide structure of SiO_2 and HfO_2. In homojunction TFETs, the source, channel, and drain regions are assumed to be of the same materials while a low band gap material such as Ge is used for the source region in the heterojunction TFETs with Si in both the channel and drain regions of the device. The heterojunction TFETs is generally used to improve the drive current with reduced ambipolar effect. The effects of gate-electrode and gate-oxide engineering on the I_{ON}/I_{OFF} ratio and subthreshold swing characteristics of the homo/heterojunction DG

TFET structures have been studied. The entire thesis has been presented in SIX Chapters including the present one. The contents of the remaining FIVE chapters of the thesis are outlined as follows:

Chapter-2 presents the analytical modeling of electrical characteristics such as surface potential, drain current, and the threshold voltage of the DG TFETs with a vertical SiO_2/HfO_2 stacked gate-oxide structure. Parabolic approximation method has been used for solving the two-dimensional (2-D) Poisson equation in the channel region to obtain the channel potential distribution of the device. The channel potential model has been developed by considering the depletion regions at source/channel and drain/channel junctions for better accuracy. The band-to-band tunneling generation rate has been expressed as a function of channel electric field derived from the channel potential of the device. The generation rate function has then been integrated analytically over the channel thickness to derive the drain current of the stacked-gate DG TFETs using the shortest tunneling path (L_t) concept. The maximum transconductance method has been used to extract the threshold voltage from the drain current of the device. The effects of various device parameters on the channel potential, drain current, and the threshold voltage have been investigated. The model results have been compared with the simulation data obtained using the commercially available ATLAS^{TM} 2-D device simulator from SILVACO for the validity of the proposed model.

Chapter-3 reports the 2-D analytical modeling of surface potential, electric field, drain current, and threshold voltage of dual-material (DM) double-gate (DG) TFETs with a vertical SiO_2/HfO_2 stacked gate-oxide structure. Following the parabolic-approximation technique of Chapter-2, the 2-D Poisson's equation has been solved for the channel potential function by using suitable boundary conditions. The band-to-band

tunneling generation rate, drain current, and the threshold voltage of the proposed TFET structure have been modeled in the similar manner as considered in Chapter-2. The effects of tunnel gate and auxiliary gate lengths in the DMG gate-electrode structure, thicknesses of SiO_2 and HfO_2 oxides in the gate-oxide structure and other device parameters on the drain current characteristics, subthreshold swing, I_{ON}/I_{OFF} ratio and the threshold voltage of the proposed DMDG TFET structure has been studied. The results of the proposed models have been validated by comparing them with the simulation data obtained by using the commercially available ATLAS™ TCAD device simulation software.

Chapter-4 presents the 2-D analytical modeling of the electrical characteristics such as surface potential, drain current, and threshold voltage of dual-material (DM) heterogeneous gate dielectric (HGD) DG TFETs with localized interface charges. In the heterogeneous gate dielectric (HGD) structure of the proposed TFET, the gate-oxide consists of the cascade connection of HfO_2 and SiO_2 under the tunnel gate and auxiliary gate regions, respectively. Using the parabolic approximation method, the 2-D Poisson's equation is solved for channel potential of the device by considering the effects of the localized charges near the source/channel junctions, mobile charges in the channel region, and the depletion regions at source/channel and drain/channel junctions. The band-to-band tunneling (BTBT) generation rate has been developed by taking the effects of the electric fields at source/channel and drain/channel junctions into consideration. The drain current model for both the positive and negative bias voltages has been derived by using the tangent line approximation (TLA) method. The threshold voltage model of the proposed DM-HGD DG-TFET structure has been developed by using the concept of shortest tunneling path. The impact of localized interface charges

on the drain current and threshold voltage for different the device dimensions have also been investigated in this chapter. The validity of our model results are verified by comparing them ATLAS^{TM} based TCAD simulation data.

Chapter-5 presents the 2-D analytical modeling of surface potential, drain current, and threshold voltage model of double-gate (DG) heterojunction tunnel field-effect transistors (HJTFETs) with a SiO_2/HfO_2 stacked gate-oxide structure. The germanium (Ge) is used for the source while the silicon (Si) has been considered for both the channel and drain regions of the proposed device. The surface potential model has been developed by considering the effect of accumulation/inversion charges and depletion charges of the source/channel and drain/channel junctions. The electric field-dependent band-to-band tunneling (BTBT) generation rate has been derived from the surface potential model. The tangent line approximation (TLA) method has been used to calculate the drain current of the proposed DG HJTFETs. The developed model is considered to be valid for all regions (*i.e.,* from subthreshold to strong accumulation/inversion region) of operation of the device. Finally, the threshold voltage model has been developed by using the shortest tunneling path concept. The model has also been shown to be applicable for III–V materials (*e.g.,* InAs/GaSb) based DG HJTFETs, and silicon-on-insulator (SOI) based HJTFETs. Further, the proposed model can also be applicable for conventional Si homojunction-based TFETs. A reasonably good matching between the model results and 2-D ATLAS^{TM} TCAD simulation data is obtained to show the validity of the proposed models presented in this chapter.

Chapter-6 includes the overall summary and conclusion of the works carried out in the present thesis. Finally, some future scopes of research related to TFETs carried out in the present thesis have been briefly discussed at the end of this chapter.