Preface

As CMOS technology is scaling down below sub-100 nm to follow Moore's law, a number of challenges come in the optimization of the performance of the MOS transistors. Severe increase in the subthreshold current with the decrease in the gate length of the MOS transistors imposes the important challenges of minimizing the static power consumption of the device. Besides improving the energy-efficiency of CMOS circuits, another important challenge is to improve the switching characteristics by reducing the subthreshold swing of the MOS transistors. For the conventional MOS transistors working on the principle of either surface inversion or volume inversion theory, the subthreshold swing can't be reduced below the Boltzmann limit of the 60 mV/decade. The tunnel field effect transistor (TFET), also known as the green transistor, is good potential device for replacing the conventional MOS transistors for its extremely low OFF-state current and low subthreshold swing (SS) much below the theoretical Boltzmann limit of 60 mV/decade applicable for the conventional MOS devices. However, the low ON-state current and drain current dependence on the gate voltage (*i.e.,* ambipolarity phenomenon) are the major drawbacks of the TFETs. To overcome them, various techniques such as the work-function engineering (*i.e.,* combination of different materials with different work functions in cascade to form the gate electrode), channel engineering (*i.e.,* use of strained-Si channel), gate-dielectric engineering (*i.e.,* high-*k* dielectrics in place of SiO_2 either in the form of single dielectric or lateral/vertical stacked gate oxide, SiO_2/high-*k* etc.), multi-gate engineering (*i.e.,* double-gate, tri-gate, gate all around), negative capacitance engineering (*i.e.,* using ferroelectric materaial as gate oxide), low band gap engineering (*i.e.,* low band-gap such as Ge, InAs in the place of Si channel), source/drain engineering (*i.e.,* use of low band-gap materials such as Ge and InAs as a source) and heterojunction source(drain)/channel engineering have been explored by the researchers to overcome the above drawbacks. In view of the above, the present thesis deals with some theoretical investigations of performance characteristics of some gate-electrode and gate-oxide structure engineered home/heterojunction double-gate (DG) TFETs. Under gate-electrode engineering, the dual-material gate (DMG) electrode structure has been

explored for enhancing the drive current and reducing ambipolarity effect in the TFET devices. In the DMG structures, the entire gate electrode over the gate-oxide consists of two non-overlapped regions of two different metals connected in cascade where the work function of metal gate near the source side (called tunneling gate) is maintained lower than that of the metal gate near the drain side (*i.e.,* auxiliary gate) so that the sum of the tunneling and auxiliary gate lengths equal to the total gate length of the device. Under gate-oxide engineering, instead of using the conventional SiO_2 as the gate oxide, two different types of gate oxide structures have been studied: One structure uses a stacked gate-oxide structure of SiO_2/high-k (*e.g.,* HfO_2) while the other gate-oxide structure consists of cascade connection of SiO_2 and high-k (*e.g.,* HfO_2) in the proposed TFETs investigated in this thesis. In homojunction TFETs, the source, channel and drain regions are assumed to be of the same materials. On the other hand, a low band gap material (*e.g.,* Ge) is used for the source region and a material (*e.g.,* Si) with band gap energy larger than that of the source is considered for both the channel and drain regions in the heterojunction TFET structures. The heterojunction TFETs is generally used to improve the drive current with reduced ambipolar effect. The effects of gate-electrode and gate-oxide engineering on the I_{ON}/I_{OFF} ratio and subthreshold swing characteristics of the homo/heterojunction DG TFET structures have been studied in the present thesis. Both depletion regions created at the source/channel junction and drain/channel junctions due to finite doping concentration of the source, channel and drain regions have been considered for improving the accuracy in the modeling of the electrical characteristics of TFETs considered in this thesis. The overall chapter-wise layout of the thesis is given below:

Chapter-1 presents a brief introduction of TFETs and their properties for low power applications. Various reported techniques used for improving the drive current of the TFETs have also been discussed. A general review of various state-of-the-art theoretical and simulation works on the TFETs been briefly discussed. Finally, based on the literature survey, the scopes of the present thesis have been outlined at the end of this chapter.

Chapter-2 presents the analytical modeling of electrical characteristics such as surface potential, drain current, and the threshold voltage of the DG TFETs with a SiO_2/HfO_2 stacked gate-oxide structure. Parabolic approximation method has been used for solving the two-dimensional (2-D) Poisson equation in the channel region to obtain the channel

potential distribution of the device. The channel potential model has been developed by considering the depletion regions at source/channel and drain/channel junctions for better accuracy. The band-to-band tunneling generation rate has been expressed as a function of channel electric field derived from the channel potential of the device. The generation rate function has then been integrated analytically over the channel thickness to derive the drain current of the stacked-gate DG TFETs using the shortest tunneling path (L_t) concept. The maximum transconductance method has been used to extract the threshold voltage from the drain current of the device. The effects of various device parameters on the channel potential, drain current, and threshold voltage have been investigated. The model results have been compared with the simulation data obtained using the commercially available ATLAS 2-D device simulator from SILVACO for the validity of the proposed model.

Chapter-3 reports the 2-D analytical modeling of surface potential, electric field, drain current, and threshold voltage of dual-material (DM) double-gate (DG) TFETs with a SiO_2/HfO_2 stacked gate-oxide structure. Following the parabolic-approximation technique of Chapter-2, the 2-D Poisson's equation has been solved for the channel potential function by using suitable boundary conditions. The band-to-band tunneling generation rate, drain current and threshold voltage of the proposed TFET structure have been modeled in the similar manner as considered in Chapter-2. The effects of tunnel gate and auxiliary gate lengths in the DMG gate-electrode structure, thicknesses of SiO_2 and HfO_2 oxides in the gate-oxide structure and other device parameters on the drain current characteristics, subthreshold swing, I_{ON}/I_{OFF} ratio and threshold voltage of the proposed DMDG TFET structure have been studied. The results of the proposed models have been validated by comparing them with the simulation data obtained by using the commercially available ATLAS^{TM} TCAD device simulation software.

Chapter-4 presents the 2-D analytical modeling of the electrical characteristics such as surface potential, drain current, and threshold voltage of dual-material (DM) heterogeneous gate dielectric (HGD) DG TFETs with localized interface charges have been investigated. Using the parabolic approximation method, the 2-D Poissons equation is solved for channel potential of the device by considering the effects of the localized charges near the source/channel junction and mobile charges in channel region as well as the effect of the depletion regions formed at source/channel and drain/channel junctions. The band-to-band tunneling (BTBT) generation rate has been developed by

taking the effects of the electric fields at source/channel and drain/channel junctions. The drain current model for all gate bias (*i.e.,* from ambipolar to forward gate bias) has been derived by using the tangent line approximation (TLA) method. The threshold voltage model has been developed by using the concept of shortest tunneling path of the proposed DM-HGD DG-TFET structure. The impact of localized interface charges on the drain current and threshold voltage by varying the device dimensions are also investigated. The validity of our model results are verified by comparing them ATLAS^{TM} based TCAD simulation data.

Chapter-5 presents the 2-D analytical modeling of surface potential, drain current, and threshold voltage model of double-gate (DG) heterojunction tunnel field-effect transistors (HJTFETs) with a SiO_2/HfO_2 stacked gate-oxide structure. The surface potential model has been developed by considering the effect of accumulation/inversion charges and depletion region at source/channel and drain/channel junctions. The electric field-dependent band-to-band tunneling generation rate has been derived from the surface potential model. The tangent line approximation (TLA) method has been used to calculate the drain current of the proposed DG HJTFETs. The developed model is considered to be valid for all regions (*i.e.,* subthreshold to strong accumulation/inversion region) of operation. Finally, the threshold voltage model has been developed by using the shortest tunneling path concept. A reasonably good matching between the proposed analytical model results and 2-D ATLASTM TCAD simulation data is obtained to show the validity of the models presented in this chapter.

Chapter-6 includes the summary and conclusions of this thesis. Some possible future scopes of research in the related area of the present thesis are presented at the end of this chapter.