AUTHOR'S RELEVANT PUBLICATIONS

Journals:

1. **Sanjay Kumar**, Ekta Goel, Kunal Singh, Balraj Singh, Mirgender Kumar and Satyabrata Jit, "A Compact 2-D Analytical Model for Electrical Characteristics of Double-Gate Tunnel FET with a SiO_2/High-k Stacked Gate-Oxide Structure," ***IEEE Transactions on Electron Devices,*** vol. 63, pp. 3291-3299, (2016).

2. **Sanjay Kumar**, Ekta Goel, Kunal Singh, Balraj Singh, Prince Kumar Singh, Kamlaksha Baral and Satyabrata Jit, "2-D Analytical Modelinng of the Electrical Characteristics of Dual-Material DG TFETs with a SiO_2/High-*k* Stacked Gate-Oxide Structure," ***IEEE Transactions on Electron Devices,*** vol. 64, pp. 960-968, (2017).

3. **Sanjay Kumar**, Kunal Singh, Sweta Chander Ekta Goel, Balraj Singh, Prince Kumar Singh, Kamlaksha Baral and Satyabrata Jit, "2-D Analytical Drain Current Model of Heterojunction DG TFETs with a SiO_2/High-*k* Stacked Gate-Oxide Structure," ***IEEE Transactions on Electron Devices,*** vol 65, no.1 pp. 331-338, Jan.(2018).

4. **Sanjay Kumar**, Kunal Singh, Sweta Chander Ekta Goel, Prince Kumar Singh, Kamlaksha Baral and Satyabrata Jit, "2-D Analytical Modelinng for Electrical Characteristics of Dual-Material Heterogenious Gate DG TFETs with Localized Interface Charges," ***IEEE Transactions on Electron Devices.***(Communicated)

International Conference:

1. **Sanjay Kumar**, Kamalaksha Baral, Sweta Chander, Kunal Singh, Prince Kumar Singh, and S. Jit, "Influence of localized Interface Charges on Drain Current of Dual-Material Double-Gate Tunnel FETs," *International Conferences for Convergence of Technology* **(I2CT)**, *7-8th April,* Pune 2018.

2. **Sanjay Kumar**, Kamalaksha Baral, Sweta Chander, Prince Kumar Singh, Balraj Singh and S. Jit, "Performance Evaluation of Double Gate III-V Heterojunction Tunnel FETs with SiO_2/HfO_2 Gate Oxide Structure," *IEEE International Symposium on Devices, Circuits and Systems* **(ISDCS)**, 29th - 31st March IIST Shivpur, India 2018.

3. **Sanjay Kumar**, Kunal Singh, Sweta Chander, Prince Kumar Singh, Kamalaksha Baral, and S. Jit, "Temperature Sensitivity Analysis of Double Gate Tunnel FETs with SiO_2/HfO_2 Stacked Gate Oxide Structure," *Nanotechnology for Instrumentation & measurement Workshop*, **NANOfIM** , India 2017.

4. **Sanjay Kumar**, Ekta Goel, Kunal Singh, Balraj Singh, Mirgender Kumar, and S. Jit, "A 2D Analytical Model of Double-Gate (DG) Tunnel-Field-Effect Transistor (TFET): Impact of Shortest Tunneling Distance," *18th International Workshop on the Physics of Semiconductor Devices* **(IWPSD)**, @Indian Institute of Science, Banglore, 2015.