Chapter 1

1.1 Introduction

In the modern era, active matrix light emitting display (AMLED) technology has been started to substitute massive cathode ray tube (CRO) from computer monitors. There are two different types of flat panel display; one of them is “active matrix” and another one is “passive matrix” display. In around 1995, active matrix thin film transistor (TFT) based flat panel display was adopted the first time in the laptop screen. Flat panel display is also a new appliance in large screen display, TVs, smartphones, tablets and laptops; these are the most important components. Hence, TFTs are important features of the most ordinary type of active matrix display technology. In active matrix display, TFT works as a driver (switching device) to drive a pixel in display ‘on’ (light) or ‘off’ (dark).

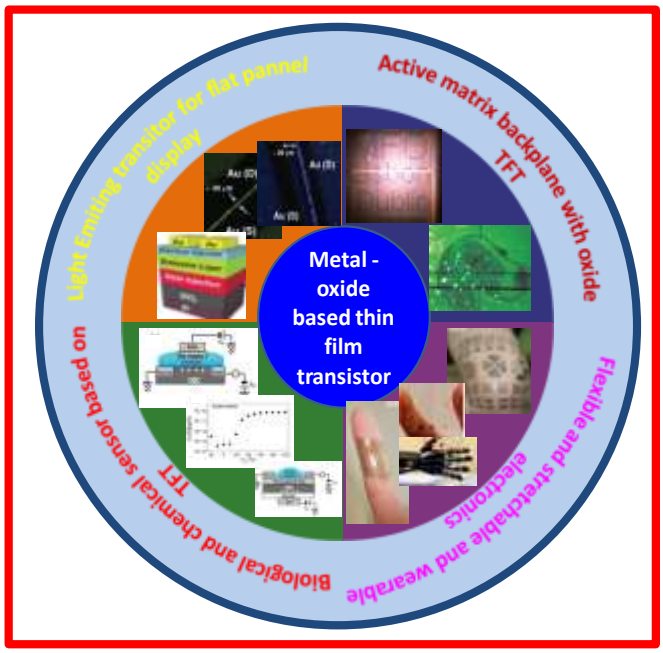

Figure 1.1: *Schematic of low voltage TFT application in various technologies.*

Higher resolution, higher color accuracy, faster refresh rates and thinner form factor are the key requirements for the most immersive viewing experience display with high pixel density (pixel per inch (ppi)). Therefore, the development of next-generation AMD display demands a higher performance TFT to improve its quality display with lower cost. In addition to display technology, metal oxide TFT can be used in different electronics and optoelectronics application which is summarized in **figure 1.1**. A TFT mainly consists of three terminals; gate, source and drain. Source and drain electrodes are separated from the gate by an insulator commonly called a gate dielectric. Transistor drain-current flows in between the source and drain electrodes through an active channel semiconductor layer which is controlled by the gate electrode. Materials of the gate dielectric, active channel layer and their fabrication process play a very crucial role in the performance of TFTs. There exist various techniques to fabricate thin film transistors e.g. vacuum based methods like sputtering, molecular beam epitaxy (MBE), chemical and atomic vapor depositions. Although, high quality thin films can be deposited by the vacuum based technique but those techniques require expensive infrastructure. Moreover, for large area electronics application, the production rates of those vacuum-based deposition techniques are not satisfactory. In a combination of these two issues, vacuum-based fabrication cost can not be reduced as per demand. Therefore, the development of a non-vacuum based solution-processed technique is required to reduce the production cost. This thesis work particularly focuses the development of that solution processed technique for low operating voltage metal oxide TFT.

1.2 Introduction to TFT

Since their discovery, transistors are a single dominant component as a building block for analytical circuits in the microelectronics industry and this makes a revolutionary impact on every aspect of human life. As the cornerstone of modern electronics, transistor works as the elementary structure of various electronic devices, television, cell phones, including computers and cameras. J. E. Lilienfeld and O. Heil invented the history of the transistor whose early patents indicated several ways in which solid state electronic materials can be employed in amplification devices.[1-3] However, in 1940, Bell Telephone Laboratories demonstrated the first example of a working transistor.[4] While Weimer RCA laboratories recognized a first working thin film transistor in early 1960.[5] In the later 1960, RCA reported the development of the first LCD (liquid crystal display) using TFT which took only the six-year from the invention of TFT.[6] These TFTs are the unipolar device that conducts current by single type charge carrier; i.e. electron or hole. This conduction is controlled by an electric field applied at the gate electrode, which essentially trigger the signal amplification or electrical switching. TFTs are constructed using three main components **(figure 1.2 a))**, namely i) a dielectric layer through which, the modulation of current is attained by the capacitive effect between the gate and active layer (semiconductor) is established ii) a semiconductor layer that acts as an active channel in which charge carriers accumulates as shown in **figure 1.2 b)** (i.e., electrons or holes) are moved laterally iii) metallic electrodes (source (S), drain (D) and gate (G)), the injection or extraction of charge carriers from source and drain, respectively whereas gate electrode is capable of modulating the charge conduction from source-to-drain.

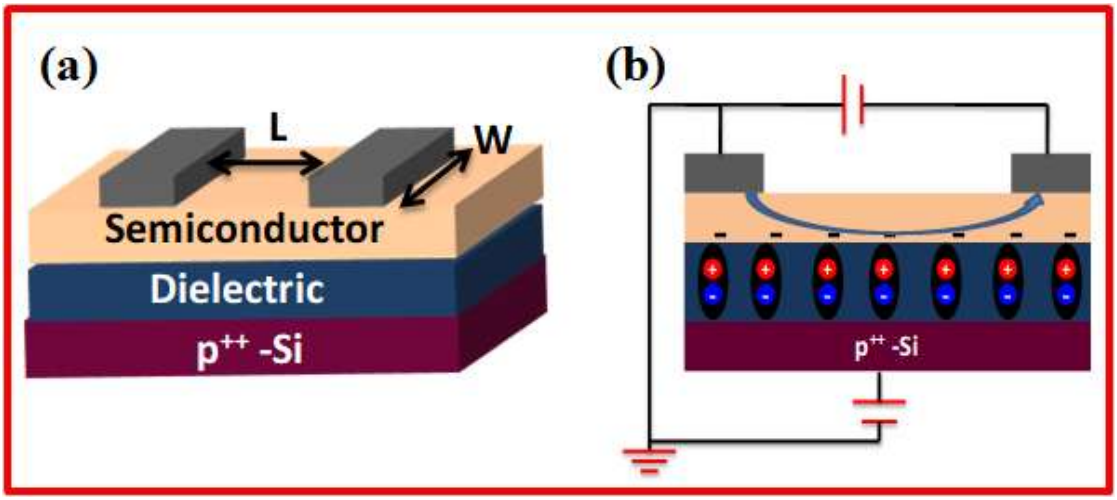

Figure 1.2: *A schematic diagram of* ***a)*** *TFT with the bottom gate and top contact arrangement* ***b)*** *charge transportation in TFT channel under the applied electric field.*

1.3 Device configuration

In general, there are four basic device structures namely (a) staggered top gate (STG); (b) staggered bottom gate (SBG); (c) coplanar top gate (CTG); and (d) coplanar bottom gate (CBG), as shown in **figure 1.3**. Active layer isolates gate electrode from source and drain electrodes in opposite sides in staggered geometry. Alternatively, all three electrodes located on the same side of the active layer in the coplanar structure. Each geometry has its own advantages and disadvantages, however transistors with the same materials but dissimilar geometries can demonstrate different behavior.[7] The staggered bottom gate is regularly used TFT configuration because it is possible to achieve high device performance with simple fabrication steps. In this thesis, we worked with the BG/TC geometry **(figure 1.3 a))** because this structure gives the high performance and low contact resistance owing to its more effective area that provides facile injection of charge into the active layer **(figure 1.2 b))**.

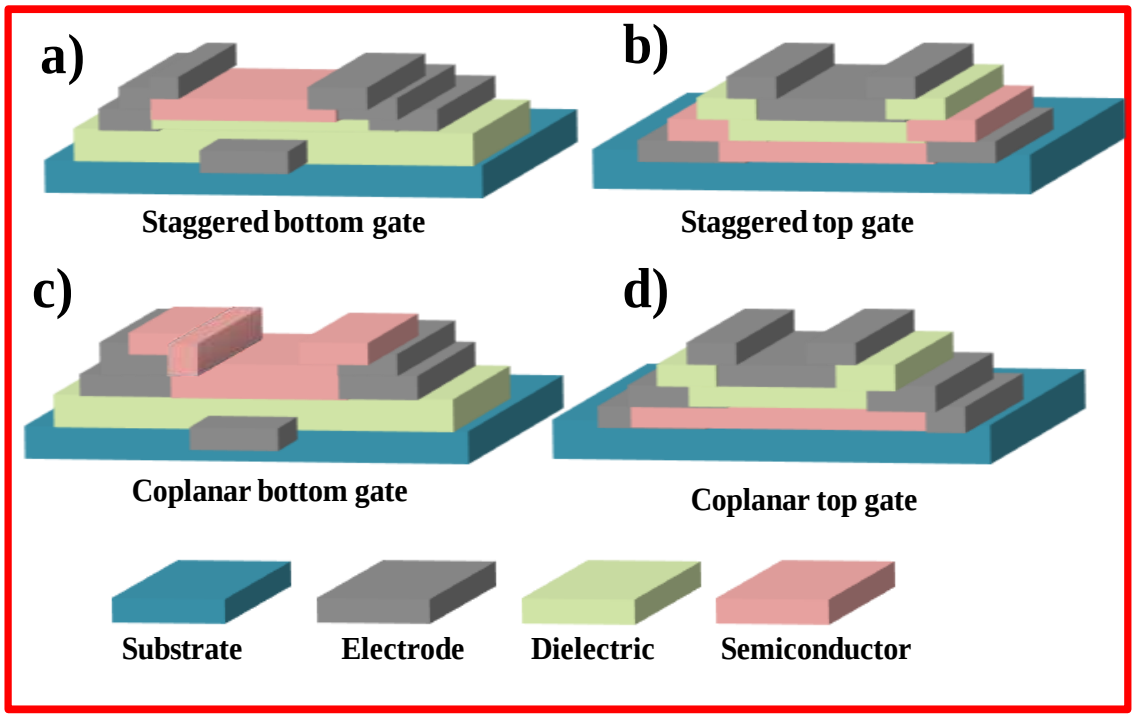

Figure 1.3: *Schematic diagram of the configuration of the thin film transistor* ***a)*** *staggered bottom gate* ***b)*** *staggered top gate* ***c)*** *coplanar bottom gate* ***d)*** *coplanar top gate.*

1.4 Operation of TFT

In this section, we will briefly explain the fundamental operation of the TFT and the role of the gate dielectric in it. Thin film transistors are basically operated in accumulation mode unlike the MOSFET, which commonly works in depletion mode. By application of the positive gate voltage (V_G), it electrostatically produces the polarization of charge in the dielectric materials while the source voltage is normally grounded. This polarization enables the accumulation of the charge carrier (electron) in an n-type semiconductor at the dielectric-semiconductor interfaces. These accumulated charge carriers in semiconductor form a conducting channel between the source and drain.[8] These movements of the charge carrier in this channel occurred from the source electrode side and finally enter the drain end. The accumulated charge carrier density is proportional to the gate voltage and

the capacitance of an insulator. The drain current (I_D) in the active layer between the drain and source electrode is controlled by the drain voltage (V_D). If V_D is less than (V_G-V_T), a uniform density of charge carrier is formed in the channel. The current-voltage relations in a TFT can be derived based on the gradual channel approximation ohmic current and calculated analytically with the help of **equation (1)**, leading to the linear region[9]

$$\boldsymbol{I_{D,Lin} = \frac{W}{L}\mu_{Lin}C_i(V_G - V_T - \frac{V_D}{2})V_D} \quad \text{..... (1)}$$

where, W is termed as the channel width, L is known as the channel length and μ (charge carrier mobility). The channel becomes pinched-off at the drain side that saturates the drain current at a certain value of V_D that is $V_D > (V_G\text{-}V_T)$. Using **equation (2)** given below**,** the saturation-region drain current $I_{D,sat}$ can be calculated:

$$\boldsymbol{I_{D,Sat} = \frac{W}{2L}\mu_{Sat}C_i(V_G - V_T)^2} \quad \text{..... (2)}$$

1.5 Extraction of important parameters of TFT

In general, current-voltage characteristics of a TFT are expressed in two ways because of the drain current can be modulated by two independent voltages; drain voltage (V_D) and gate voltage (V_G). The variation of I_D with V_D for constant V_G is called the output characteristics of a TFT. Clear linear and saturation region of I_D and gradual enhancement of I_D with V_G demonstrates the quality of TFT. However, variation of I_D with V_G for constant V_D is call the transfer characteristics of a TFT, give us all important parameters including mobility, on/off ratio, subthreshold swing and subthreshold voltage of the device.

Typical output and transfer curves for n-channel transistors are depicted in **figure 1.4 a) and 1.4 b)** respectively.

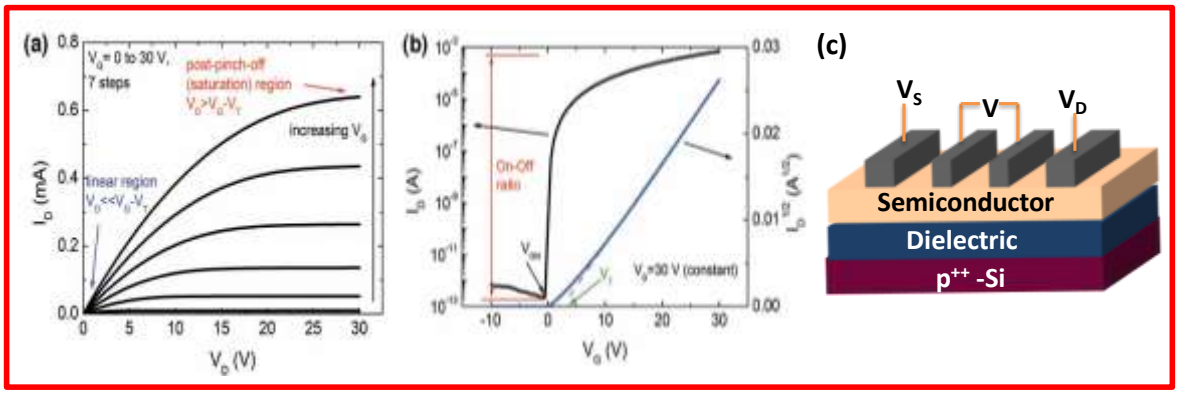

Figure 1.4: *Typical **a)** output and **b)** transfer characteristics of an n-type oxide TFT.[10]**c)** cross-section of devices for gated four point probe Method*

1.5.1 Mobility

Mobility (μ) measures the efficiency of charge carrier transport in the TFT device. In a thin film material, μ can be influenced by numerous scattering parameters, like the thermal vibrations of lattice, ionized impurities and lattice mismatch at the boundaries of grains including undesirable defects related to the crystal structures. Particularly in a TFT, the movement of carriers is constrained to a narrow region close to the dielectric/semiconductor interface.[9] From the application point of view, the saturation mobility of a TFT is the most important parameter and very commonly reported in the literature. Mobilities in linear and saturation regimes can easily be calculated by differentiating **equation (1) and (2)**. In the linear region, mobility is extracted using following equation;

$$\mu_{Lin} = \frac{L}{WC_iV_D}\left(\frac{\partial I_{D,Lin}}{\partial V_G}\right)$$

Similarly, from saturation region mobility is calculated using the equation,

$$\mu_{Sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{D,Sat}}}{\partial V_G}\right)^2$$

1.5.1.1 Issues of the mobility estimations

High values of carrier mobility have been recently reported in newly developed materials for FET or TFTs. However, there is an increasing concern of whether the values are overestimated or not. In this section, we will discuss issues about the mobility calculation using conventional Schottky equations. These equations strongly depend on device geometry and does not account for contact resistance caused by the presence of an injection barrier. We contend that mobility in transistors with resistive contact can be underestimated in the presence of the injection barrier, whereas mobility in transistors with gated Schottky contact can be overestimated by more than 10 times. The latter phenomenon occurs even in long-channel devices, and it becomes more severe when using low-k dielectrics. This is because the band bending and injection barrier experience a complicated evolution on account of electrostatic doping in the semiconducting layer; thus, they do not follow a capacitance approximation. When the band bending is weak, the accumulation is as weak as that in the subthreshold regime. Accordingly, the carrier concentration nonlinearly increases with the gate field. This mechanism can occur with or without exhibiting the "kink" feature in the transfer curves, which has been suggested as the signature of overestimation. For precision, carrier mobility should be presented against gate voltage and should be examined by other recommended extraction method.

Gated 4-probe measurements eliminate the issue of contact resistance but are geometry dependent. Also correct probe positioning and confinement of the semiconducting layer are crucial to generate meaningful results and avoid overestimation. According to this four probe method mobility calculation **figure 1.4 c)**, four probes are deposited on the semiconducting layer in equal separation. Two end probes measure the TFT drain current and two intermediate probe measure the voltage difference. Since, current doesn't flow through these two intermediate probes; therefore, effect of contact resistance on this voltage measurement is literally zero. Two end probes on the other hand, measure the current. After measuring the accurate voltage differences and current, true mobility of TFT can be calculated from the following equation;

$$\mu_{\text{true}} = \frac{1}{C}\frac{\partial\sigma}{\partial V_G} \text{ where } \sigma = \frac{I_{SD}}{[V_{P1} - V_{P2}]}\frac{D}{W}$$

Here, D is the distance between the voltage probes and VP1 and VP2 are their respective potentials. Detail of this measurement has been discussed earlier literatures.[11] A third approach to mobility calculation is the gated van der Pauw method, which removes both of the above limiting factors (i.e., geometry factor and contact resistance) and allows for feasible performance statistics, since a single device can be measured in eight different orientations.[12, 13]

1.5.2 On/Off ratio

On/off current ratio (I_{On}/I_{Off}) is a parameter that represents drain current modulation as applied gate voltage sweep from depletion mode operation to accumulation mode. It is defined as the ratio of the highest current of accumulation mode to the lowest current level in depletion mode operation of transfer characteristics of TFT. Generally, for a good

switching behavior on/off ratio should be as large as possible. The typical values of on/off ratio for TFTs range from10^3 to 10^8. The minimum I_D is normally attained by the gate leakage current and the noise level of the instruments used for measurement, etc., whereas the maximum I_D primarily relies on the active layer itself, nature of the dielectric-semiconductor interface and on the nature of dielectric materials[14].

1.5.3 Subthreshold swing

The minimum variation of gate voltage required to enhance the drain current by an order of magnitude is called as subthreshold swing (SS). SS represents the switching speed of a transistor, i.e. how fast transistor switches from the off state to on state. The SS value of a TFT can be calculated from the transfer curve with the help of **equation (3)** [14];

$$\mathbf{SS} = \left[\frac{\mathbf{d(\log I_D)}}{\mathbf{dV_G}}\right]^{-1} \quad \text{.....(3)}$$

Subthreshold slope also indicate about the superiority of the interface between dielectric and semiconductor as it is related to interface trap density (N_{ss}^{max}) shown in **equation (4)**. The smaller value of (N_{ss}^{max}) implies that the dielectric form an excellent dielectric/semiconductor interfaces which are required for reaching to high carrier mobility in TFT device. From **equation (4)** it is clear that the interface trap density depends on the SS and capacitance of the dielectric layer. Carrier accumulation at the interface is directly proportional to the capacitance of insulator, which implies that greater the capacitance, larger is the accumulation. The expression for N_{ss}^{max} at interfaces has been given below[15],

$$N_{SS}^{max} = \left[\frac{SS \times \log e}{kT/q} - 1\right]\frac{C}{q} \quad \text{.....(4)}$$

1.5.4 Threshold voltage

The threshold (V_T) voltage of a TFT is defined by the minimum gate voltage that requires accumulating carrier in the dielectric/semiconductor interface to form a conductive channel (an accumulation layer). The threshold voltage of the device has been determined by extrapolating the straight line of $I_{DS}^{1/2}$ versus V_G curve. The threshold voltage V_T of TFTs depends on dielectric/semiconductor interface trap state, nature of dielectric, and the thickness of the semiconductor film.[16]

1.6 High-k dielectric materials

For TFT fabrication, SiO_2 is the most commonly used dielectric due to its defect-free nature and high-quality film (free from the pinhole, impurity) that can be grown on highly doped Si just by thermal annealing.[17-19] However, this dielectric has one major disadvantage i.e., the lower dielectric constant (k) because of this most of the TFT requires high operating voltages (≥40V) which limit its application to portable low power electronics. For the demand for high-performance portable electronics devices, it is required to maintain low power consumption. Additionally, core unit size, i.e., field effect transistors (FETs) need to be notably scaled down.[20] According to Moore's law, the number of transistors in a chip has doubled in every two years[21]. This requires the size of FET and thickness of SiO_2 dielectric scaling down. When the thickness of SiO_2 layer approaches atomic scale, the huge amount of leakage current release at 1 V

($J_{leakage}$=1A/cm^2) due to direct tunneling, consequentially in a serious problem for low power consumption and device reliability.[7, 22, 23]

This technological barrier is removed by substituting SiO_2 with high-k HfO_2 (k=25) and other dielectric materials that exhibited high permittivity. In large areal TFT based microelectronics production, high –k dielectrics materials play a key function in reducing energy consumption (low leakage current) as it reduces the operating voltage of TFT. Besides the uses of high-k dielectric, there is another way to reduce the operating voltage of the device, that is lowering the thickness of typical dielectric insulator up to several monolayer thickness that allows lower tunneling current. However, in both cases, it is very essential to maintain high-performance TFT at that lower operating voltage. The relation of capacitance density (C) of the gate insulator of a TFT with a dielectric constant (k) and dielectric thin film thickness (d) according to the **equation (5)**

$$\mathbf{C} = \boldsymbol{k\varepsilon_0 A/d} \qquad \textbf{... (5)}$$

where, k is dielectric constant, A is area of the electrode, d is referred as dielectric thickness and C is the capacitance of the dielectric. The enhancement of capacitance by reducing the thickness of dielectric can be achieved, later alternatively has been displayed by employing self-assembled monolayer and multilayer assembles of organic-inorganic hybrid structure.[24-26] However, high-k dielectric allows the deposition of films with a higher thickness, which reduces gate leakage current even after maintaining the high capacitance properties. In both cases, higher capacitance thin film dielectric is capable to accumulate a larger amount of mobile charge carrier in the semiconductor/dielectric interface of the channel in a TFT at a lower gate voltage.[27]

1.6.1 Dielectric charge polarization mechanism

Dielectrics are electronically insulators which are ionically polarized in the presence of the electric field. Therefore, when an insulator is placed under the electric field, due to the lack of free electron, charge carriers can not pass through such materials; as an alternative, their charge shifted from the position of equilibrium. This phenomenon is called dielectric polarization. Thus, due to the applied field, positive and negative charges are displaced in the reverse direction to field direction generating an intrinsic electric field that weakens the whole field inside the dielectric material.[8, 28] The various polarization mechanisms of materials occurs as depicted in **figure 1.5.** These polarization mechanisms are totally material dependent which can be categorized in different polarization e.g., electronic, ionic, orientation of molecule, chain relaxation counter ions, space charges (condensed counter ions) and the electrode or electric double-layer (EDL) polarization.[29-31] However, all these polarization mechanisms are not active equally in the entire frequency range of external bias. All polarization mechanism with their active frequency range is represented in **figure 1.5 h)**.[8]

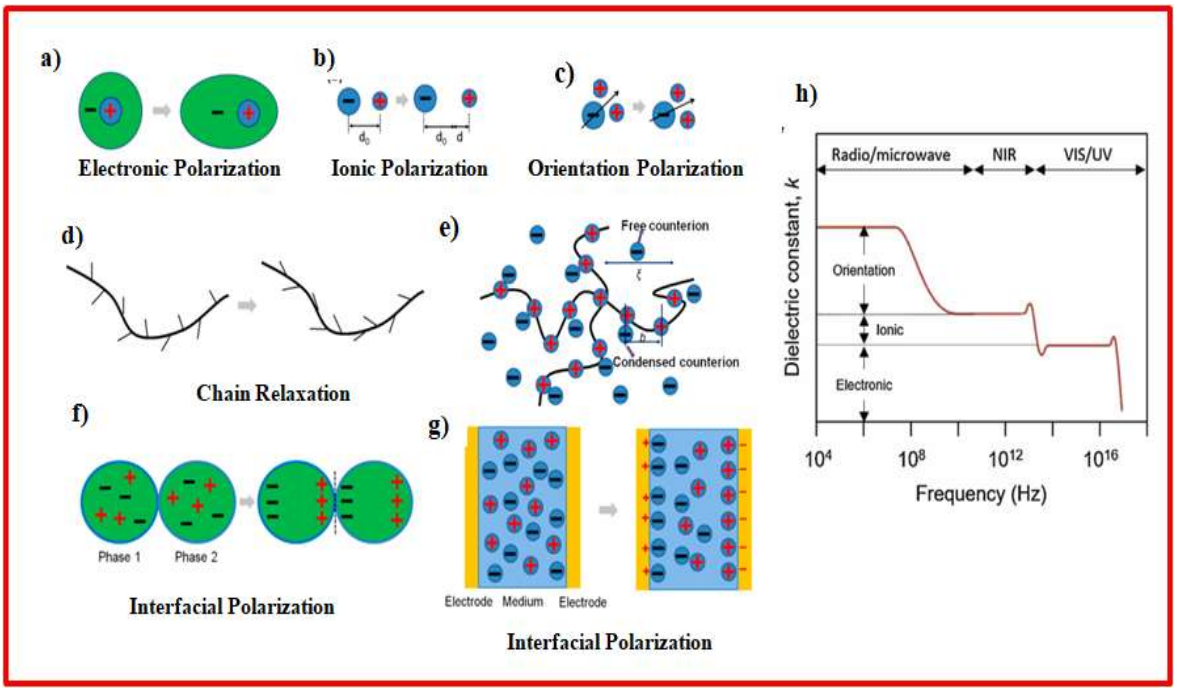

Figure 1.5: *The schematics of basic mechanism of dielectric polarization* ***a)*** *electronics polarization* ***b)*** *ionic polarization* ***c)*** *orientation polarization* ***d)*** *chain relaxation* ***e)*** *free counter ion polarization in electrolyte* ***f)*** *interfacial polarization* ***g)*** *electrode or EDL polarization* ***h)*** *the contribution of the different polarization mechanism to the dielectric constant with various frequency regions.[8, 30]*

Dielectric insulators are characterized by the absence of the charge transport under the applied electric field. The mechanism of the dielectric exemplified with the help of parallel-plate capacitor as shown in **figure 1.6** under the presence and absence of the applied electric field, when there is no electric field the charge distribution is spontaneous or in equilibrium and absence of directional effect **(figure 1.6 c))**. Polarization occurrs in the dielectric material under the applied electric field by applying a positive bias to the bottom metal plate resulting in the form of a net dipole moment averaged throughout the volume, this creates a surface charge density at upper and lower part of the dielectric as shown in **figure 1.6 c)**. The amount of accumulated charge Q indicates the capacity of a

capacitor to accumulate electrical charges at the given field; the capacitance (C) of parallel-plate capacitor is expressed using **equation 5**.[32]

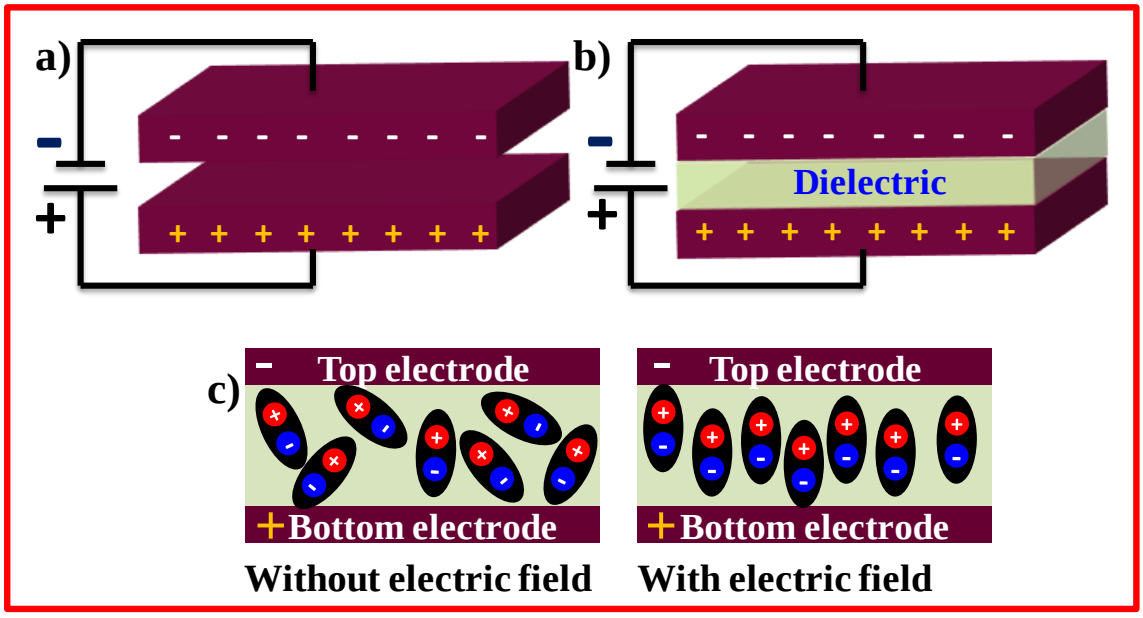

Figure 1.6: *The simple schematic diagram of the basic mechanism of parallel plate metal-insulator-metal capacitor* ***a)*** *with dielectric layer* ***b)*** *without dielectric layer* ***c)*** *dipole polarization mechanism under the no applied electric field and under the applied field. .*

1.7 Choice of dielectric for low operating voltage TFT

During the past decade, a series of insulating materials reported as a gate dielectric through advanced processing techniques for the development of the microelectronics, low operating voltage and high on-off ratio TFTs devices. These new emerging dielectrics can be divided into a few categories: (a) self-assembled monolayer (SAM)[33-35] (b) self-assembled multilayer nanodielectrics (SANDs)[36-38] (c) high-k metal oxide dielectrics[32, 39-43] (d) nanostructured and nanocomposite dielectrics[44-48] (e) ion-gel dielectrics[48-50] (f) polymer electrolyte dielectrics[51-54] and (g) ion-conducting oxide dielectrics.[55-58] Among the above mention list of dielectric, SAM is one unique class of dielectric that is

widely used for fabricating low operating voltage organic TFTs. In addition to the low operating voltage, it is also compatible to fabricate mechanically flexible TFT. Similar to SAM, SANDs is also another popular dielectric for organic and flexible organic TFT fabrication. Ion-gel dielectric has been used more widely for the fabrication of organic TFTs, performance of this ion-gel dielectric is even better than SAM and SANDs dielectric. However, all these three class of dielectrics are not a very good choice for high temperature annealed metal-oxide TFT fabrication. Particularly for sol-gel metal oxide TFT fabrication high-k oxide dielectric and ion-conduction metal oxide dielectrics are the best choices. In the area of metal oxide dielectric, a large number of novel dielectrics (HfO_2, Al_2O_3, ZrO_2, TiO_2, Y_2O_3 and Ta_2O_5, etc.) have been developed as a substitute to the traditional SiO_2 insulating layer (k = 3.9) and all of them can be synthesized in a solution processed technique.[43, 59-63] However, solution processed low operating voltage metal oxide TFT shows the best performance with ion-conducting metal oxide dielectric. This class of dielectric contains lightweight metal ion (like Na^+, Li^+, K^+) which are capable to move freely through the crystal channel. Due to the free movement of such light cation, this dielectric thin film can be easily polarized by applying external bias. In addition to excellent ionic conductivity, these dielectric materials are electronically very insulating and have a larger bandgap. Combination of these unique properties makes this class of materials as a novel gate dielectric for low voltage TFT fabrication. Typically, in an inorganic dielectric, the dielectric constant varies inversely to the bandgap as shown in **figure 1.7 a)**. For gate dielectric application, the band offset of the dielectric materials with respect to silicon should be greater than 1 eV as shown in **figure 1.7 b)**. Therefore each high –k dielectric materials can not be used as a gate dielectric for TFTs. Also, the

selection of high-k dielectric need to fulfills a few more important properties for using in TFT which are discussed below.[64]

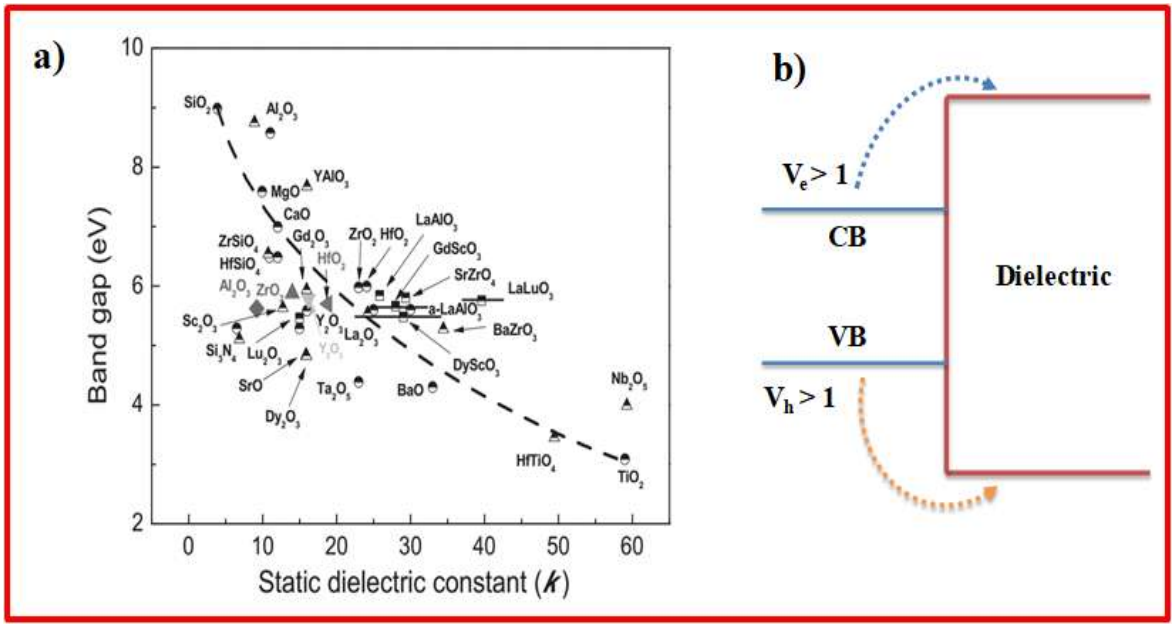

Figure 1.7: a) *A relation dielectric constant versus measured bandgap of the various metal oxide dielectric[65]* ***b)*** *schematic diagram of band offset determining carrier injection in oxide band offset V_e and V_h indicate the potential barriers for electrons and holes, CB and VB are conduction and valence bands for channel and dielectric layers.*

1.8 Choice of high-k dielectric for low operating voltage TFT

In this context, apart from the high-k, gate insulators of as TFT should have some other properties, e.g., smooth surface, low leakage current, high breakdown field etc. Apart from them, kinetic stability, cost (depending on synthetic complexity), material toxicity should also be considered for good insulator selection.[66, 67] The criteria to select the gate dielectrics for low operating voltage TFT are summarized in **figure 1.8**. The key factors for the best gate dielectric for TFT fabrication are six-fold as given below.[64]

1. **High permittivity:** The primary key factor is the high dielectric constant. High-k offers larger film thickness with the high capacitance density which reduces the leakage current of the device.

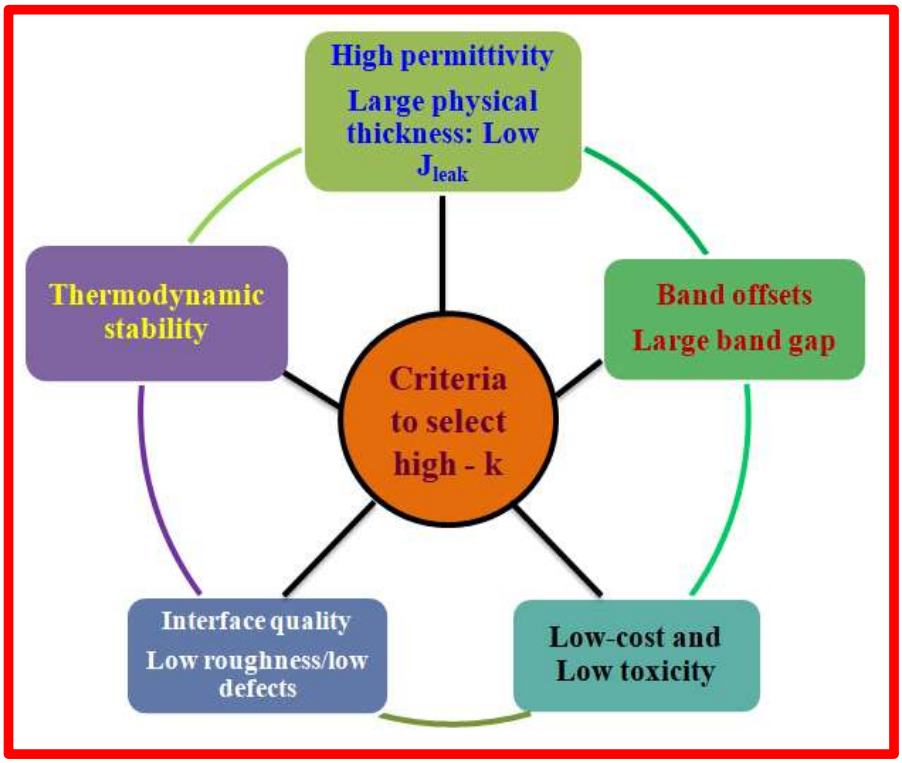

Figure 1.8: *Criteria to choose the high-k dielectric for a thin film transistor.*

2. **Thermodynamic stability:** The second necessity of dielectric is thermodynamic stability. The metal oxide dielectric is in direct contact with the active channel, so it must not react with it.

3. **Kinetic stability:** It must be kinetically stable, and be compatible with semiconductor processing temperature that may go up to 1000 ^{o}C.

4. **Band offsets:** High-k insulators must act as a gate dielectric exhibiting band offsets of more than 1 eV with respect to the semiconductor to diminish charge injection into its bands. The band offsets of the insulator valence band maximum (VBM) and the conduction band minimum (CBM) in p-type and n-type semiconductor must be greater than that of 1 eV relative to those of the TFT maintating low leakage Schottky emission.[67]

5. **Interface quality**: Since dielectric materials have direct contact with channel semiconductors, which form a better electrical interface with it. Typically, TFT is the sandwiched device of dielectric between the gate electrode and the semiconductor layer. Thus for the growth of a semiconductor on the dielectric, the interface of dielectric and gate electrode (Si substrate) must stable and pure.

6. **Defects:** Surface of the dielectric thin film must be with very low defect density to achieve high-performance of the devices. An ideal dielectric should have a smooth surface to avoid unwanted scattering of the carrier that reduces the effective mobility of the device.

1.9 Metal oxide semiconductor

High mobility semiconductor is not the most severe design criterion and single-crystal silicon is not the leading semiconductor material for large-area electronics application due to the high cost of fabrication. Relatively lower cost polycrystalline or amorphous silicon semiconductor, oxide semiconductors (polycrystalline and amorphous) and organic semiconductors are more favored options for large-area electronics applications.[68, 69] Among them, oxide semiconductors, particularly the amorphous ones, are potential candidates as a transparent semiconductor for TFT materials that have made a remarkable development mainly in display applications[70] that doesn’t require a very long

lifetime.[71] The unique features of metal oxide semiconductor with respect to realistic application are their outstanding stability against environment and thermal budget, superior visual transparency and promising for film processing at relatively low-temperature. The investigation of transparent conductive oxides (TCOs) around sixty years ago, in 1954, In_2O_3:Sn (ITO) was published as the first TCO material, after SnO_2 and ZnO.[72] Apart from the conventional applications of challenging silicon, this opens new pathways for fully non hazardous fields like paper electronics.[73, 74] Besides that, the grain boundaries are absent in the amorphous oxide semiconductor, thereby discarding the prime constraint of mobility in semiconductor materials of polycrystalline nature, which is a huge benefit for process integration and especially for large area application. At the same time, there are other advantages including film deposition routes at low-temperature facilitating ultra-smooth surfaces that greatly suppress the traps at interface and minimize the concentration of scattering centers. In addition, such emerging advanced new technologies offer excellent platforms for real solutions and can help to overcome many practical difficulties and limitations contained in the traditional silicon based technology utilizing materials that are itself known to be non-toxic, non-hazardous and much cost effective. Amorphous oxides semiconductor (AOS) consists of post-transition metal cations with $(n-1)d^{10}ns^0$, where $n>4$, electronic configurations represent an appealing subclass of transparent semiconductors, while they acquire comparatively higher charge carrier mobilities even with their amorphous nature. Specifically, between conventional amorphous silicon and amorphous chalcogenides, AOS preserve high mobility in the amorphous state because of its unique band structure. Highly directional sp^3 hybrid orbital in silicon give rises to valence band and conduction band. In single crystalline silicon, extremely high charge carrier mobility

(>1000 cm^2/Vs) is ascribe to the huge overlap of sp^3 orbital and large conduction band spreading in the periodic single crystal structure. Nevertheless, a little overlap of sp^3 orbital in amorphous silicon restricts the spreading of the conduction band and thereby limits the mobility less than 1 cm^2/Vs.. The CBM can possibly create effective pathways that conduct the free electron in AOS materials, which is collected at empty s-states of the metal cation. The more spatial area than inter-cation distances of s states represents that AOS exhibits the electron mobility due to that of the crystalline phase.[71, 75, 76] The principal quantum number n controlls the spatial overlap of the s state, therefore transition metal ions with electronic configuration $(n–1)d^{10}ns^0$, where n>4, are most suitable candidates for AOS. Among p block indium (In) and Tin (Sn) having same electronic configuration $[Kr](4d)^{10}(5s)^0$ also assemble this condition. Because of the small interaction distances, ZnO possesses CBM which is extremely dispersive in nature.[76, 77] The notable enhancement in amorphous character is achieved due to mixing of cations having dissimilar size [78] thereby inducing the formation of stable amorphous phases in both binary and ternary AOS materials.

Conduction of hole in metal oxide is influenced by the more dispersion in VBM or effective mass of hole that needs to be smaller. Currently, significant attention has been paid to Cu(I) based compounds including copper oxide Cu_2O, delafossites $CuMO_2$ (M = Al, Ga, or In), and oxychalcogenides (LaCuOCh (Ch = S, Se, or Te)).[79, 80] A striking feature in these Cu compounds is their contribution of the 3d state close to VBM, which is against to common n-type metal oxides leading to smaller hole effective mass (value shown in **table 1.1** for Cu_2O) with enhanced hole transport properties. Another currently investigated and most fascinating candidate is stannous oxide SnO, where the hybridization

involving 5s orbital of Sn and 2p of O in valence band leads to better p-type conductivity.[81] Due to this typical characteristic, both Cu_2O and SnO have been successfully employed in thin-film transistors and logic circuits.[82, 83]

Table 1.1: *Typical electrical and optical properties of ZnO, In_2O_3 and SnO_2 thin films[84]*

Oxide	Optical bandgap (eV)	Effective mass[a] (in units of free electron mass, m_o) Electron	Hole
n-Type			
ZnO	3.41	$m_e = 0.24$	$m_{h\perp} = 0.8$ $m_{h\parallel} = 5$
In_2O_3	3.38	$m_e = 0.3$	N/A
SnO_2	3.50	$m_{e\perp} = 0.30$ $m_{e\parallel} = 0.23$	$m_{h\perp} = 3.3$ $m_{h\parallel} = 2.3$
p-Type			
Cu_2O	2.17	$m_e = 0.99$	$m_{lh} = 0.58$
SnO	2.7[b]	N/A	N/A
CuSCN[c]	3.9[d]	$m_{e\perp} = 2$ $m_{e\parallel} = 1$	$m_{lh\perp} = 0.5$ $m_{lh\parallel} = 0.8$

Just like in case of solids, the band structures of metal oxides precisely determine by analyzing their electronic properties. Yet the interaction between the orbit of metal and oxygen leads to the highly perplexed structure along with significant inequality between the hole and electron conduction in a given system. For a covalent semiconductor like Si, the conduction band minimum and valance band maxima are attributed the antibonding (sp^3 s*) and bonding (sp^3 s) hybrid orbital of silicon. Thus the bandgap is the difference between the two energy states (σ*–σ).[71, 85] In contrast to this, the metal oxide semiconductor is valence compounds, possessing higher ionic character in their chemical bonds. This ionicity is responsible for the electronic structure which differs from the covalent semiconductor.

Usually for binary and ternary semiconducting metal oxides discussed in literature namely In_2O_3, SnO_2, ZnO, IZO and IGZO, where the formation of CBM and VBM is attributed from the ns orbital of metal and 2p orbital of oxygen respectively, also leads to more dispersive CBM and a localized VBM.[84, 86] This results in smaller effective mass of the electron and thus better electron transport as compared to hole transport. This is the principal cause for predominant n-type conductivity observed in the majority of metal oxide semiconductors so far reported. Values of effective masses of electron and hole of different AOSs reported in the literature are given in **table 1.1**.[84, 87-90] ZnO has a direct bandgap of 3.4 eV, which can be tuned by substitutional doping on the cation site and possess three crystal structures: wurtzite, zincblend, and rocksalt.[91-93] Among them, wurtzite is the most stable structure at ambient conditions. In_2O_3 crystallizes in the cubic structure with a lattice constant of ~10.12 Å.[91, 94] Though, an amorphous nature of the film is achieved at low processing temperatures which depend upon the deposition parameters, they readily possess the cubic symmetry after annealing at around 150 °C.[88, 95, 96] In_2O_3 is capable of absorbing incident light through both an indirect and direct interband transitions. Following this, the bandgap, E_g of ~2.7 and 3.5–3.7 eV is estimated for indirect and direct electronic transitions, respectively.[96, 97] The typical electrical and optical properties of ZnO and In_2O_3 thin films, with SnO_2 are listed in **table 1.1**.

The **figure 1.9** lists 15 d-block transition elements with $(n\text{-}l)d^{10}ns^0$ ($n\geq4$) configuration.[98] Among them, Ag, Au, and Ge are costly metals while Cd, Hg, Tl, Pb, and As are not used in AOS application due to their high toxicity. Typically, Cu successfully used as a p-type semiconductor. In the remaining six elements, Zn, Ga, In and Sn are the most commonly used in AOS. Indium-based amorphous oxides, including IGZO and IZO, show better

electrical properties even with low-temperature processing. In IZO and GIZO, In^{3+} cations are the key elements of the CBM, like in In_2O_3, but the doping of Zn (and Ga) in considerable concentrations prevent the crystallization process in In_2O_3.

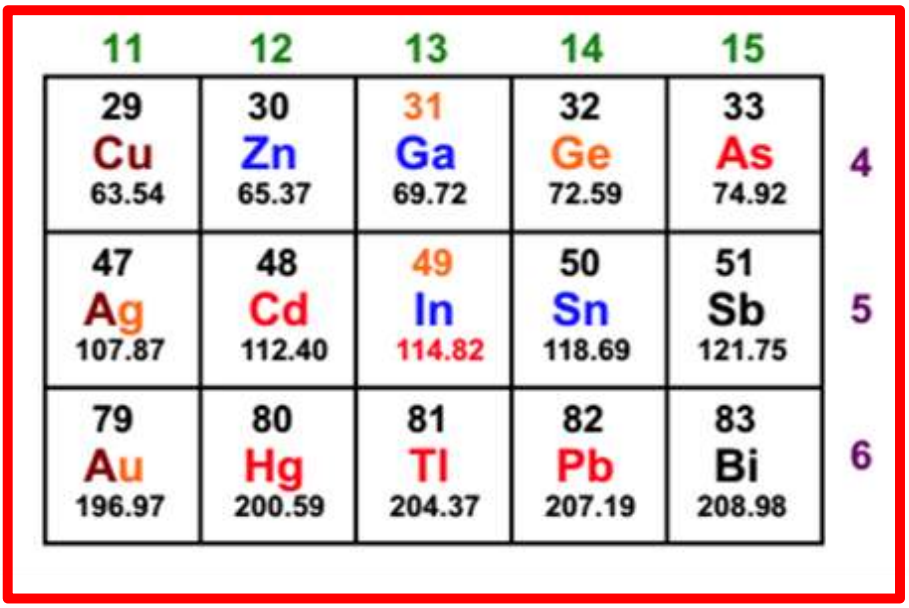

Figure 1.9: *d block metal elements with (n-l)$d^{10}ns^0$(n≥4) configuration.[98]*

1.10 Solution processing low operating voltage TFT

As mentioned earlier, most vacuum based techniques need long processing time for high vacuum environment for good quality film deposition that requires more preliminary (instruments) setup expenditure. In general, there is an addition of requirement of post-annealing treatment at high thermal budget which complete the densification process for the film. Due to such drawbacks, these techniques are not appropriate for material deposition onto flexible type substrates with large-area and great scalability. Thus, it is apparent that traditional vacuum-based deposition techniques call for more efficient alternate methods in the near future. This can provide excellent compliance to the large-

area requirement and flexible electronic gadgets developed by employing processes which are inexpensive and capable for mass production at industrial scale.[99] Therefore, it is urgently required to develop solution based printable technique, like sol-gel process, for low-cost mass production. The advantages of sol-gel processed oxide have been summarized in **figure 1.10 a)**[30, 67, 100]

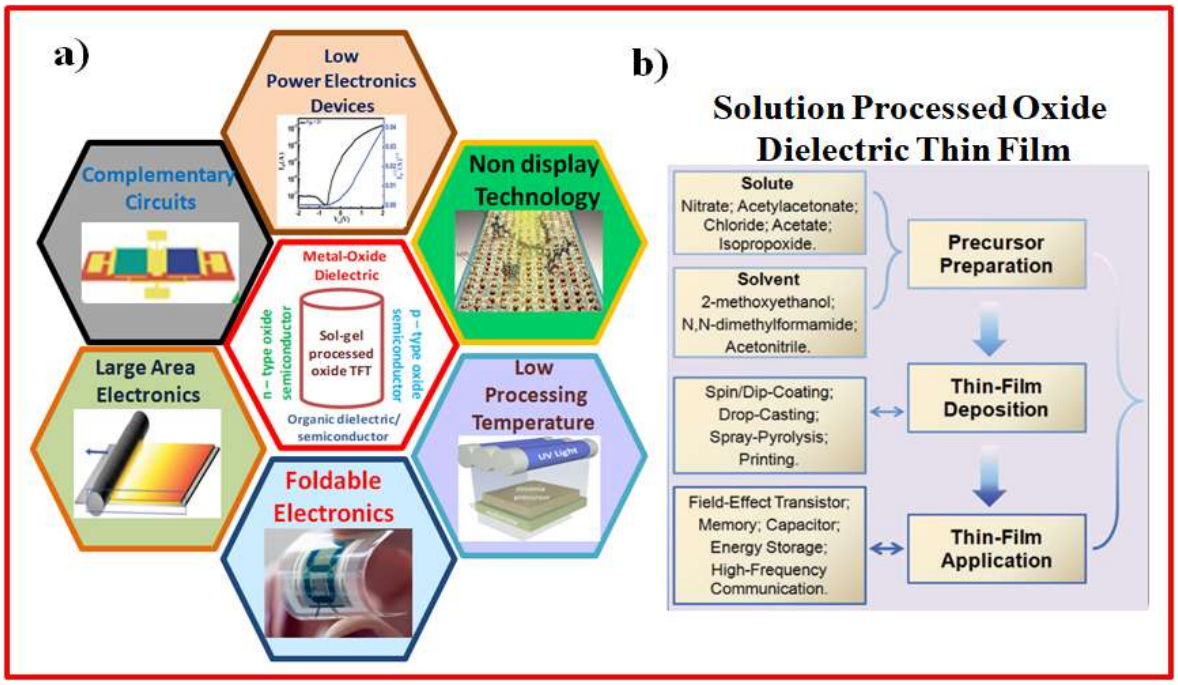

Figure 1.10: *Schematic diagram of the **a)** application of sol-gel metal oxide for thin film device application **b)** process flow chart for solution-processed thin film deposition.[67]*

Solution-based processing **(figure 1.10 b))** has recently alleviated the quick development of film deposition techniques. Consequently, inexpensive and high throughput solution processed methods has emerged as a subject of continuing research focusing academic as well as several industrial fields (**figure 1.10).** Using Solution-based fabrication technique; it is possible to reduce the manufacturing cost and fabrication time instead of vacuum deposition processes and to replace them with printable precursor materials. Both high-κ

oxide and AOSs thin films can be deposited in several ways by sol-gel routes, like spin coating, dip coating, spray pyrolysis, drop casting, inkjet printing, screen printing, chemical bath deposition, doctor blade coating, aerosol jet and various printing method.[101, 102] Each and every deposition method exhibits own benefits and drawbacks, as well as ease of operation, precursor synthesis, throughput competence and suitability for roll to roll (R2R) process **(Table 1.2)**.[102-105]

Table 1.2: *Comparison of film deposition techniques using printing and coating[67]*

Technique	**Spin**	**Spray**	**Bar**	**Ink-jet**	**Screen**	**Gravure**
Ink preparation	Simple	Moderate	Simple	Moderate	Demanding	Difficult
Ink waste	Significant	Considerable	Little	None	None	Significant
Speed	–	Fast	Medium	Medium	Fast	Very fast
Noncontact processability	Yes	Yes	No	Yes	Yes	No
R2R compatible	No	Yes	Yes	Yes	Yes	Yes

In a typical sol-gel method the precursors i.e. metal alkoxides ($M\text{-}(OR)_z$) and metal salts i.e. chloride, acetates, sulfides, nitrates are dissolved in alcohol or aqueous solvent. Metal alkoxides and derivatives of alcohols are the well-liked precursors for solution processed because of some marvelous properties e.g. appropriate solubility in organic solvents with superior tendency to produce metal oxides due to well suited chemical reactivity including facile purification process.[106] In spite of, this metal alkoxides are generally costly and comparatively hard to control since they are chemically more reactive leading to short shelf-life. Metal acetates are also widely used (like acetates or other metal carboxylates) because of their unique properties, i.e., easily soluble in many solvents and low-cost,

stable, environment-friendly and non-hazardous.[107, 108] After treating with the solvent (e.g., H_2O or ROH) molecules, the metal cations lose a proton due to hydrolysis reaction which eventually form metal hydroxides depicted in **figure 1.11**. Formation of M-O-M polymeric framework followed by the condensation reaction via an oxolation among metal hydroxides is depicted in **figure 1.11**. Depending upon the reaction temperature, time, pH, and catalyst, three different kinds of products are obtained from the sol-gel route such as sol, gel, and nanoparticles shown in **figure 1.12**. In order to obtain the oxide thin film, the precursor solution is coated followed by post-annealing treatment which (1) forms M−O−M structure completing condensation process, (2) eliminate the residues and impurities of secondary products and organic solvents via thermal decomposition and (3) produce a dense oxide film diminishing unwanted voids in the film (densification process).[109]

Solution processed metal oxide dielectrics allow to deposit films of low surface roughness by reducing defect states. These factors are pivotal which guarantees the suitable electrical insulation maintaining its high-k value. In this technological background, solution processed metal oxides are the emerging materials considered for extensive investigation for their implementation as a multifold device building block i.e. low voltage TFT in materials research and technology. Specifically, low operating voltage oxide TFTs have attracted significant research interest as a prospective materials for active matrix light emitting diode (AMLED), flat panel display (FPD), optoelectronic applications including light emitting transistors and phototransistors.[110-114]

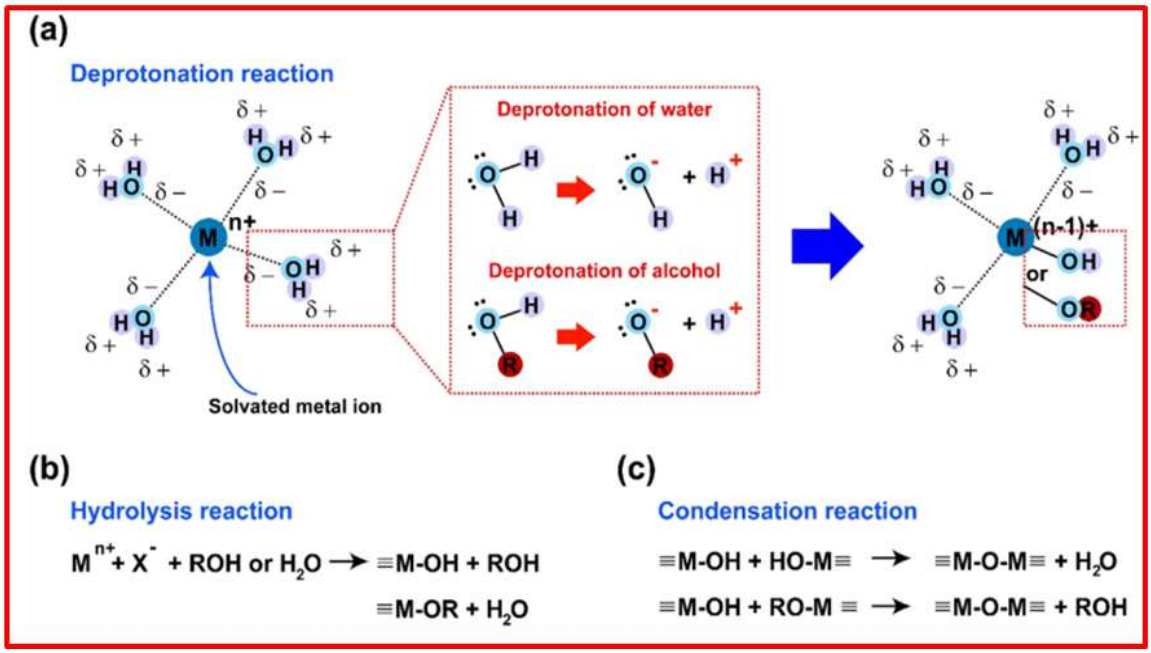

Figure 1.11: *Steps of sol-gel chemical reaction* ***a)*** *an illustration of deprotonation reaction between metal ions and solvent (H_2O or alcohol) molecules to metal hydroxides. Typical reactions for* ***b)*** *hydrolysis and* ***c)*** *condensation.[30, 100]*

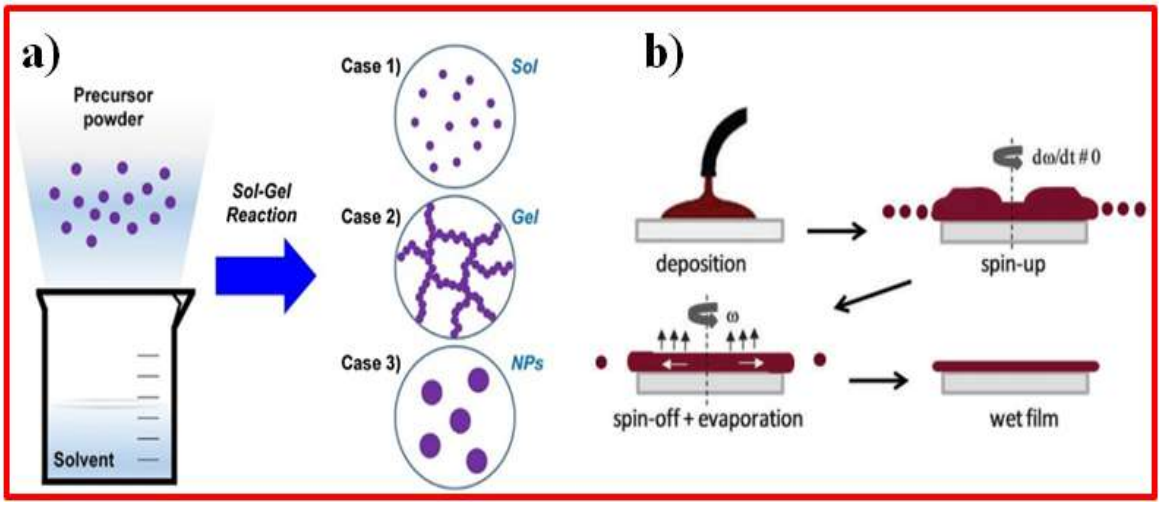

Figure 1.12: *schematic of deposition of solution processed metal oxide thin films* ***a)*** *different kinds of final products such as sol, gel, and nanoparticles* ***b)*** *a representation for densification of sol-gel thin film using high-temperature annealing.[30]*

Additionally, operation at low voltage renders great feasibility for portable electronics e.g, mobiles, electronic tablets, laptops, etc those work at low power. Many research groups gave considerable effort for the development of low voltage metal oxide TFT by sol-gel route. As discussed in the dielectric section most binary oxide e.g., HfO_2, TiO_2 Al_2O_3, ZrO_2 based TFT has been reported for the improvement of the low voltage metal oxide TFT.[115-125] A summary has been given in **table 1.3** on different solution processed oxide gate dielectric that has been used as a gate dielectric of TFT.[30, 62, 63, 126, 127] For the deployment in practical applications, a low-voltage operated oxide TFTs are the most suited which necessarily strive to develop new and more efficient gate insulating material with higher areal capacitance. Recently, low power consuming oxide TFTs have been revolutionized by means of sol-gel prepared inorganic high-k dielectrics. However, as suggested earlier, high κ oxides undergo from a compromise between κ and E_g **(Figure 1.7 a))**. For low voltage and high performance TFT one must choose materials having appropriate high κ as well as large E_g. A number of strategies have been developed to remove these issues including i.e., ionic liquids[54, 128-130], ion-gel[48, 131, 132], polyelectrolytes[22, 53, 133] and self-assembled monolayer (SAM),[134-136]. Nevertheless, all such types of dielectrics do not offer a good replacement for sol gel prepared low voltage oxide TFT fabrication due to incompatibility at high annealing temperature when the oxide semiconductor layer is deposited. In contrast, inorganic dielectrics are broadly used for this purpose due to their better stability during the high-temperature treatment. Multi-component and multilayered inorganic dielectrics consolidated high κ and large E_g into the same gate dielectric **(table 1.4)**.[137-143] This inorganic dielectric provides the excellent interface between the dielectric and

semiconductor which is an essential requirement for TFT fabrication maintaining the high-performance with low-voltage.

Table 1.3: *Performance of the sol-gel coated binary oxide dielectric based TFT[30, 67]*

Dielectric[a]	Coating method[b]	Process Temp. (°C)	*d* (nm)	*C* (nF cm^{-2})	*k*	E_b (MV cm^{-1})	Semiconductor	Maximum mobility (cm^{2}V^{-1}s^{-1})	On/off ratio
ZircSOx HafSOx	SC	325	150 ~ 300	-	9 ~ 12	~6	IZO	1	~10^6
ZrOx	SC	300	149	-	10	-	CdS	~48	~10^5
ZrOx	SP	450	~98	126	~14	~1.6	ZnO:Li	~85	~10^6
ZrOx	SC	150 (UV)	5	~830	8.79	~18	ZnO	0.45	~10^5
ZrOx	SC	300	35	~240	24.5	-	ZTO	4	~10^5
ZrOx	SC	400	100	-	-	-	SnO	~100	~10^5
ZrOx:B	SC	250	100	-	12.1	~3.94	InO	39.3	~10^7
ZrOx	SC	350	210	-	14.8	~2.8	IZO	7.21	~10^6
ZrOx	SC	500	90	~240	-	-	ZTO	~10	~10^9
ZrOx	SC	300	-	426	12.5	7.2	InO	23	~10^7
ZrOx	SC	300	54.2	369	22.6	>2	InO	1.6	~10^4
ZrOx	SC	450	<100	108.7	19.1	3.2	ITZO/IGZO	40	~10^6
ZrOx	IJ	500	~60	-	22	4	SnO	11	~10^6
ZrOx	SC	250	20	502	13	>5	IZO	75	~10^4
ZrOx	SC	350	45	255	-	-	IZO	93.4	~10^5
ZrOx	SCS	350	25	370	14.3	9.5	IGZO	28.5	~10^5
HfOx	SC	400	~120	-	~13	~5.5	IGZO	13.1	~10^7
HfOx	SC	300	65	~190	~14	-	ZTO	1.05	~10^5
HfOx	SC	450	100	155	18.5	>2.5	ZnO	42	~10^5
HfOx	SC	385	16	409	11	-	-	-	-
YOx	SC	400	-	134.1	16.2	~1.8	ZnO	34	~10^4
YOx	SC	300	59.2	380	25.4	>2	IZO	0.1	~10^2
YOx	SC	300	20	360	14.8	4	IZO	25.9	~10^6
YOx	SC	350	17	448	16.5	>5	InO	15.9	~10^6
YOx	SC	400	22.7	345.7	8.85	3.5	IZO	20.9	~10^6
GdOx	SC	500	100	146	9 ~ 14	~3.5	ITZO	~1.9	~10^3
GdOx	SC	400	100	-	10 ~ 12	~3.5	ZTO	~2.53	~10^5
GaOx	SC	250	52	172	10.1	>2.5	InO	4.1	~10^5

Recently, Pal et al. developed first time a new sodium beta-alumina (SBA) a solid electrolyte thin film via cost-effective solution processed technique and it's successfully employed as a gate insulator material for the fabrication of low voltage TFT. **Figure 1.13 a) and b)** illustrate the structures of SBA, which is ion (Li^+, Na^+, and K^+) incorporated into alumina dielectrics. This 75-nm-thick SBA insulator film exhibited high areal capacitance of 2μF/cm^2 because of ionic movement with very low leakage current.[55] The deposited dielectric thin film showed a very high k value of 170 and a reasonably high E_b of 5.3 MV cm^{-1}.

Table 1.4: *The summary of TFT parameters for spin-coated multicomponent or multilayered oxide dielectrics[30]*

Dielectric	Temperature [°C]	d [nm]	C_i [nF cm^{-2}]	κ	E_b [MV cm^{-1}]	Channel	μ_{FE} [cm^2 V^{-1} s^{-1}]	I_{on}/I_{off}
$HfSO_x$:La	325	192	–	9–12	4–6	IZO	1	≈10^7
AlPO (2:1)	800	155	–	4.8	≈5	ZnO	3.5	≈10^6
AlNaO (11:1)	600	75	2000	170	5.3	ZTO	28	≈10^4
YHfZnO	600	235	61.7	16.4	2.68	IGZO	0.29	≈10^5
AlPO (2:1)	300	180	–	5.2	≈6	IGZO	4.5	≈10^9
TaSrO (2:1)	700	100	–	36	–	IZO	0.24	5×10^6
ZrO_2:B	250	100	–	12.1	≈4	In_2O_3	39.3	≈10^7
AlZrO (9:1)	350	95	110	11.8	–	IZO	≈53	≈10^6
HfLaO (1:1)	500	60	178	22	≈5	ZnO	1.6	10^6
AlZrO (2:1)	400	133	131	19.7	–	IHZO	18.1	10^7
MgTiO (3:2)	500	180	≈85	17.2	–	IZO	3.41	6×10^6
LaAlO (1:1)	600	100	≈100	11.5	>4	IGZO	11.1	≈10^6
AlZrO (19:1)	150	≈35	≈180	≈7.3	>7	IGZO	7.71	2×10^5
HfSiO (2:1)	500	105	91	10.8	2.9	ZTO	153	3×10^7
AlZrO (2:1)	500	60	123	8.3	–	ZTO	37	≈10^6
AlLaO (4:1)	200	92	128	9	>4	In_2O_3	≈5	≈10^6
AlYO (1:3)	400	37	443	19.5	≈5	IZO	52.9	≈10^6
HfO_x/AlO_x	400	85	≈150	–	–	ZTO	3.84	≈10^5
ZrO_x/AlO_x	180	≈35	≈235	≈9	–	ZnO	11	≈10^4
TiO_x/AlPO	350	150	–	8	>3.5	IGZO	3.2	≈10^5
ZrO/AlO/ZrO	350	250	45.8	14.8	≈3.4	IZO	3.27	≈10^7
LaTaO/BiNbO	550	190	–	90	–	IGZO	0.49	≈10^7
$LaZrO_x/SiO_2$	180	188	25	–	–	IZO	24.8	4×10^7
ZrO_2/Al_2O_3	150	39	279	12.3	8	ZnO	1.37	4×10^6
AlO/ZrO/AlO	350	61	95.6	–	2.42	IZO	4.51	5×10^5
Al_2O_3/ZrO_2	≈150	49	115	8.53	–	IGZO	12.85	≈10^8

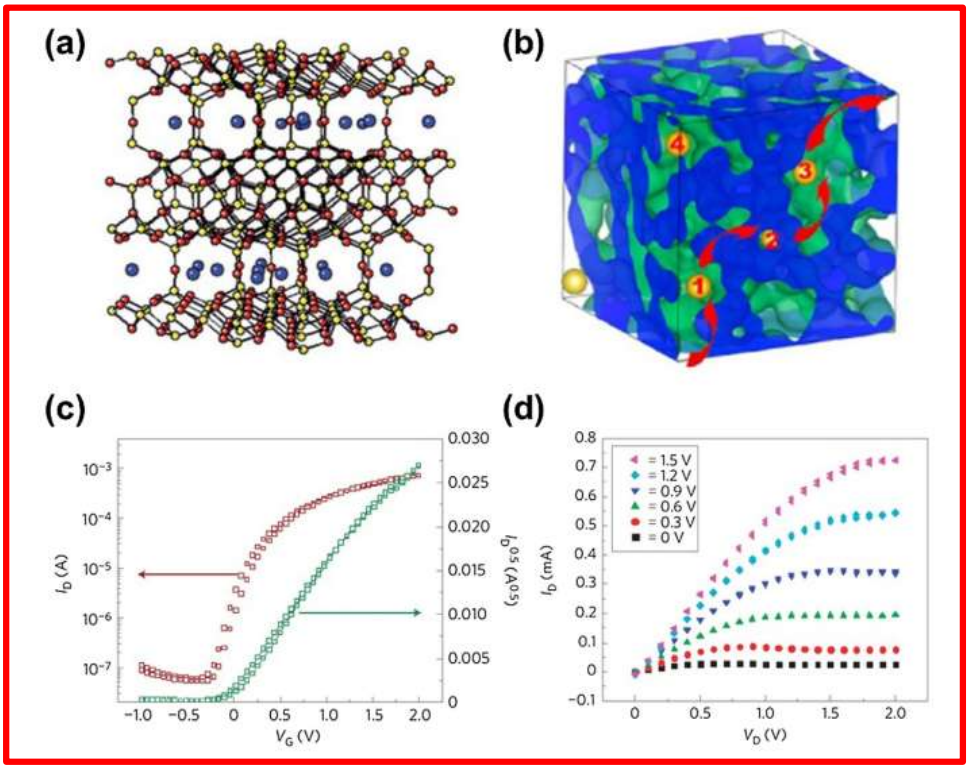

Figure 1.13: *Solution-processed ion conducting metal oxide thin film transistor* ***a)*** *crystal structure of SBA dielectric Na^+ ion is denoted by blue dot and red and yellow color represents oxygen and aluminum atoms respectively* ***b)*** *a proposed ionic path inside the dielectric* ***c)*** *transfer and* ***d)*** *output characteristics of ZTO transistor with sol-gel coated SBA dielectric based TFT.[30]*

This high capacitance was ascribed to the substantial improvement in polarization realized by displacement of alkali dopant ion when subjected to electric field keeping the low leakage current by the hindrance of electron transportation within the dielectric lattice. The output and transfer characteristics are depicted in **figure 1.13 c) and d).** These characteristics show that SBA is a good alternate gate dielectric for the low voltage TFT with high mobility and moderate On/Off ratio.[55, 67] Among the different types of gate dielectrics for metal oxide TFT applications, ion conducting SBA and its related dielectrics show the highest performance. Fabrication of this class of dielectrics is possible with a low-cost solution processing technique like spin or dip coating followed by an annealing

step.[56, 57] However, the sodium beta-alumina (SBA) class of materials requires a very high annealing temperature (830 ^{o}C), limiting the accessibility of substrate materials. In order to overcome this issue, in this thesis work, we have searched new ion-conducting dielectrics which have lower crystallization temperature maintaining the high mobility, high on/off ratio and most important by low operating voltage.

1.11 Scope and objective of present work

From the above discussion of introduction, metal-oxide TFT has been widely considered for different applications including active-matrix light-emitting diodes (AMLEDs), light emitting transistors, photodetectors, biosensors arrays etc, due to their outstanding transport properties. These metal oxide TFTs demonstrate reasonably high mobility, high on/off ratio, excellent thermal and chemical stability which are the crucial requirements for practical uses. However, due to the low dielectric constant (k) of conventional SiO_2 gate dielectric, most of these TFTs require high operating voltages (≥40V) which is commonly used for metal oxide TFT, limiting its application to portable low power electronics. Additionally, it has been established that high-k polarization behavior of dielectric especially binary oxide dielectric materials and its thin film have been studied extensively as gate dielectric materials in thin film transistor which provides low power consumption. In this area, Pal et. al. first demonstrated a novel strategy to develop dielectric material with enhanced ‘k’ value after incorporating ionic dopants into oxide lattices. SBA is the first ion conducting dielectric that successfully used as a gate insulator in low voltage TFTs. However, ion-conducting behavior of dielectric materials in TFT and the effect of lithium ion in metal oxide are rarely available in the literature. We introduce here two new Li^{+} containing ion-conducting insulators and successfully used as a gate dielectric in low

voltage TFT. These dielectrics exhibited crystalline nature at much lower processing temperature and displayed higher performance of TFTs. Hence, the central objective of the present thesis is to synthesize the ion conducting dielectric through a cost-effective sol-gel process. Additionally, using this ion conducting dielectric with bilayer device structure, one can enhance the device performance i.e. improved subthreshold swing, least interface states, high on/off ratio and most important lowering the operating voltage. Overall, the thesis provides an overview of the development of the ion conducting materials as a gate dielectric for the high-performance and low voltage TFT via a cost-effective sol-gel route. On the basis of above discussion given in this chapter, the thesis is divided in to main objectives comprising these chapters:

Chapter 2 discusses the synthesis of dielectric and semiconductor through the cost-effective solution process. The thin film of dielectric and semiconductor is fabricated by spin coater and used as a gate dielectric in TFTs. In addition, materials and device characterization techniques are explained in this chapter.

Chapter 3 describes the synthesis of Li_5AlO_4 by solution processed technique and its application as a gate dielectric of a metal-oxide TFT. The high dielectric constant (k) of the insulator Li_5AlO_4 has been achieved by utilizing the improved capacitance contributed by the mobile lithium ion (Li^+) within the dielectric film. Li_5AlO_4, a well-known material for solid state electrolyte application, has never been considered hitherto as a gate dielectric of metal oxide thin film transistor (TFT). We have synthesized this dielectric by cost-effective sol-gel method followed by a low-temperature annealing process yielding three phases such as amorphous-Li_5AlO_4 (a- Li_5AlO_4), α-Li_5AlO_4, and β-Li_5AlO_4 at different annealing conditions. The optimized TFTs fabricated with all of these three phases of Li_5AlO_4 on top

of highly doped silicon (p^{++}-Si) wafer and a solution processed semiconducting layer of indium zinc oxide (IZO) exhibit an excellent TFT performance at the operating voltage of 2V. Among all of these three different types of TFTs, the device with α-Li_5AlO_4 gate dielectric annealed at 500 ^oC shows the best device performance with an on/off ratio of 5x 10^4 and electron mobility of 21.9 $cm^2\ V^{-1}\ s^{-1}$. In addition, this device requires a least drain voltage of <2V to reach the saturation drain current due to higher Li^+ mobility of α-Li_5AlO_4 gate dielectric. Metal oxide/quantum dot heterojunction phototransistor fabricated by coating IZO TFT with colloidal lead sulfide (PbS) quantum dot shows the responsivity and the response time of 4.5 $x10^{-4}$A/W and 2.2 sec respectively.

In chapter 4 we describe the sol-gel synthesis of ion-conducting $LiAlO_2$ insulator and its application as a gate dielectric of ultra-low voltage (≤1.0 V) indium-zinc-oxide (IZO) thin film transistor (TFT). This $LiAlO_2$ dielectric has two distinct phases of α- and γ-. These α-$LiAlO_2$ and γ-$LiAlO_2$ phases those have been grown at two different processing temperatures. For both phases, mobile Li^+-ion is responsible to achieve a high dielectric constant (k) of the material that helps to reduce the operating voltage of TFT. Additionally, the lower surface roughness of $LiAlO_2$ thin film creates a low-density trap state in the semiconductor/dielectric interface which is capable to reduce operating voltage within 1.0-volt. The most interesting achievement of this work is the development of 1.0-volt operation voltage TFT by using 350 ^oC annealed α-$LiAlO_2$ dielectric. Besides, the device with 700 ^oC annealed γ-$LiAlO_2$ gate dielectric shows the best device performance with high electron mobility and on/off ratio of 3 x 10^5. Instead, 350 ^oC annealed α-$LiAlO_2$ dielectric require only one volt to saturate the drain current and shows its mobility and on/off ratio are 13.5 $cm^2\ V^{-1}\ s^{-1}$ and 1 x 10^4 respectively. Such kind of unusually low

operation voltage TFT fabrication becomes possible because of the higher Li^+ mobility of α-$LiAlO_2$ gate dielectric and very low surface trap density. A model on the carrier transport mechanism has been proposed to explain this achievement.

In chapter 5, a new method of high-performance solution-processed one-volt metal oxide thin film transistor (TFT) fabrication has been described. For this achievement, metal oxide TFT has been fabricated onto highly p-doped silicon (p^{++}-Si) substrate with sol-gel derived ion-conducting gate dielectric by electron donating TiO_2 gate interface. Comparative electrical characterization of two different TFTs with TiO_2 and Al_2O_3 gate interface device reveals that n-type TiO_2 works as an electron donor to the semiconductor/dielectric interface trap state. As a consequence, sub-threshold swing (SS) of the TiO_2 interface device reduces significantly by keeping threshold voltage closer to zero, enabling to achieve significantly high-performance one-volt TFT with respect to 'without TiO_2' and 'with Al_2O_3' interface devices. Additionally, the depleted layer of p^{++}-Si (111)/TiO_2 interface reduces gate leakage current significantly that helps to improve the on/off ratio of the device. Specifically, in this report, one-volt TFT with indium zinc oxide semiconductor has been fabricated using Li_5AlO_4 dielectric with TiO_2 gate interface that achieved electron mobility of 32 cm^2/V.s with on/off ratio of 5×10^5 and sub-threshold swing of 110 mV/dec. This investigation provides a feasible direction towards the development of high-performance and low voltage TFT fabrication with various material combinations.

Finally, chapter 6 is committed to sum up the major findings of the thesis. In the end, the future scopes of works related to the present thesis have been briefly outlined.