Chapter 5

Three level Z source ultra sparse matrix converter

5.1 Introduction

Standard matrix converter topologies produces two level outputs. Even though matrix converters are known to produce low THD at the input terminals but it delivers two level output voltage which is similar to the standard two level inverter. To improve output THD characteristics for matrix converters, researchers gave a direction to imbibe the multi level behaviour in matrix converters which resulted in multi level matrix converters concept [53] [54], [55]. In addition, lower voltage stress, better EMI and $\frac{dv}{dt}$ are other benefits at the cost of complexity and number of switches. Standard multilevel inverters have various types reported in literature such as flying capacitor (FC), neutral point clamped (NPC) and cascaded multilevel inverter (CMLI). Among the reported multi level topologies, NPC better suits to be cascaded with current source rectifier to form multi level matrix converter. To reduce the number of switches another 3 level matrix converter topology is reported in literature [54]. Although multilevel matrix converters as an AC-AC converter have attractive properties, but it has low voltage transfer ratio. To resolve this issue Z-source based multilevel matrix converters are evolved. In this chapter three level Z-source based matrix converter is proposed with reduced switching devices.

5.2 Proposed topology

The proposed topology is derived from three level Z-source NPC [56] and two cascaded DC link inverters [57]. Three level Z source NPC consists of Z source impedance network connected between diode bridge rectifier and three level neutral point clamped inverter which has benefit of boosting three level output voltage using reduced passive elements. On the other hand, two cascaded DC link topology consist of two 2 level DC link inverters connected such that they produce three level output voltage with the reduction of six diodes as compared to three level neutral point clamped inverter. By combining these two concepts with current source rectifier results in two configurations as shown in Figure.5.1 and Figure.5.2. Rectifier section of proposed converter is realised with unidirectional current source rectifier. Inverter section of proposed converter is realised with two 2-level voltage source inverters with one VSI DC link connected at the output terminals of another VSI. With this approach, six clamping diodes are reduced, compared to other existing topologies. The major difference between the two configurations is placement of output load terminals. Placement of load terminals closest to either positive or negative DC link terminals will impose twice voltage across certain set of top/bottom switches. In case of configuration 1 (Figure.5.1) top switches $S1, S5, S9$ while in configuration 2 (Figure.5.2) bottom switches $S4, S8, S12$ have to bear twice voltage.

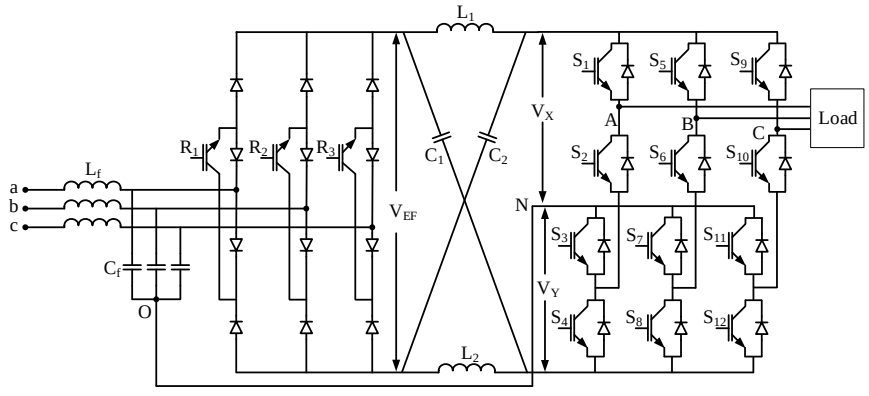

Figure 5.1: Configuration 1

Operation of proposed converter is divided into three modes namely non-shoot through mode, upper shoot through mode and lower shoot through mode. Operating modes explanation below is restricted to configuration 1.

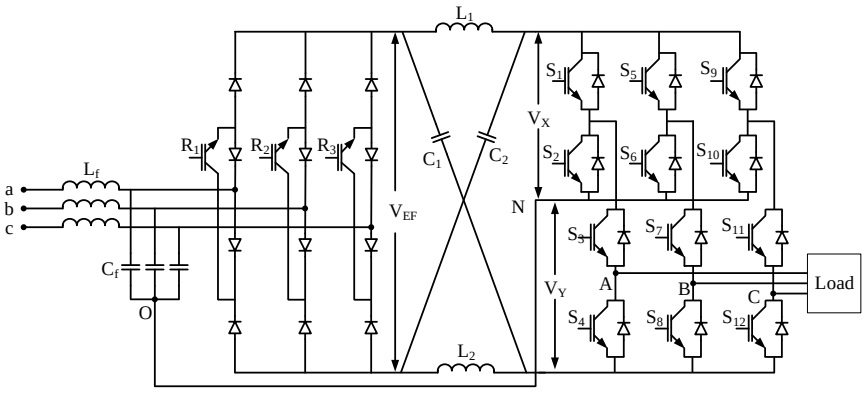

Figure 5.2: Configuration 2

In non-shoot through mode, switching combination are kept such that among the set of ($S1S2$, $S3S4$, $S5S6$, $S7S8$, $S9S10$, $S11S12$) the switching is complementary say $S1$ ON $\Rightarrow$ $S2$ OFF at any instant in the leg. This allows the stored energy in the Z source network to be delivered to the load. For better understanding of this state, proposed converter is reconfigured as shown in Figure.5.3 where $p, q \in$ (input phases a, b, c). Assuming inductors (L_1, L_2) and Capacitors (C_1, C_2) are equal, the steady state equations are given as

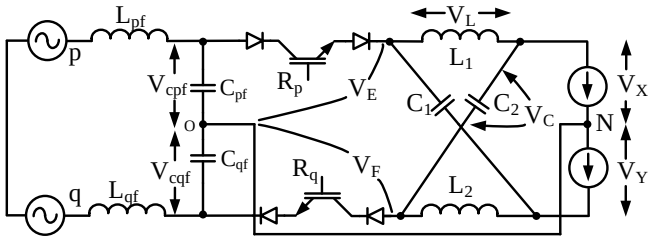

Figure 5.3: Non shoot through mode

$$V_E = V_L + V_X \tag{5.1}$$

$$V_{EF} = V_L + V_C \tag{5.2}$$

$$V_{EF} = V_{cpf} + V_{cqf} \tag{5.3}$$

$$V_F = V_L + V_Y \tag{5.4}$$

In upper shoot through (d_{ust}) mode, one switching combination in a set of ($S1S2$, $S5S6$, $S9S10$) are turned ON to provide a shoot through path for storing energy in the Z source network. While operation of lower inverter section is unaltered as shown in Figure.5.4. The inductor voltage equation can be written as

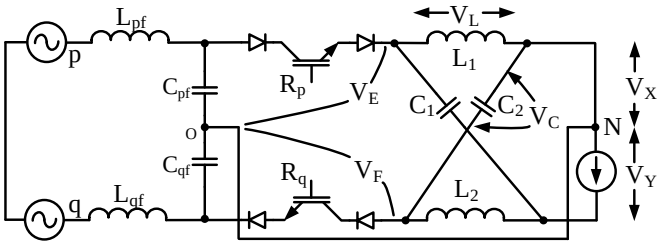

Figure 5.4: Upper shoot through mode

$$V_E = V_L \tag{5.5}$$

$$V_X = 0 \tag{5.6}$$

$$V_Y = V_C - V_L = V_C - V_E \tag{5.7}$$

In lower shoot through (d_{lst}) mode, one switching combination in a set of ($S2S3S4$, $S6S7S8$, $S10S11S12$) are turned ON to provide a shoot through path for storing energy in the Z source network. While operation of upper inverter section is unaltered as shown in Figure.5.5. The inductor voltage equation in this mode can be written as

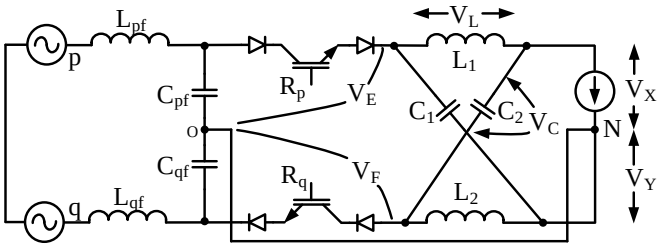

Figure 5.5: Lower shoot through mode

$$V_F = V_L \tag{5.8}$$

$$V_Y = 0 \tag{5.9}$$

$$V_X = V_C - V_L = V_C - V_F \tag{5.10}$$

According to volt-sec balance principle, the average voltage across inductor voltage equal to zero during one switching period. For equal duration of upper shoot through period and lower shoot through period ($d_{sh} = d_{ush} = d_{lsh}$), average inductor voltage should be zero.

$$(V_{EF} - V_C)(1 - d_{sh}) + V_E(d_{sh}) + V_F(d_{sh}) = 0 \tag{5.11}$$

$$V_C = V_{EF}\frac{1-d_{sh}}{(1-2d_{sh})} \tag{5.12}$$

Similarly average voltage across V_{XY} can be calculated as follows

$$V_X = (1-d_{sh})(V_E - V_L) + d_{sh}(V_C - V_F) \tag{5.13}$$

$$V_Y = (1-d_{sh})(V_F - V_L) + d_{sh}(V_C - V_E) \tag{5.14}$$

$$V_{XY} = V_X + V_Y \tag{5.15}$$

$$V_{XY} = \frac{V_{EF}}{(1-2d_{sh})} \tag{5.16}$$

5.3 Switching strategy

Space vector modulation technique is chosen for generating signals to control the proposed converter. In order to do so, current space vector and voltage space vector has been considered for controlling input power factor and output voltage, respectively.

Considering input voltages V_a, V_b, V_c given in eq.(5.17) are supplied to the rectifier

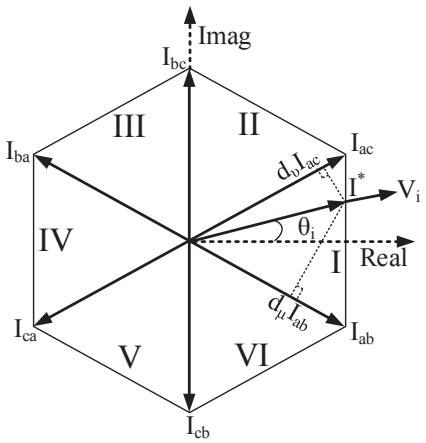

Figure 5.6: Current space vector diagram

section through an input low pass filter.

$$\begin{aligned} V_a &= V_i\cos(\theta_i) \\ V_b &= V_i\cos(\theta_i - 120^o) \\ V_c &= V_i\cos(\theta_i - 240^o) \end{aligned} \tag{5.17}$$

The current drawn from the supply I^* is aligned with input voltage vector V_i, as shown in Figure.5.6. Rectifier space vector diagram with reference current having a magnitude of I^* and angle θ_i lying in sector I, adjacent to the line currents I_{ab}, I_{bc}.

Reference current I^* projection on to the adjacent line currents results the duty ratio d_μ, d_ν. To reduce complexity and number of switching transitions burden on processor, null state (I_{aa}) of current source rectifier section is not considered in this chapter. Mathematically the duty ratios d_μ, d_ν are given as

$$\begin{aligned} d_\mu &= \frac{\sin\left(\frac{\pi}{6}-\theta_i\right)}{\cos(\theta_i)} \\ d_\nu &= \frac{\sin\left(\frac{\pi}{6}+\theta_i\right)}{\cos(\theta_i)} \end{aligned} \tag{5.18}$$

The average output voltage of rectifier section is calculated as

$$\begin{aligned} V_{EF} = (V_a - V_b)\,.\,(d_\mu d_\alpha + d_\mu d_\beta + d_\mu d_\delta + d_\mu d_{sh}) + \\ (V_a - V_c)\,.\,(d_\nu d_\alpha + d_\nu d_\beta + d_\nu d_\delta + d_\nu d_{sh}) \end{aligned} \tag{5.19}$$

$$V_{EF} = (d_\mu)\,(V_a - V_b) + (d_\nu)\,(V_a - V_c) \tag{5.20}$$

$$V_{EF} = \frac{3}{2cos(\theta_i)} V_i. \tag{5.21}$$

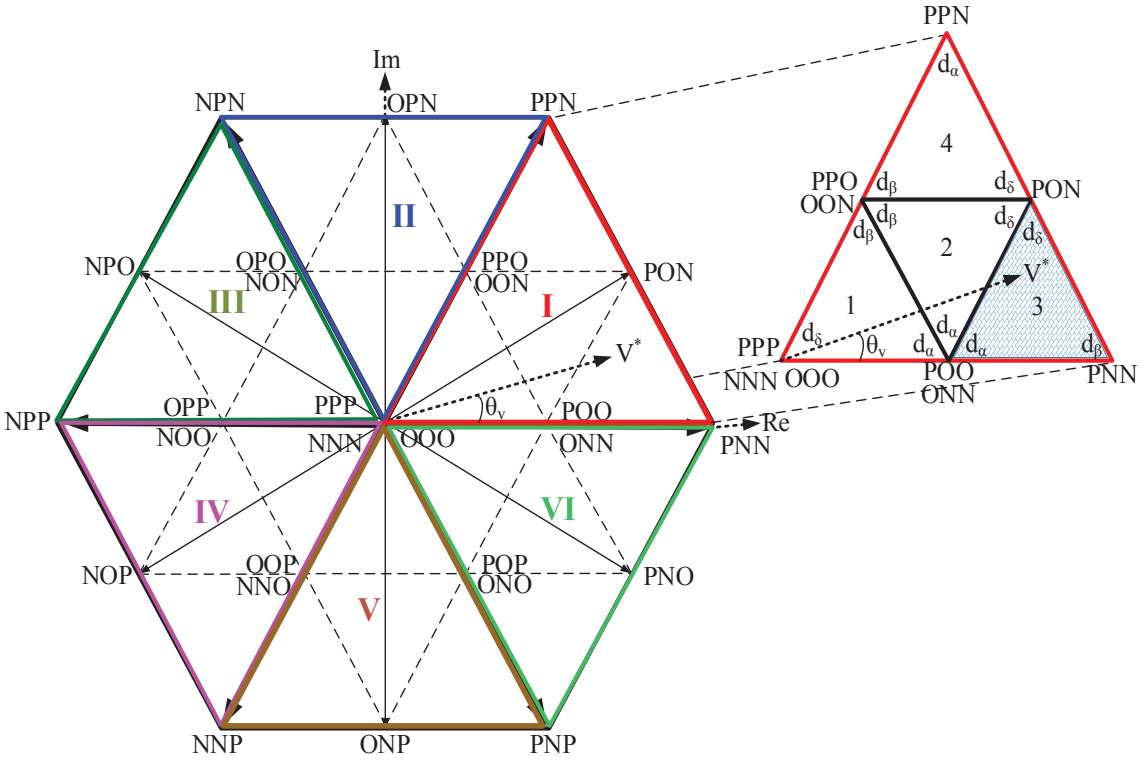

Figure 5.7: Three level inverter space vector diagram

Figure.5.7 shows three level inverter space vector diagram consisting of six sectors (I, II, III, IV, V, VI), magnifying sector I and denoting its sub sector regions as (1,2,3,4). It consists of total 27 switching states, out of which 6 are long vectors (PNN,

PPN, NPN, NPP, NNP, PNP), 6 are medium vectors (PON, OPN, NPO, NOP, ONP, PNO), 12 are small vectors (POO/ONN, PPO/OON, OPO/NON, OPP/NOO, OOP/ NNO, POP/ONO) and remaining 3 are zero vectors (PPP, NNN, OOO). Here in reference voltage vector (V^*) lies in sub sector region 3 with nearest voltage vectors are POO or ONN, PNN and PON. By projecting reference voltage vector (V^*) on to the nearest three vectors, dwell timings are calculated with respect to switching period. This results in duty ratios $d_\alpha, d_\delta, d_\beta$. d_α, d_β and d_δ which are corresponding to the switching states POO/ONN, PNN and PON. Duty ratio calculations are given in Table.5.1 where m_v is the modulation index of inverter section.

Table 5.1: Duty ratio equations

Region	d_α	d_δ	d_β
1	$m_v.\sin\left(\frac{\pi}{3}-\theta_v\right)$	$1-m_v.\sin\left(\frac{\pi}{3}+\theta_v\right)$	$m_v.sin\left(\theta_v\right)$
2	$1-m_v.sin\left(\theta_v\right)$	$m_v.\sin\left(\frac{\pi}{3}+\theta_v\right)-1$	$1-m_v.\sin\left(\frac{\pi}{3}-\theta_v\right)$
3	$2-m_v.\sin\left(\frac{\pi}{3}+\theta_v\right)$	$m_v.sin\left(\theta_v\right)$	$m_v.\sin\left(\frac{\pi}{3}-\theta_v\right)-1$
4	$m_v.sin\left(\theta_v\right)-1$	$m_v.\sin\left(\frac{\pi}{3}-\theta_v\right)$	$2-m_v.\sin\left(\frac{\pi}{3}+\theta_v\right)$

Assuming PON switching state is selected for generating signals which means, first letter P represents firing pulse (1010) for the first leg of the inverter (S1,S2,S3,S4), second letter O represents firing pulse (0110) for the second leg of the inverter (S5,S6,S7,S8) and last letter N represents firing pulse (0101) for the third leg of the inverter (S9,S10, S11,S12). All switching states represented in Figure.5.7 comes under non shoot through mode which is a normal three level inverter operation. In addition, with the presence of Z source network, upper shoot through and lower shoot through mode are required for boosting purposes. To achieve this, lower shoot through state is inserted when switching is taking place from O to N or vice versa without affecting upper inverter operation. Similarly upper shoot through state is inserted when switching is taking place from P to O or vice versa without affecting lower inverter operation. Upper shoot through firing pulse is given by U, which stands for switching state (1100) and lower shoot through firing pulse is given by L, which stands for switching state (0111) in a leg of inverter section. To make the proposed converter act as single stage converter, rectifier and inverter duty ratios are synchronised with each other ($d_\mu d_\alpha, d_\mu d_\beta, d_\mu d_\delta, d_\mu d_{sh}, d_\nu d_\alpha, d_\nu d_\beta, d_\nu d_\delta, d_\nu d_{sh}$) and compared with carrier wave

to generate signals. This allows control of input displacement angle, output voltage, sinusoidal input and output currents.

d_μ											d_υ										
d_α POO	d_{lst} POL	d_δ PON	d_β PNN	d_{ust} UNN	d_α ONN	d_{ust} UNN	d_β PNN	d_δ PON	d_{lst} POL	d_α POO	d_α POO	d_{lst} POL	d_δ PON	d_β PNN	d_{ust} UNN	d_α ONN	d_{ust} UNN	d_β PNN	d_δ PON	d_{lst} POL	d_α POO

Figure 5.8: Switching pattern for one cycle of operation

Switching pattern for one cycle of operation is shown in Figure.5.8 when V^* lies within sub sector region 3 under sector I, and I^* lies with in sector I. In Figure.5.8 shaded region indicates shoot through period. The final output voltage V_o equation through space vector modulation is given as

$$V_o = \frac{m_v}{\sqrt{3}} V_{XY} \tag{5.22}$$

5.4 Results

In order to verify the proposed topology, its operation is simulated in Matlab/Simulink environment. Table. 5.2 describes the parameters used for the simulation of the converter.

Table 5.2: Parameters

Power rating, P	$200W$
Input Voltage, V_i	$50V$
Fundamental line frequency, f_i	$50Hz$
Fundamental output frequency, f_o	$100Hz$
Switching frequency, f_{sw}	$5kHz$
Boost inductance, $L1, L2$	$2mH$
Boost Capacitance, C_1, C_2	100 μF
Load R	40 Ω

5.4.1 Simulation results

The converter is supplied with an input voltage of $50V, 50Hz$. By keeping supply constant, shoot through period ($d_{sh} = 0.2$) is applied to the converter which draws an

input current with RMS value of $1.8A$ for boosting, as shown in Figure.5.9. With this duty ratio, the total harmonic distortion (THD) of input currents is measured as 20% with respect to the fundamental value. However this THD can be reduced further by involving null vector in rectifier section.

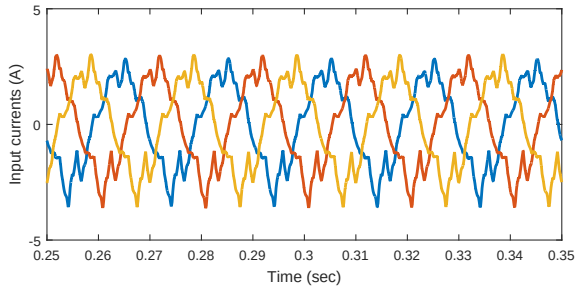

Figure 5.9: Input currents

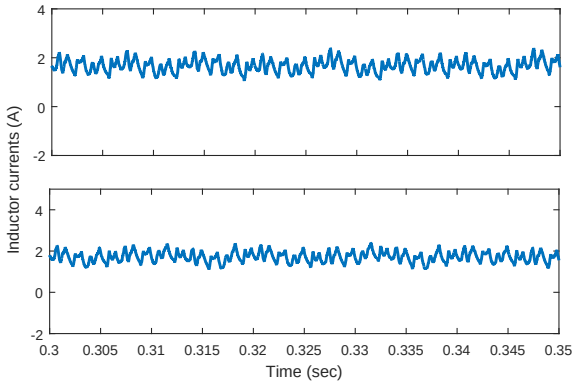

Figure 5.10: Currents in inductor

Current flowing in inductors (I_{L1}, I_{L2}) and voltage across capacitors (V_{C1}, V_{C2}) over a few cycles of switching frequency operation are given in Figure.5.10 and Figure.5.11, respectively. It can be noticed that current in the inductors shows a ripple current due to the switching behaviour of inverter section. However this ripple current variation depends upon switching frequency, duty ratio and inductor value. Similarly, the voltage across capacitors showing ripple voltage generated due to the switching behaviour of inverter section. This can be controlled by the proper selection of capacitance, switching frequency and duty ratio. Corresponding to the duty ratio $d_{sh} = 0.2$ and $m_v = 0.8$ average current flowing through inductor of Z source network is $1.9A$ and voltage across capacitor is $95V$.

Figure.5.12 shows the voltage variation at the input terminals V_x and V_y of three level inverter section. The voltage available at V_E terminals is get boosted to V_x voltage

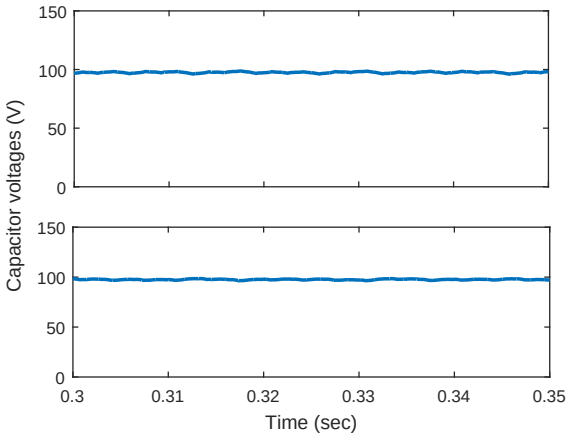

Figure 5.11: Voltage across capacitor

level with the help of Z source network by applying UST duty ratio d_{ush} in a switching period. In a similar line the voltage available at V_F terminals is get boosted to V_y voltage level with the help of Z source network by applying LST duty ratio d_{lsh} in a switching period. However this change in voltage variation at V_x, V_y terminals is corresponding to change in voltage variation at V_E, V_F terminals which is a resultant switching in between input line voltages.

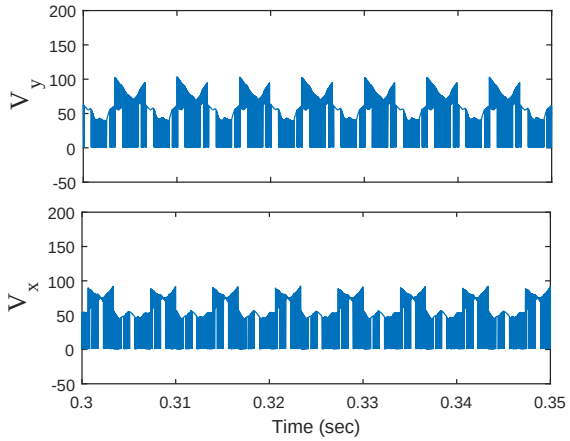

Figure 5.12: Voltage across V_x, V_y

Figure.5.13 shows the three level output line voltages operated with duty ratio. With $d_{sh} = 0.2$ the RMS value of output voltage is observed as $68V$ which is greater than the input $50V$. Through FFT analysis, THD of output voltage corresponding to fundamental frequency $100Hz$ is obtained as 39%. It shows that the inherent property of multilevel matrix converter is a buck converter, but with the integration of Z source network at DC link boosting in output voltage is achieved without tampering the

multilevel output behaviour.

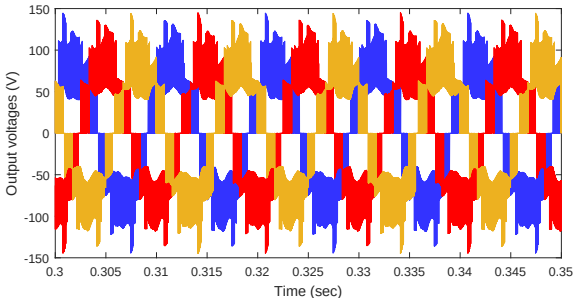

Figure 5.13: Output voltages

5.4.2 Experiment results

In order to validate the proof of concept, an experimental test rig was built as shown in Figure.5.14, by keeping similar parameters which are used for simulation.

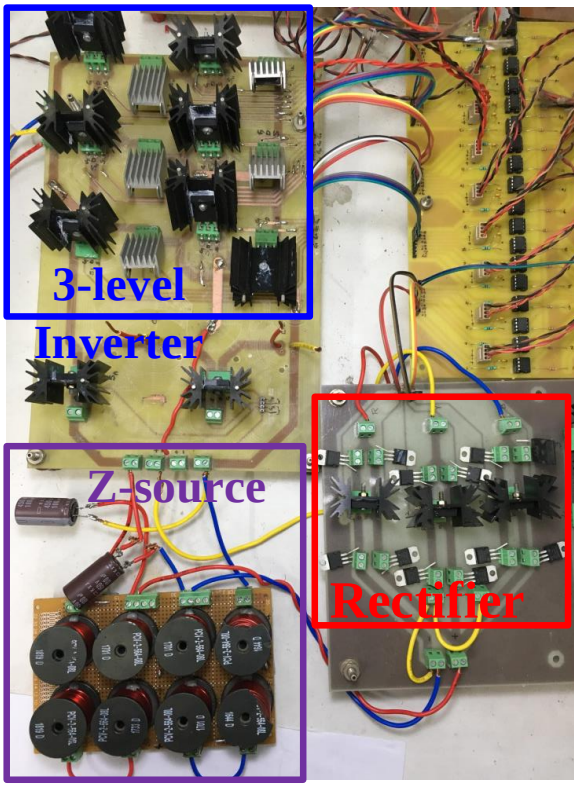

Figure 5.14: Experimental test rig circuit

The converter is supplied with an input voltage of $50V$ operating with frequency of $50Hz$. The current drawn from the supply is shown in Figure.5.15 with an RMS value of $1.6A$. Experimental THD value of an input currents are around 25% which is

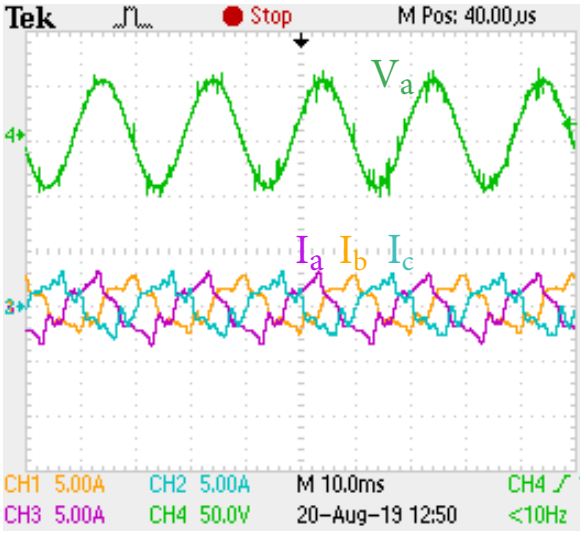

Figure 5.15: Input voltage (50V/div) and currents (5A/div)

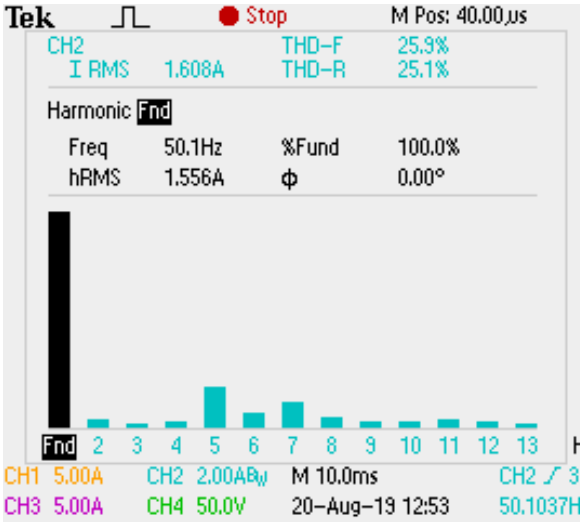

Figure 5.16: THD of input currents

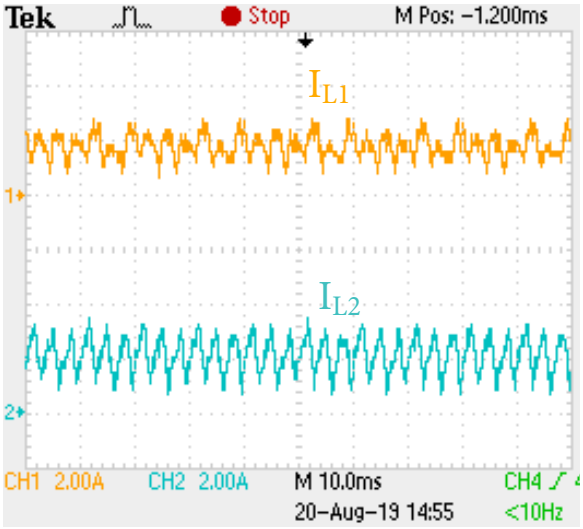

Figure 5.17: Inductor currents (5A/div)

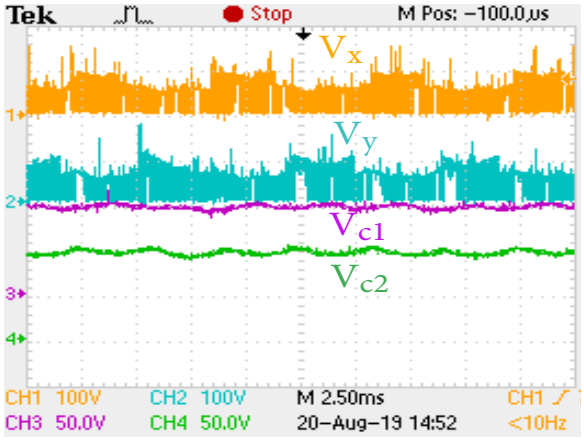

Figure 5.18: V_x, V_y voltages (50V/div)and capacitor voltages (50V/div)

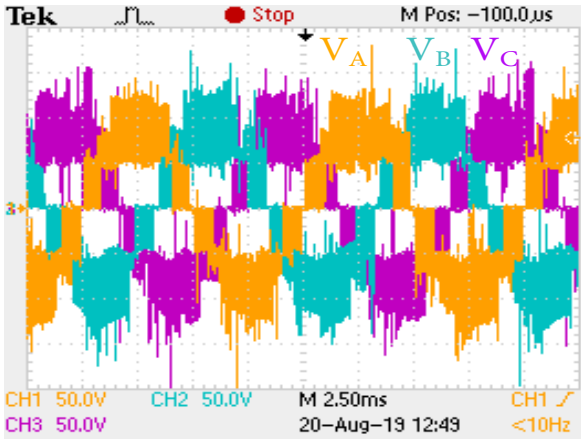

Figure 5.19: Output voltages (50V/div)

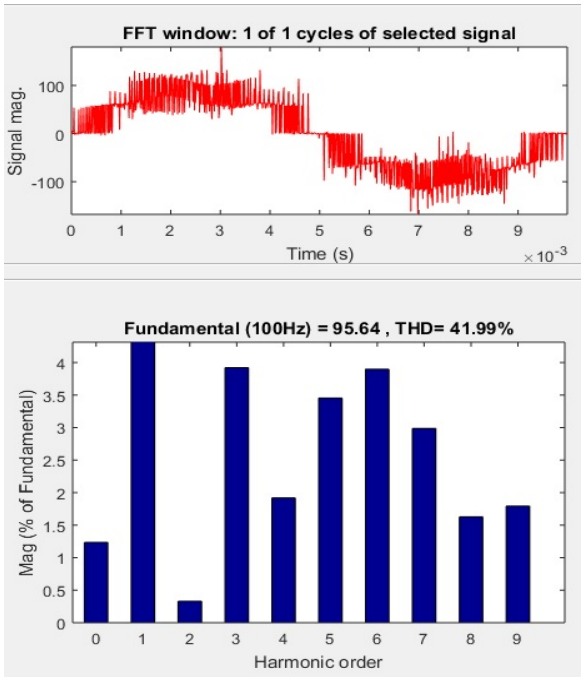

Figure 5.20: FFT analysis of output phase A voltage

shown in Figure.5.16. For the duty ratio $d_{sh} = 0.2$ and modulation index $m_v = 0.8$ the switching signals are generated using space vector modulation technique as discussed in previous section. Inductor currents and capacitor voltages waveforms are shown in Figures.5.17 and Figure.5.18 respectively. By observing the waveforms, it is found that the current flowing through inductor and voltage across capacitors follows the simulation results with slight variation due to the parasitics inductor and capacitor. In addition, voltage across V_x, V_y terminals are shown in Figure.5.18. Voltage across output terminals are shown in Figure.5.19 with an RMS value of $68V$. FFT analysis has been performed on output voltage. Figure.5.20 shows the THD of output voltage which is around 41% achieved without any output filter. There are voltage spikes present in waveforms due to connecting wires between Z source network and the inverter section.

5.5 Conclusion

This chapter gives a solution in improving the limitations of voltage gain and usage of number of power devices for multilevel ultra sparse matrix converter. Deriving the idea from cascaded DC link multilevel inverter and Z source ultra sparse matrix converter, a modification is made to multilevel ultra sparse matrix converter at the intermediate DC link section. While analysing the operation of proposed converter, output voltage gain greater than unity is observed. There is a trade off between reduction of 6 neutral clamped diodes with 3 over rated switches. Collectively the proposed converter renders high quality output waveforms without any filter, immune to external disturbances and false triggering, variable output voltage and frequency operation, control over input power factor operation. With these features the proposed converter could be a potential candidate among the existing topologies.