Chapter 4

Switched Boost Ultra Sparse Matrix Converter

4.1 Introduction

With the introduction of Z source network, power electronics community paved a way to extended topologies. The Z source network utilises the shoot through state of the converter for boosting. For this, shoot through pulses are given to the converter during zero state. This feature of Z source network makes it immune to EMI problems. The main restriction imposed by this network on to the converter is to maintain $m+d_{sh} \leq 1$, where m is the modulation of the converter and d_{sh} is the shoot through period. Integration of Z source network within matrix converters overcomes the major limitation likes voltage gain, shoot through capability and reactive power transfer capability. Integration of Z source network can be done in two cases, one by placing it before rectifier section of IMC and other is at DC link section of IMC. First case requires more number of passive elements and higher power rating of the devices as compared to the second case. Various Z source networks such as conventional Z source [30]- [50], quasi Z source [51], series Z source [34] and switched inductor Z source [31] are integrated at the DC link section of IMC. To implement these, Z source indirect matrix converter requires minimum 2 inductors and 2 capacitors which occupies more space. To achieve same voltage gain with lesser number of passive elements and to reduce the ripple current of inductor is motive of this chapter.

4.2 Proposed topology

The proposed converter is derived from USMC by the integration of switched boost network [52], as shown in Figure.4.1. Switched boost network consists of an inductor, capacitor, one switch and two diodes, as shown in Figure.4.2. By incorporating switched boost network at DC link section of USMC, Switched Boost Ultra Sparse Matrix Converter (SB-USMC) is obtained. Operation of SB-USMC is dependent on the operating modes of switched boost network.

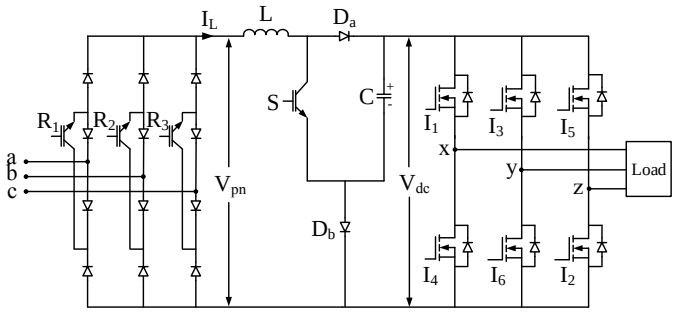


Figure 4.1: Switched boost Indirect matrix converter (SB-IMC)

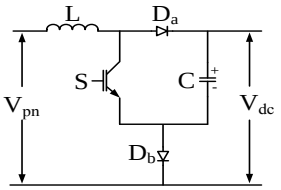


Figure 4.2: Switched Boost (SB) network

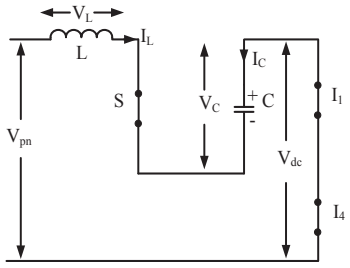


Figure 4.3: SB during shoot through mode

Switched boost network exhibits two modes: 1) Shoot through mode, 2) Non-shoot through mode.

Shoot through mode (d_{sh}): In this mode, inverter (top and bottom) switches of one or more legs are turned ON along with switch 'S' as shown in Figure.4.3. The diodes D_a

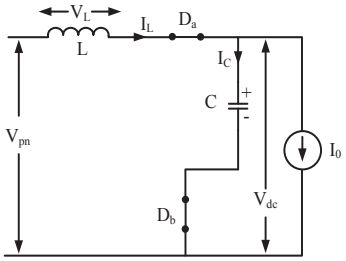


Figure 4.4: SB during non-shoot through mode

and D_b of boosting network gets reverse biased, allowing inductor to store energy with voltage $V_{pn} + V_C$.

Non-shoot through mode : During this mode, switch 'S' of boosting network is turned OFF. Keeping inverter stage active at the V_{dc} terminal. The diodes D_a and D_b gets forward biased allowing capacitor to connect in parallel with the inverter, as shown in Figure.4.4. Moreover the inductor delivers its energy to the load and charges the capacitor as well.

The boosting (B) achieved by this network is $B = \frac{1}{1-2d_{sh}} \Rightarrow d_{sh} = \frac{B-1}{2B}$ (where d_{sh} is shoot through period), which will be discussed in section 4.4

4.3 Switching strategy

In general, impedance source indirect matrix converters uses combination of current space vector (CSV) for rectifier and voltage space vector for inverter (VSV). It means rectifier section switches are operated with CSV, while inverter section switches are operated with VSV. As shown in Figure.4.5 and Figure.4.6 the reference current drawn from input and reference voltage desired at the output, are projected onto the respective active vectors for sector 1. In case of CSV, active vectors are line currents where as VSV has six active switching states as normal inverter. The duty ratios are calculated for both sections as given by eq.(4.1) and (4.2)

$$\begin{aligned} d_\mu &= \frac{\sin\left(\left(\frac{\pi}{6}\right)-\theta_i\right)}{\cos(\theta_i)} \\ d_\nu &= \frac{\sin\left(\left(\frac{\pi}{6}\right)+\theta_i\right)}{\cos(\theta_i)} \end{aligned} \tag{4.1}$$

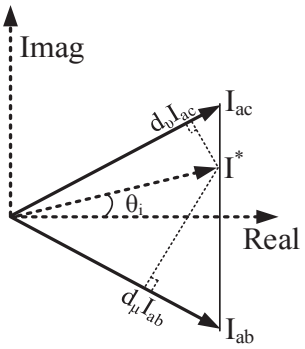


Figure 4.5: Current space vector (CSV)

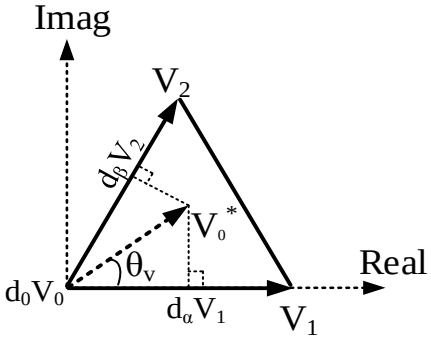


Figure 4.6: Voltage space vector (CSV)

$$\begin{aligned} d_\alpha &= m_v.\sin\left(\tfrac{\pi}{3} - \theta_v\right) \\ d_\beta &= m_v.\sin\left(\theta_v\right) \\ d_{sh} &= \tfrac{B-1}{2B} \\ d_0 &= 1 - (d_\alpha + d_\beta + d_{sh}) \end{aligned} \tag{4.2}$$

where θ_i is the angle of the current space vector. The voltage space vector modulation index $m_v = \frac{\sqrt{3}V^*}{V_{dc}}$ and θ_v is its angle. Shoot through state is a part of zero state in VSV and its corresponding duty ratio is denoted as d_{sh}. B is the boosting factor of the impedance source network.

To operate impedance source USMC as single stage converter, CSV and VSV duty ratio are multiplied as given in eq.(4.3). There are different possibilities to place these duty ratios within a switching period.

$$\begin{aligned} d_{\mu\alpha} &= d_\mu d_\alpha; \quad d_{\mu 0} = d_\mu d_0 \\ d_{\mu\beta} &= d_\mu d_\beta; \quad d_{\mu sh} = d_\mu d_{sh} \\ d_{\nu\alpha} &= d_\nu d_\alpha; \quad d_{\nu 0} = d_\nu d_0 \\ d_{\nu\beta} &= d_\nu d_\beta; \quad d_{\nu sh} = d_\nu d_{sh} \end{aligned} \tag{4.3}$$

The conventional way of placing the duty ratio for impedance source USMC are shown in Figure.4.7.

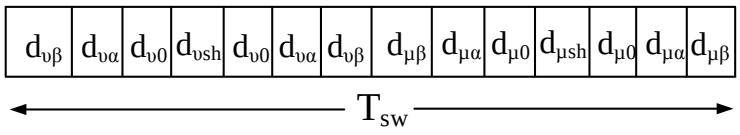
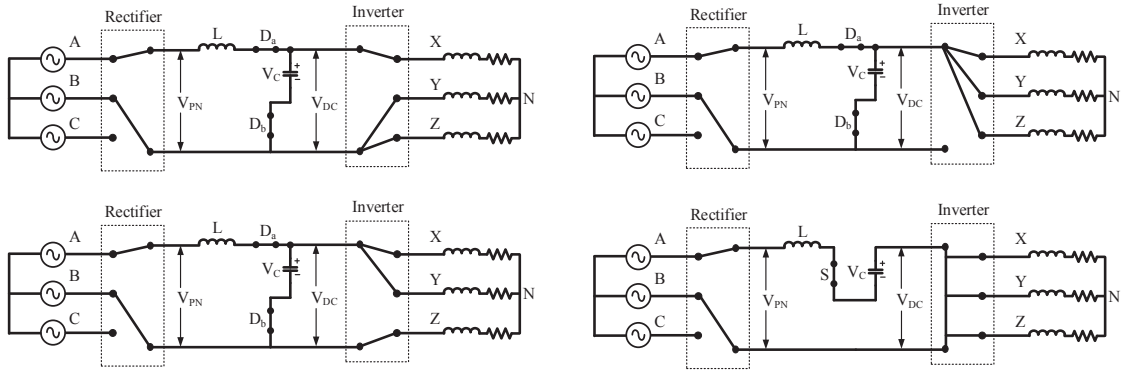


Figure 4.7: Switching states placement using two rectifier active vectors

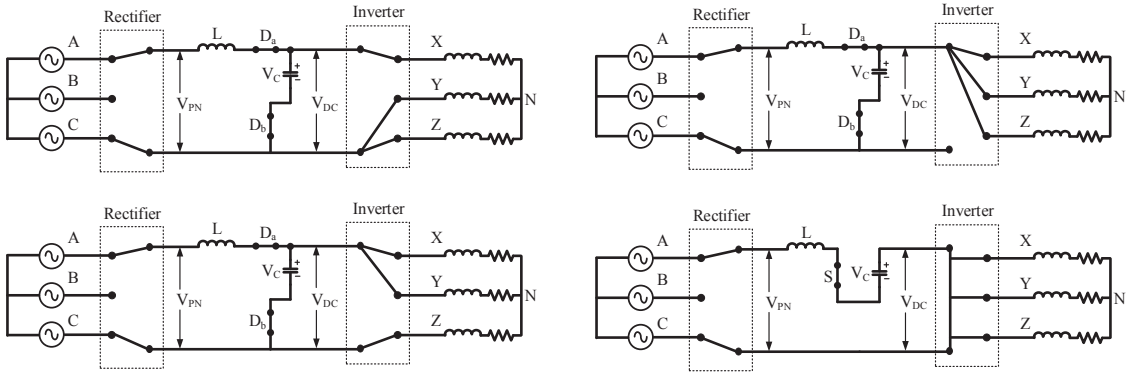
Consider rectifier section of impedance source USMC is supplied with input voltages V_a,V_b V_c.

$$\begin{aligned} V_a &= \hat{V}_i.\cos(\theta_i) \\ V_b &= \hat{V}_i.\cos\left(\theta_i - \tfrac{2\pi}{3}\right) \\ V_c &= \hat{V}_i.\cos\left(\theta_i - \tfrac{4\pi}{3}\right) \end{aligned} \tag{4.4}$$

Average rectifier voltage (V_{pn}) is obtained by considering combination of all switching states as shown in Figure.4.8.



(a) $d_\mu d_\alpha, d_\mu d_0, d_\mu d_{sh}, d_\mu d_\beta$ (clockwise)



(b) $d_\nu d_\alpha, d_\nu d_0, d_\nu d_{sh}, d_\nu d_\beta$ (clockwise)

Figure 4.8: Switching states of SB-USMC

$$\begin{aligned} V_{pn} &= (V_a - V_b) \,.\, (d_\mu d_\alpha + d_\mu d_\beta + d_\mu d_0 + d_\mu d_{sh}) + \\ &(V_a - V_c) \,.\, (d_\upsilon d_\alpha + d_\upsilon d_\beta + d_\upsilon d_0 + d_\upsilon d_{sh}) \end{aligned} \tag{4.5}$$

Since $d_\alpha + d_\beta + d_0 + d_{sh} = 1$, eq.(4.5) becomes

$$V_{pn} = (V_a - V_b) \,.d_\mu + (V_a - V_c) \,.d_\nu \tag{4.6}$$

By substituting (4.3) and eq.(4.4) in eq.(4.6)

$$\begin{aligned} V_{pn} = \left(\hat{V}_i \cos(\theta_i) - \hat{V}_i \cos\left(\theta_i - \left(\tfrac{2\pi}{3}\right)\right)\right) \tfrac{\sin\left(\left(\frac{\pi}{6}\right) - \theta_i\right)}{\cos(\theta_i)} + \\ \left(\hat{V}_i \cos(\theta_i) - \hat{V}_i \cos\left(\theta_i - \left(\tfrac{4\pi}{3}\right)\right)\right) \tfrac{\sin\left(\left(\frac{\pi}{6}\right) + \theta_i\right)}{\cos(\theta_i)} \\ V_{pn} = \tfrac{3.\hat{V}_i}{2\cos(\theta_i)}. \end{aligned} \tag{4.7}$$

It must be noticed that the average rectified voltage (V_{pn}) for sector 1 region contains a variable in the form of theta. For one complete cycle of input frequency, V_{pn} produces a ripple with six times the input frequency. By applying this voltage V_{pn} across the impedance source networks in various types of impedance source USMC results in non sinusoidal output voltages, unless the factor $\frac{1}{\cos(\theta_i)}$ can be nullified with the design of impedance network [29], [50]. However, it is a cumbersome solution for design. In order to make average rectifier voltage a constant value, two solutions are possible using zero vector and using three vector.

4.3.1 Using Zero vector

Using zero vector in the rectifier section of impedance source USMC which is reported in literature [34] [50]. With the inclusion of zero vector ($d_z I_{aa}$ in sector 1 of Figure.4.9), there is extra degree of freedom in the form of modulation index (m_c) to control the average voltage V_{pn}. Previously it was with θ_i variable which has no control and depends only on input voltage vector position ($m_c = \frac{1}{\cos(\theta_i)}$). By the use of zero vector as shown in Figure.4.9, the rectifier duty ratios are rewritten as given by eq.(4.8).

$$\begin{aligned} d_\mu &= m_c . \sin\left(\tfrac{\pi}{6} - \theta_i\right) \\ d_\nu &= m_c . \sin\left(\tfrac{\pi}{6} + \theta_i\right) \\ d_z &= 1 - (d_\mu + d_\nu) \end{aligned} \tag{4.8}$$

where $m_c = \frac{I^*}{I}$ is the modulation index of current space vector.

Placement of duty ratio in a switching period is shown in Figure.4.10.

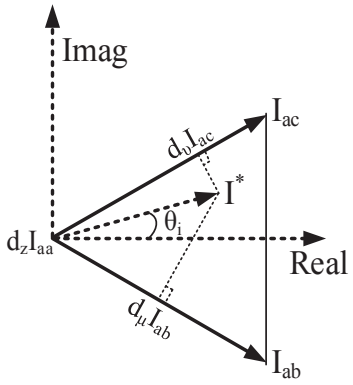


Figure 4.9: SVR with two rectifier active vectors and one null vector

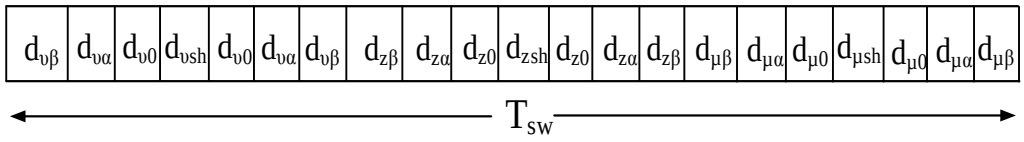


Figure 4.10: Switching states placement using two rectifier active vectors and one null vector

Substituting eq.(4.8) in eq.(4.5) gives

$$\begin{aligned} V_{pn} &= d_\mu.(V_a - V_b) + d_\nu.(V_a - V_c) + d_z.(V_b - V_c) \\ V_{pn} &= \tfrac{3.\hat{V}_i.m_c}{2} \end{aligned} \tag{4.9}$$

Although average voltage of V_{pn} can be made constant using zero vector, but operating rectifier closer to $m_c = 1$ results lower d_z value which further reduces to quite low value by multiplying with the inverter active states that is $d_z d_\alpha, d_z d_\beta, d_z d_0, d_z d_{sh}$. The low duty ratio period in a switching period is sliced with very small periods which increases stress across the switching power devices to switch ON and OFF resulting in requirement of high speed power devices.

4.3.2 Using Three vector

To achieve constant average voltage across V_{pn} another approach is by involving third vector I_{bc} which is adjacent to sector 1 as shown in Figure.4.11. Usage of three vector space vector modulation (TSVM) for rectifier section is already reported for current source rectifier [11]. Till now TSVM is not considered for impedance source matrix converters. The TSVM is more advantageous for impedance source converters in terms of inductor current ripple reduction. This can be explained by projecting reference current vector on to the line currents as shown in Figure.4.11 and corresponding duty

ratio calculations are given below.

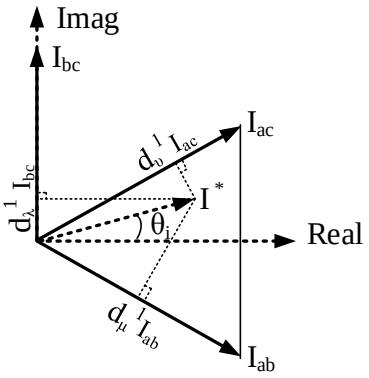


Figure 4.11: SVR using three rectifier active vectors

$$\begin{aligned} d_{\mu}^{1} &= 1 - m_c \sin\left(\theta_i + \tfrac{\pi}{6}\right) \\ d_{\nu}^{1} &= -1 + \sqrt{3} m_c \sin\left(\theta_i + \tfrac{\pi}{6}\right) \\ d_{\lambda}^{1} &= 1 - m_c \cos\left(\theta_i\right) \end{aligned} \tag{4.10}$$

The modified active duty ratios are presented in eq.(4.11)

$$\begin{aligned} d_{\mu\alpha}^{1} &= d_{\mu}^{1} d_{\alpha}, \quad d_{\mu o}^{1} = d_{\mu}^{1} d_{o} \\ d_{\mu\beta}^{1} &= d_{\mu}^{1} d_{\beta}, \quad d_{\mu sh}^{1} = d_{\mu}^{1} d_{sh} \\ d_{\nu\alpha}^{1} &= d_{\nu}^{1} d_{\alpha}, \quad d_{\nu o}^{1} = d_{\nu}^{1} d_{o} \\ d_{\nu\beta}^{1} &= d_{\nu}^{1} d_{\beta}, \quad d_{\nu sh}^{1} = d_{\nu}^{1} d_{sh} \\ d_{\lambda\alpha}^{1} &= d_{\lambda}^{1} d_{\alpha}, \quad d_{\lambda o}^{1} = d_{\lambda}^{1} d_{o} \\ d_{\lambda\beta}^{1} &= d_{\nu}^{1} d_{\beta}, \quad d_{\lambda sh}^{1} = d_{\lambda}^{1} d_{sh} \end{aligned} \tag{4.11}$$

The corresponding switching state placement is shown in Figure.4.12. By calculating

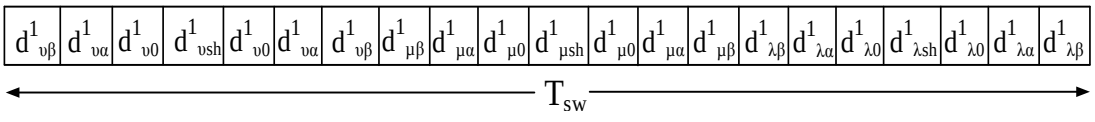


Figure 4.12: Switching states placement using three rectifier active vectors

average rectifier voltage with three vector modulation scheme results in constant value which depends upon the peak input voltage.

$$\begin{aligned} V_{pn} &= d_{\mu}^{1}.\left(V_a - V_b\right) + d_{\nu}^{1}.\left(V_a - V_c\right) + d_{\lambda}^{1}.\left(V_b - V_c\right) \\ V_{pn} &= \tfrac{3.\hat{V}_i.m_c}{2} \end{aligned} \tag{4.12}$$

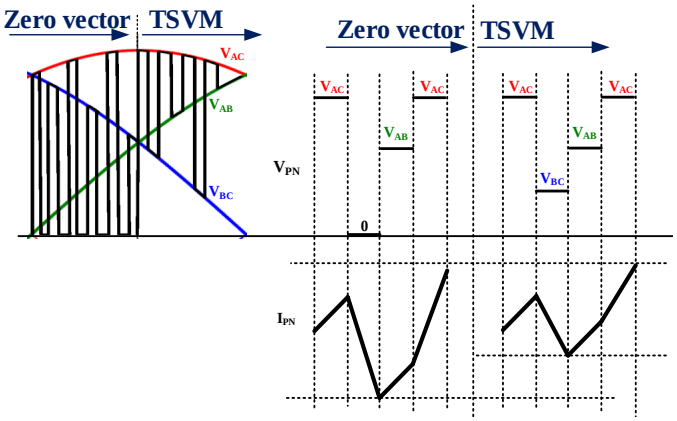


Figure 4.13: Visualization of switching in between line voltages

Visualization of TSVM switching across V_{pn} terminals and corresponding current ripple is shown in Figure.4.13, where at any instant of time three line voltages are available. It is to be noted that during first half period with zero vector, after active state V_{pn} falls to zero voltage level. Whereas with TSVM, V_{pn} switches to another line voltage rather than zero. The effective voltage change in V_{pn} (applied to the inductor for charging) is less for TSVM. Hence the current ripple is reduced for the proposed SB-USMC.

4.4 Steady state Analysis

The steady state analysis of the proposed converter is done by assuming ideal characteristics of diodes, switches, inductor and capacitors. The input voltage, as given by eq.(4.4), are fed into the system. The voltage available across the V_{pn} is controlled with SVR using three vectors as given in eq.(4.12). With respect to voltage V_{pn}, as shown in Figure.4.3, inductor voltage and capacitor current during shoot through state ($d_{sh}T_{SW}$) of switched boost network is represented as

$$\begin{aligned} V_L &= V_{pn} + V_C \\ i_C &= -i_L \end{aligned} \tag{4.13}$$

From Figure.4.4 during non shoot through state $(1 - d_{sh}).T_{SW}$

$$\begin{aligned} V_L &= V_{pn} - V_C \\ i_C &= i_L - i_o \end{aligned} \tag{4.14}$$

By volt-sec balance principle for inductor and current-sec balance principle for capacitor, above equations can be represented as

$$\begin{aligned}&(V_{pn}+V_C)\,d_{sh}T_{sw}+(V_{pn}-V_C)\,(1-d_{sh})\,T_{sw}=0\\&\tfrac{V_C}{V_{pn}}=\tfrac{1}{1-2d_{sh}}\end{aligned}\tag{4.15}$$

$$\begin{aligned}&(-i_L)\,d_{sh}T_{sw}+(i_L-i_o)\,(1-d_{sh})\,T_{sw}=0\\&\tfrac{i_L}{i_o}=\tfrac{1-d_{sh}}{1-2d_{sh}}\end{aligned}\tag{4.16}$$

The boosting achieved with switched boost network

$$V_{dc}=V_C=\frac{1}{1-2d_{sh}}V_{pn}=BV_{pn}\tag{4.17}$$

Using eq.(4.12) and eq.(4.17)

$$V_{dc}=\frac{3}{2}m_cBV_i\tag{4.18}$$

Since inverter is operated with conventional space vector modulation, the output voltage achieved is given as

$$V_0=\frac{m_v}{\sqrt{3}}V_{dc}\tag{4.19}$$

By substituting eq.(4.18) in eq.(4.19) results in

$$V_0=\frac{\sqrt{3}m_cm_v}{2}B\hat{V}_i\tag{4.20}$$

Taking into account input power factor ($\cos(\phi_i)$) the output voltage of the proposed converter is given as

$$V_0=\frac{\sqrt{3}m_cm_v}{2}B\hat{V}_i\cos(\phi_i)\tag{4.21}$$

$$V_0=\frac{\sqrt{3}m_cm_v}{2(1-2d_{sh})}\hat{V}_i\cos(\phi_i)\tag{4.22}$$

Design equations: Selection of passive components is chosen based on ripple in voltage and current. By considering design equation during shoot state, the equation for inductor current is given as

$$L\frac{di_L}{dt}=V_{pn}+V_C\tag{4.23}$$

since $\frac{di_L}{dt}$ can be written as follows $\frac{di_L}{dt}=\frac{\Delta I_L}{d_{sh}T_{SW}}$, eq.(4.23) is modified as

$$\Delta I_L=\frac{V_{pn}+V_C}{L}d_{sh}T_{SW}\tag{4.24}$$

Substituting eq.(4.15) in eq.(4.24)

$$\Delta I_L=\frac{V_{pn}T_{sw}2d_{sh}\,(1-d_{sh})}{L\,(1-2d_{sh})}=\frac{3\hat{V}_im_cd_{sh}\,(1-d_{sh})}{f_{sw}L\,(1-2d_{sh})}\tag{4.25}$$

In terms of rectified power P the inductor current can be written as

$$I_L = \frac{P}{V_{pn}} = \frac{P}{\left(\frac{3}{2}\right)\hat{V}_i \cos\left(\phi_i\right)} \tag{4.26}$$

Considering $\Delta I_L = k\%\left(I_L\right)$ and $m_c = 1$, above equation can be rearranged as

$$L = \frac{2\hat{V}_i^2 d_{sh}\left(1 - d_{sh}\right)\cos^2\left(\phi_i\right)}{f_{sw} k\% P\left(1 - 2d_{sh}\right)} \tag{4.27}$$

Similar analysis for capacitor is given as

$$C\frac{dV_C}{dt} = i_L \tag{4.28}$$

$$\Delta V_C = \frac{I_L d_{sh} T_{sw}}{C} = \frac{2P d_{sh}}{3C f_{sw}\hat{V}_i \cos\left(\phi_i\right)} \tag{4.29}$$

Assuming $\Delta V_C = q\%(V_C)$ the above equation can be modified as

$$C = \frac{4P d_{sh}\left(1 - 2d_{sh}\right)}{9 f_{sw} q\% \hat{V}_i^2 \cos^2\left(\phi_i\right)} \tag{4.30}$$

4.5 Validation

In order to validate the proposed concept, switched boost ultra sparse matrix converter is first simulated in MATLAB/Simulink environment delivers an efficiency of 86% and same is implemented to build experimental test rig as shown in Figure.4.14 with specifications as listed in Table.4.1. The switches and diodes in the proposed converter are realised using STmicroelectronic components $STW33N60DM2$ and $STPS60170CT$.

The proposed converter is supplied with an input voltage of $60V$. Rectifier section is operated with space vector modulation having current modulation index $m_c = 1$. It draws sinusoidal input currents with peak amplitude of $4.4A$. Input voltage and current waveforms are shown in Figure.4.15, which shows that currents drawn from supply consists of harmonic contents with total harmonic distortion (THD) of around 9%, as shown in Figure.4.16. Though in simulation the THD was around 3%, due to the stray inductance of connecting wires and PCB tracks the THD during experiment changed between $6 - 9\%$. THD can be reduced by increasing size of input filter. The voltage produced at V_{pn} terminals follows the pattern of positive line voltages switching in between them, with an average voltage of $83V$ as per eq.(4.12). The duty ratio is kept at $d_{sh} = 0.28$ to boost the average V_{pn} by 2.29 times, as shown in Figure.4.17. The

Table 4.1: Parameters

Power	$320W$
Input Voltage, $\hat{V}_i$	$60\ V$
Fundamental line frequency, f_i	$50\ Hz$
Fundamental output frequency, f_o	$100\ Hz$
Switching frequency, f_{sw}	$5\ kHz$
Boost inductance, L	$3\ mH$
Boost Capacitance, C	$290\ \mu$F
Inductor current ripple, ΔI_L	10%
Capacitor voltage ripple, ΔV_C	10%

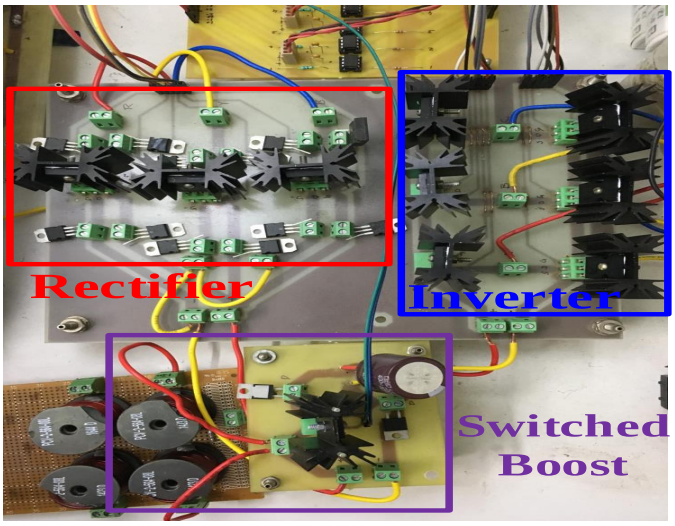


Figure 4.14: Experimental test rig

inductor current drawn from rectifier section is shown in Figure.4.18 with an amplitude of $4.4A$. Fig.4.18 shows that the voltage across capacitor is $185V$ which is controlled by duty ratio as per eq.(4.15). This is equivalent to the value of V_{dc} during non shoot through period.

Voltage across V_{dc} terminals is shown in Figure.4.19. It can be seen that voltage across V_{dc} terminals is switching in between $0V$ to $150V$. The level $0V$ corresponds to shoot through state while $150V$ to non shoot through state of the proposed converter. In Figure.4.20 the voltage across switch S is similar to the voltage V_{dc} across which decides the voltage rating of the switch. With the available boosted voltage V_{dc} across the inverter and by operating it using space vector modulation having a modulation

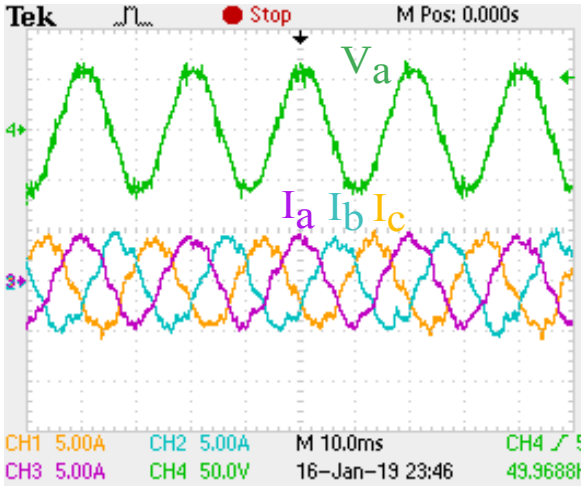


Figure 4.15: Input voltage (50V/div) and currents (5A/div)

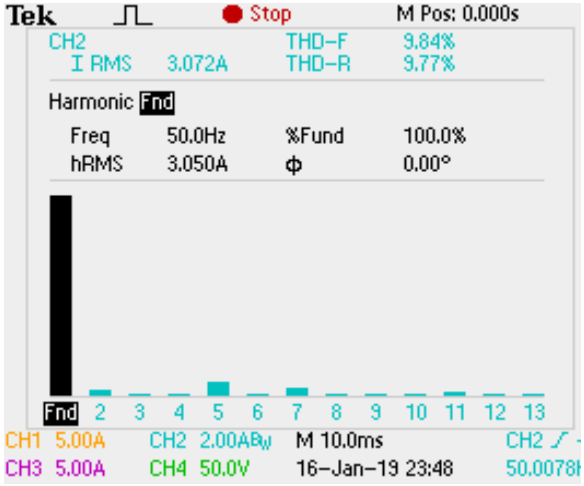


Figure 4.16: THD of input currents

index ($m_v = 0.72$), the output voltages are obtained as shown in Figure.4.21. The maximum value of output voltage is $80V$ which is $5V$ less than the theoretical value due to drop in diodes and switches. The THD in the output voltage is less than 7% value which is suitable for practical application.

4.6 Comparative analysis

The ZS-USMC, SZ-USMC, QZ-USMC and SWZ-USMC converter's are recently reported impedance source USMC. These converters are chosen here to compare with the proposed converter. All the converters are operated under similar operating conditions in respect of input supply voltage, modulation scheme and connected load. For

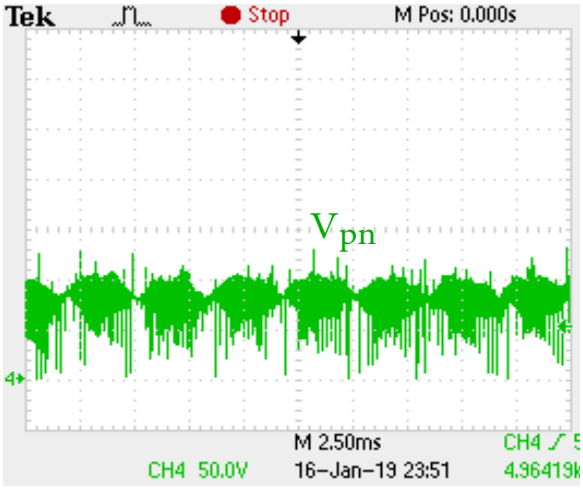


Figure 4.17: V_{pn} voltage (50V/div)

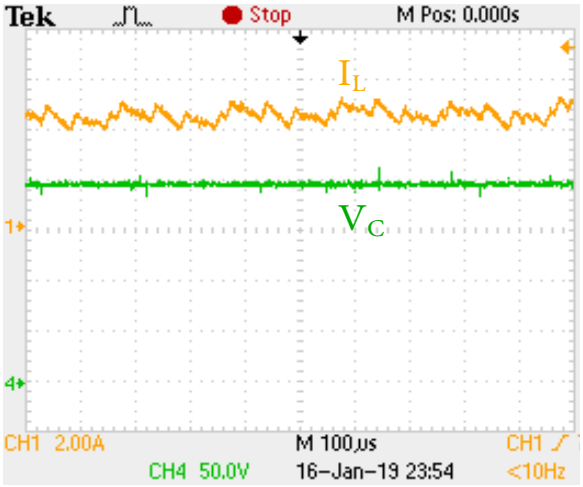


Figure 4.18: I_L current (2A/div) and V_C voltage (50V/div)

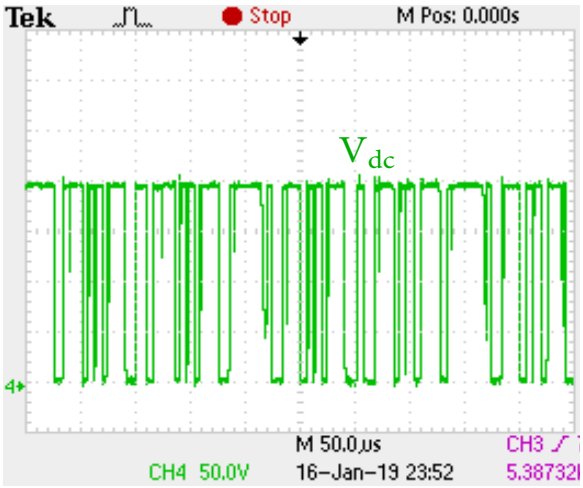


Figure 4.19: V_{dc} voltage (50V/div)

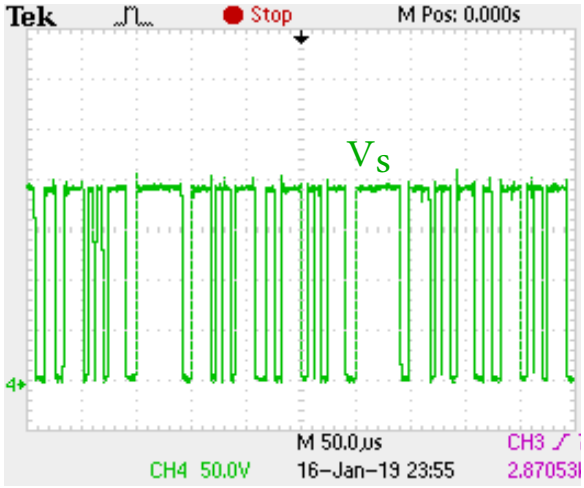


Figure 4.20: V_S switch voltage (50V/div)

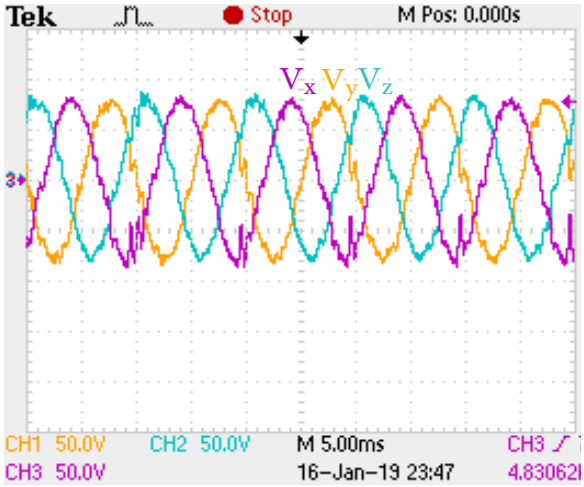


Figure 4.21: Output voltages (50V/div)

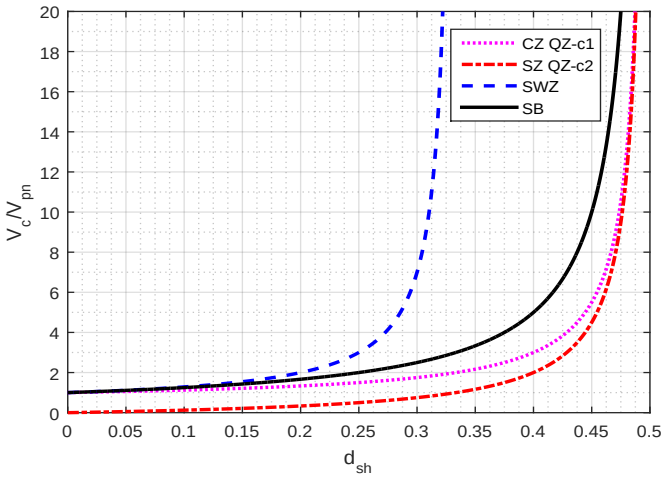


Figure 4.22: $\frac{V_c}{V_{pn}}$ Vs d_{sh}

boosting factor (B), which is controlled by duty ratio (d_{sh}), inductor current and capacitor voltage equations are derived as listed in Table 4.2. It can be seen that current

Table 4.2: Parameters

Converter	Inductor current	Capacitor voltage	No.of passive elements	No. of diodes	No. of switches
ZS-USMC	$I_{L1} = I_{L2} = \frac{\sqrt{3}m_v I_o cos(\phi_o)}{2}$	$V_{C1} = V_{C2} = \frac{(1-d_{sh})}{(1-2d_{sh})}V_{pn}$	4	18	9
SZ-USMC	$I_{L1} = I_{L2} = \frac{\sqrt{3}(1-d_{sh})m_v I_o cos(\phi_o)}{2(1-2d_{sh})}$	$V_{C1} = V_{C2} = \frac{(d_{sh})}{(1-2d_{sh})}V_{pn}$	4	19	9
QZ-USMC	$I_{L1} = I_{L2} = \frac{\sqrt{3}(1-d_{sh})m_v I_o cos(\phi_o)}{2(1-2d_{sh})}$	$V_{C1} = \frac{(1-d_{sh})}{(1-2d_{sh})}V_{pn}$,$V_{C2} = \frac{(d_{sh})}{(1-2d_{sh})}V_{pn}$	4	19	9
SWZ-USMC	$I_{L1,2,3,4} = \frac{\sqrt{3}m_v I_o cos(\phi_o)}{2}$	$V_{C1} = V_{C2} = \frac{(1-d_{sh})}{(1-3d_{sh})}V_{pn}$	6	24	9
SB-USMC	$I_L = \frac{\sqrt{3}(1-d_{sh})m_v I_o cos(\phi_o)}{2(1-2d_{sh})}$	$V_C = \frac{1}{(1-2d_{sh})}V_{pn}$	2	20	10

rating of the inductor required for boosting in case of proposed converter, SZ-USMC and QZ-USMC remains same while others require higher value. The voltage rating of capacitors are different for various converters. By plotting ratio of capacitor voltage and V_{pn} against duty ratio as shown in Figure.4.22, it is observed that proposed converter requires slightly higher value of capacitor voltage rating than others due to higher boosting ratio (except for SWZ-USMC). The passive elements required for proposed converter is much lesser than other converters, However, SB-USMC requires one extra switch. The voltage and current rating of the extra switch S is same as capacitor voltage rating and current rating of the inductor. The Proposed converter SB-USMC is implemented using TSVM, which reduces the ripple current by around 2%.

4.7 Conclusion

By utilizing the idea of switched boost network, a modification is made to integrate it within USMC. With this modification, it overcomes the inherent limitations of limited output voltage without compromising any input and output THD performances. During boosting operation experimental results are in agreement with analytical calculation. Corresponding to duty ratio $d_{sh} = 0.28$, for input voltage of $60V$, $V_{dc} = 185V$ and output voltage of $85V$ is observed with the proposed SB-USMC. Compared to contemporary converters the proposed SB-USMC has advantages of having less number of passive elements and linear operating region. In addition TSVM technique is implemented and validated for proposed SB-USMC. With the TSVM technique, current ripple associated with the inductor reduces. In addition, unlike zero vector, TSVM don't require very high speed power devices.

Although the gain of the proposed SB-USMC is high, however, due to two level voltage at output terminals, it has higher THD. In the next chapter, a Z-source based multilevel ultra sparse matrix converter is proposed. The proposed multilevel converter have features such as high gain, lower THD and reduced EMI.