Chapter 2

Modulation techniques for matrix converters

Modulation schemes are integral component of a power converter. Various modulation techniques are reported for matrix converters. This include venturini, scalar modulation, carrier techniques and space vector modulation (SVM). A brief discussion of each modulation technique is explained in this capter.

2.1 Venturini modulation

Initially, direct matrix converters were controlled using Venturini modulation. Venturini modulation is based on direct transfer function approach. In direct matrix converters there is direct connection of input phase with output phase through bidirectional switches denoted by S_{ij}, where $i\epsilon(a,b,c)$, $j\epsilon(x,y,z)$. Since there is a direct connection, the input phase shall never be short circuited and output phase should never be open circuited.

Let us consider the set of input voltages and output voltages as

$$\begin{aligned} V_a &= V_i \cos(\omega_i t) \\ V_b &= V_i \cos(\omega_i t - 120°) \\ V_c &= V_i \cos(\omega_i t - 240°) \end{aligned} \tag{2.1}$$

$$
\begin{aligned}
V_x &= V_o \cos(\omega_o t) \\
V_y &= V_o \cos(\omega_o t - 120°) \\
V_z &= V_o \cos(\omega_o t - 240°)
\end{aligned}
\tag{2.2}
$$

where V_i, V_o are the amplitudes of input and output voltages, $\omega_i t, \omega_o t$ are the frequencies of input and output voltages.

Similarly the input currents and output currents are defined as

$$
\begin{aligned}
I_a &= I_i \cos(\omega_o t + \phi_i) \\
I_b &= I_i \cos(\omega_o t - 120° + \phi_i) \\
I_c &= I_i \cos(\omega_o t - 240° + \phi_i)
\end{aligned}
\tag{2.3}
$$

$$
\begin{aligned}
I_x &= I_o \cos(\omega_o t + \phi_o) \\
I_y &= I_o \cos(\omega_o t - 120° + \phi_o) \\
I_z &= I_o \cos(\omega_o t - 240° + \phi_o)
\end{aligned}
\tag{2.4}
$$

where I_i, I_o are the amplitudes of input and output currents, ϕ_i, ϕ_o are the input and output phase displacement factor.

Writing the above equations in matrix form

$$
V_I(t) = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{2.5}
$$

$$
V_O(t) = \begin{bmatrix} V_x \\ V_y \\ V_z \end{bmatrix} \tag{2.6}
$$

$$
I_I(t) = \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{2.7}
$$

$$
I_O(t) = \begin{bmatrix} I_x \\ I_y \\ I_z \end{bmatrix} \tag{2.8}
$$

Direct matrix converter relation is defined as

$$
V_O(t) = m(t) . V_I(t) \tag{2.9}
$$

$$I_I\left(t\right)=m(t)^T.I_O\left(t\right) \tag{2.10}$$

where $m(t)$ is the modulation matrix or low frequency transformer matrix.

$$m\left(t\right)=\begin{bmatrix} d_{ax} & d_{ay} & d_{az} \\ d_{bx} & d_{by} & d_{bz} \\ d_{cx} & d_{cy} & d_{cz} \end{bmatrix} \tag{2.11}$$

where d_{ij} is the duty cycle corresponding to the switch S_{ij}, $i\epsilon(a,b,c)$, $j\epsilon(x,y,z)$

Venturini modulation technique states that the solution of matrix $m(t)$ can be obtained by decomposing it into m^+ and m^- matrices and substituting in eq.(2.9)

$$m\left(t\right)=m^+\left(t\right)+m^-\left(t\right) \tag{2.12}$$

$$m^+\left(t\right)=\frac{\alpha_1}{3}\begin{bmatrix} 1+2Gcs\left(0\right) & 1+2Gcs\left(\frac{-2\pi}{3}\right) & 1+2Gcs\left(\frac{-4\pi}{3}\right) \\ 1+2Gcs\left(\frac{-4\pi}{3}\right) & 1+2Gcs\left(0\right) & 1+2Gcs\left(\frac{-2\pi}{3}\right) \\ 1+2Gcs\left(\frac{-2\pi}{3}\right) & 1+2Gcs\left(\frac{-4\pi}{3}\right) & 1+2Gcs\left(0\right) \end{bmatrix} \tag{2.13}$$

$$m^-\left(t\right)=\frac{\alpha_2}{3}\begin{bmatrix} 1+2Gca\left(0\right) & 1+2Gca\left(\frac{-2\pi}{3}\right) & 1+2Gca\left(\frac{-4\pi}{3}\right) \\ 1+2Gca\left(\frac{-2\pi}{3}\right) & 1+2Gca\left(\frac{-4\pi}{3}\right) & 1+2Gca\left(0\right) \\ 1+2Gca\left(\frac{-4\pi}{3}\right) & 1+2Gca\left(0\right) & 1+2Gca\left(\frac{-2\pi}{3}\right) \end{bmatrix} \tag{2.14}$$

where

$$\begin{aligned} &cs\left(x\right)=\cos\left(\omega_m t+x\right) \\ &ca\left(x\right)=\cos\left(-\left(\omega_m t+2\omega_i\right)+x\right) \\ &\omega_m=\omega_o-\omega_i \\ &\alpha_1=\tfrac{1}{2}\left(1+\tfrac{\tan(\phi_i)}{\tan(\phi_o)}\right) \\ &\alpha_2=\tfrac{1}{2}\left(1-\tfrac{\tan(\phi_i)}{\tan(\phi_o)}\right) \\ &G=\tfrac{V_0}{V_i} \end{aligned} \tag{2.15}$$

The solution presented by above equations is characterised as a limitations of voltage transfer ratio G.

$$\begin{aligned} &\alpha_1\geq 0 \\ &\alpha_2\geq 0 \\ &0\leq G\leq \tfrac{1}{2} \end{aligned} \tag{2.16}$$

The maximum voltage gain obtained by venturini modulation approach is $G = 0.5$. Improvement in voltage gain is possible by adding third harmonic voltages in output load equations. By doing this, the corresponding change in modulation matrix is

$$m(t) = \begin{bmatrix} u(0,0,0,0,0,0) & u(2,4,2,4,2,4) & u(4,2,4,2,4,2) \\ u(2,2,0,0,0,0) & u(4,0,2,4,2,4) & u(0,4,4,2,4,2) \\ u(4,4,0,0,0,0) & u(0,2,2,4,2,4) & u(2,0,4,2,4,2) \end{bmatrix} \tag{2.17}$$

where

$$\begin{aligned} u(w_1,w_2,w_3,w_4,w_5,w_6) &= \tfrac{1}{3}\Big\{1+\tfrac{\sqrt{3}}{2}p\left[r_1^1(w_1)+r_1^{-1}(w_2)-\tfrac{1}{6}r_3^1(w_3)-\tfrac{1}{6}r_3^{-1}(w_4)\right. \\ &\quad \left.+\operatorname{sign}(p)\left(-\tfrac{1}{6\sqrt{3}}r_0^4(w_5)\right)\right] + a_1 r_1^1(w_1) + a_2 r_1^{-1}(w_2)\Big\} \end{aligned}$$

$$r_\alpha^\beta(\gamma) = \cos\left((\alpha\omega_0+\beta\omega)t+\gamma\frac{\pi}{3}\right)$$

$$\begin{aligned} p &= \tfrac{1}{\sqrt{3}}(2G-a) \\ a &= 2|\theta|G \\ \theta &= \tfrac{\tan(\phi_i)}{\tan(\phi_o)} \end{aligned}$$

$$sign(p) = \begin{cases} 1, p \geq 1 \\ -1, p \leq 0 \end{cases}$$

By solving eq.(2.17) and eq.(2.9) voltage gain is

$$2G\left[|\theta|\left(1-\frac{sign(p)}{\sqrt{3}}\right)+\frac{sign(p)}{\sqrt{3}}\right] \leq 1 \tag{2.18}$$

$$G \leq 0.866 \tag{2.19}$$

2.2 Scalar modulation

Unlike venturini modulation technique, scalar modulation depends on ratio of instantaneous input voltages. Scalar modulation is proposed by Roy in [6], [38]. According to this method, the switching signals are generated directly by the measurement of source phase voltages (V_a, V_b, V_c).

Consider the instantaneous load voltages as

$$V_0 = \frac{1}{T_{sw}}\left[t_k V_k + t_l V_l + t_m V_m\right] \tag{2.20}$$

$$t_k + t_l + t_m = T_{sw} \tag{2.21}$$

$$\begin{aligned} d_k &= \frac{t_k}{T_{sw}} \\ d_l &= \frac{t_l}{T_{sw}} \\ d_m &= \frac{t_m}{T_{sw}} \end{aligned} \tag{2.22}$$

where m is the source phase voltage which has a polarity different from the others, k is the source phase voltage of same polarity and also the smallest one of the two, remaining phase voltage is denoted as l for the interval $0 \le (\frac{t_k}{t_l} = \frac{V_k}{V_l}) \le 1$.

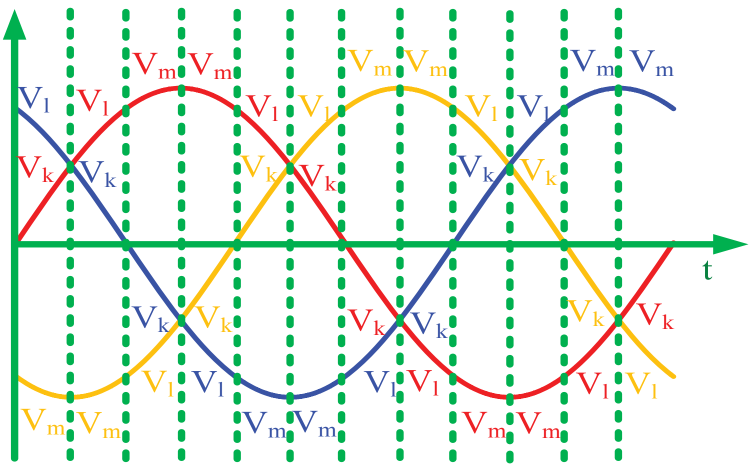

Figure 2.1: Distribution of V_k, V_l, V_m voltages with input phase voltages

Figure.2.1 shows the selection of V_k, V_l, V_m voltages with the input voltages over one input cycle of operation. The converter switching pattern depends only on the scalar comparison of input phase voltages and the instantaneous value of the desired output voltage. In a balanced three phase system, the summation of the three instantaneous phase voltages is zero. The duty ratio's of the switches are obtained as

$$\begin{aligned} d_l &= \frac{(V_0 - V_m)V_l}{V_k^2 + V_l^2 + V_m^2} = \frac{(V_0 - V_m)V_l}{1.5V_i^2} \\ d_k &= \frac{(V_0 - V_m)V_k}{1.5V_i^2} \\ d_m &= 1 - d_l - d_k \end{aligned} \tag{2.23}$$

Substituting eq.(2.23) in eq.(2.20) and solving the equations, the maximum voltage transfer ratio obtained as $G = \frac{V_o}{V_i} = 0.5$. Considering involvement of third harmonic component in voltage equations, the voltage gain (G) achieved using scalar method can be increased up to 0.866.

2.3 Carrier modulation

Carrier modulation technique is a basic modulation technique for any converter because of its simplicity and easy to implement. However in matrix converter, it requires variable sampling period approach for implementation [36] [39]- [41]. Consider indirect matrix converter, as shown in Figure.2.2, which is a combination of current source rectifier cascaded with voltage source inverter. Capacitive filters are connected at input terminals to filter out the input current harmonics generated due to switching. V_{pn} is the pseudo intermediate DC link voltage.

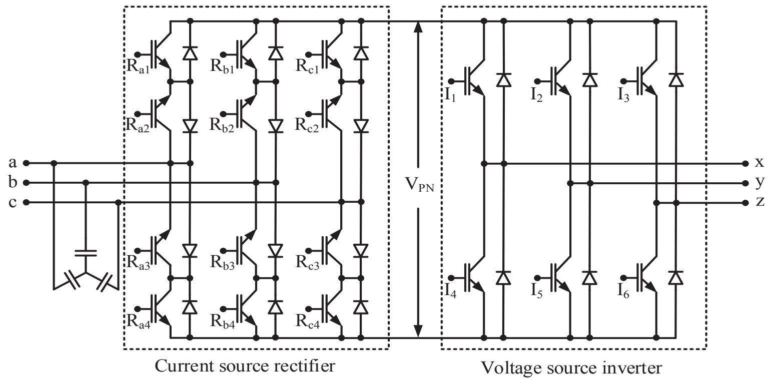

Figure 2.2: Indirect matrix converter

Balanced three phase voltages are supplied to the converter as given by eq.(2.24).

$$\begin{aligned} V_a &= V_i \cos(\theta_a) \\ V_b &= V_i \cos(\theta_b) \\ V_c &= V_i \cos(\theta_c) \end{aligned} \tag{2.24}$$

where V_i is the input voltage amplitude and $\theta_{a,b,c}$ is the respective phase angles.

Calculating duty ratio expression from above equation

$$V_a + V_b + V_c = 0 \tag{2.25}$$

$$-\frac{V_b}{V_a} - \frac{V_c}{V_a} = 1 \tag{2.26}$$

$$\delta_{ba} = -\frac{V_b}{V_a} = -\frac{cos(\theta_b)}{cos(\theta_a)},\ \delta_{ca} = -\frac{V_c}{V_a} = -\frac{cos(\theta_c)}{cos(\theta_a)} \tag{2.27}$$

Here δ_{ba}, δ_{ca} represents the duty ratios for switches in rectifier section to realise the pseudo DC link voltage V_{pn}. The δ_{ba} and δ_{ca} are function of $cos(\theta_a)$, which is periodic in nature whose value changes from -1 to 0 to 1 value. As $cos(\theta_a)$ tends to zero, duty ratios δ_{ba}, δ_{ca} approaches to infinite which is not possible. Due to this, eq.(2.27) is restricted to operate for one sixth of input cycle followed by $\delta_{ca}, \delta_{ab}, \delta_{cb}, \delta_{ac}, \delta_{bc}$ and this sequence will repeat for the remaining cycles. Duty ratio δ_{ba} means a phase is clamped to + of V_{pn} and b phase is connected to − of V_{pn} terminal through switches $R_{a1,a2}$ and $R_{b3,b4}$ respectively.

Further generalising the expressions for the entire one cycle of θ_a variation

$$\delta_1 = \begin{cases} -\frac{V_{min}}{V_{max}}, & \text{for + DC rail clamping} \\ -\frac{V_{max}}{V_{min}}, & \text{for − DC rail clamping} \end{cases} \quad \delta_2 = \begin{cases} -\frac{V_{mid}}{V_{max}}, & \text{for + DC rail clamping} \\ -\frac{V_{mid}}{V_{min}}, & \text{for − DC rail clamping} \end{cases} \tag{2.28}$$

where $V_{max} = max(V_a, V_b, V_c),\ V_{mid} = mid(V_a, V_b, V_c),\ V_{min} = min(V_a, V_b, V_c)$.

Normalised variation of V_{max},V_{mid} and V_{min} functions over one complete cycle of θ_a is shown in Figure.2.3. Similarly δ_1,δ_2 variation over one complete cycle of θ_a is shown in Figure.2.4. The generalised average DC link voltage V_{pn} is derived as

$$V_{pn} = \delta_1(V_{max} - V_{min}) + \delta_2(V_{max} - V_{mid}) \quad \text{for + DC rail clamping} \tag{2.29}$$

$$V_{pn} = \delta_1(V_{max} - V_{min}) + \delta_2(V_{mid} - V_{max}) \quad \text{for − DC rail clamping} \tag{2.30}$$

Simplifying eq.(2.29) and eq.(2.30) gives

$$V_{pn} = \frac{3V_i^2}{2|V_{max}|} \quad \text{for + DC rail clamping} \tag{2.31}$$

$$V_{pn} = \frac{3V_i^2}{2|V_{min}|} \quad \text{for − DC rail clamping} \tag{2.32}$$

Carrier based modulation for voltage source inverter section of indirect matrix converter is obtained by normalising output (V_o) references using eq.(2.31), eq.(2.32) and synchronising VSI carrier with CSR carrier. The resulting set of references ($V_o = V_x, V_y, V_z$), has a time varying modulation ratio $M(t)$ expressed as

$$M(t) = \frac{V_o}{(V_{pn}/2)} \tag{2.33}$$

$$V_x = \frac{V_o cos(\theta_x) + V_{off}}{(V_{pn}/2)} = M cos(\theta_x) + \frac{2V_{off}}{V_{pn}} \tag{2.34}$$

$$V_y = M cos(\theta_z) + \frac{2V_{off}}{V_{pn}} \tag{2.35}$$

$$V_z = M cos(\theta_z) + \frac{2V_{off}}{V_{pn}} \tag{2.36}$$

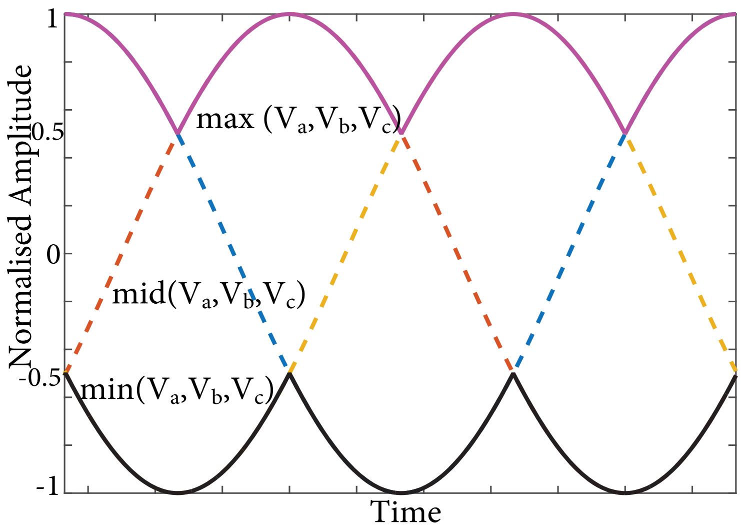

Figure 2.3: Normalised variations of max, mid and min function of input voltages

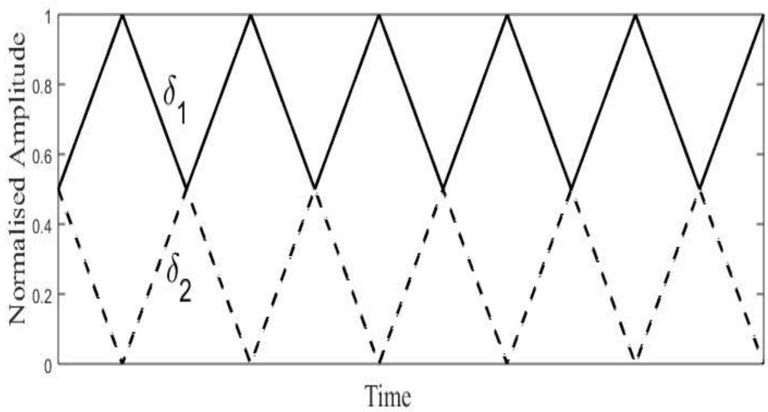

Figure 2.4: Variation of δ_1, δ_2

where $V_{x,y,z}$ is the normalised output references with phase angle $\theta_{x,y,z}$ and V_{off} is the triplen offset commonly added for enhanced maximum ratio of $\frac{2}{\sqrt{3}} = 1.15$.

Using these values the maximum input to output transfer gain is derived as $\frac{V_o}{V_i} = \frac{2}{\sqrt{3}} * \frac{3}{2} * \frac{1}{2} = \frac{\sqrt{3}}{2} = 0.866$, which is the theoretical maximum gain attainable by the matrix converter. Synchronisation between voltage source inverter (VSI) carrier with current source rectifier (CSR) switching states is illustrated in Figure.2.5. It is shown that the carrier used for VSI is different from CSR, since it has rising and falling triangular edges with constantly varying gradients. The intention for having different gradients is to force each triangular span to complete CSR switching duration expressed as either $\delta_1 T$ or $\delta_2 T$. A1 (*ppn*), A2 (*pnn*) are active states and N1 (*ppp*), N0 (*nnn*) are zero states for inverter section of matrix converter.

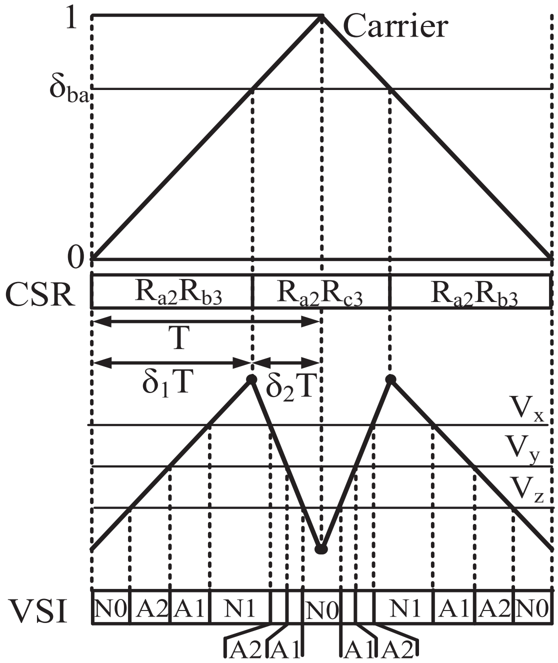

Figure 2.5: Carrier modulation

The main limitation of carrier modulation is to generate variable gradient carrier for VSI stage of the matrix converter. This has made carrier modulation less popular than SVM, which is state of the art modulation technique for matrix converter.

2.4 Space vector modulation

Initial work on SVM for matrix converter is presented by L. Huber [9], [42]. Space vector modulation technique for matrix converter (as shown in Figure.2.2) is explained by modulation of both voltage source inverter section and current source rectifier section.

2.4.1 Voltage source inverter

Standard two level voltage source inverter (VSI) consists of six switches with three output terminals (x, y, z) which are connected to DC bus (V_{pn}) as shown in Figure.2.6. Here I_1, I_2, I_3 are top end switches and I_4, I_5, I_6 are bottom end switches. The switching function is defined by $I_s = (n \text{ or } p)$, where $s = 1, 2, 3$. The switching function $I_s = p$ means that the corresponding output phase (x, y, z) is connected to the positive DC-bus p and $I_s = n$ means that the corresponding output phase is connected to the negative DC-bus n. Consequently, I_s can directly be considered as the control signal. The switching state of the VSI output stage can be described by

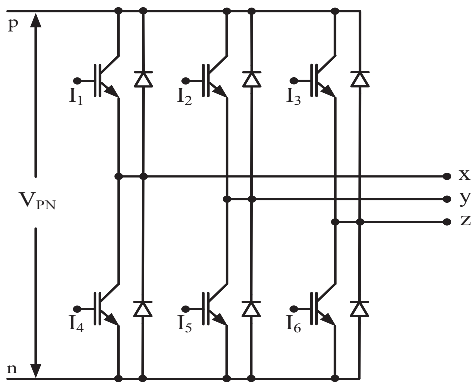

Figure 2.6: Voltage source inverter

(I_1, I_2, I_3), formed by the switching functions of the individual output phases or alternatively by replacing I_s with the corresponding connection to the DC-bus p or n. Space vector diagram for VSI has eight switching states i.e, $2^3 = 8$ where 2 represents number of input terminals and 3 represents number of output terminals. The switching states V_1(pnn), V_2(ppn), V_3(npn), V_4(npp), V_5(nnp), and V_6(pnp) are referred to as active states with a voltage space vector magnitude of $\frac{2}{3}V_{pn}$ obtained from $\left(|V^*| \angle\theta_v = \frac{2}{3}\left(e^{j0}V_x(t) + e^{j\left(\frac{2}{3}\pi\right)}V_y(t) + e^{j\left(\frac{4}{3}\pi\right)}V_z(t)\right)\right)$ and V_0(nnn), V_7(ppp) as zero or freewheeling states with a voltage space vector magnitude equal to zero, as shown in Figure.2.7.

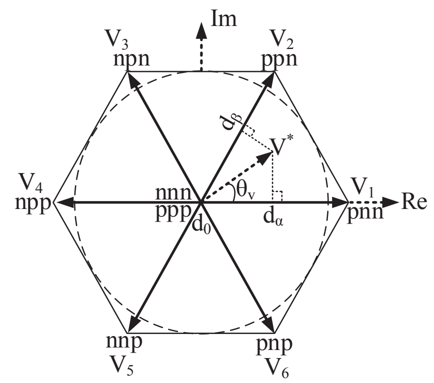

Figure 2.7: Voltage space vector (VSV) diagram

The reference output voltage space vector V^* is resultant of two adjacent voltage vectors. Mathematically, the output voltage space vector can be represented as follows:

In terms of duty ratio d_α and d_β corresponding to switching states V_1 and V_2, respectively, the projection of V^* on the real axis

$$d_\alpha V_1 + d_\beta V_2 cos(\frac{\pi}{3}) = V^* cos(\theta_v) \tag{2.37}$$

Likewise, projection of V^* on the imaginary axis

$$0 + d_\beta V_2 sin(\frac{\pi}{3}) = V^* sin(\theta_v) \tag{2.38}$$

On simplifying eq.(2.37) and eq.(2.38).

$$d_\alpha = m_v \frac{sin(\frac{\pi}{3} - \theta_v)}{sin(\frac{\pi}{3})} \tag{2.39}$$

$$d_\beta = m_v \frac{sin(\theta_v)}{sin(\frac{\pi}{3})} \tag{2.40}$$

where modulation index of inverter $m_v = \frac{\sqrt{3}V^*}{V_{pn}}$. Duty ratio corresponding to zero switching state is

$$d_0 = d_{ppp} = d_{nnn} = 1 - (d_\alpha + d_\beta) \tag{2.41}$$

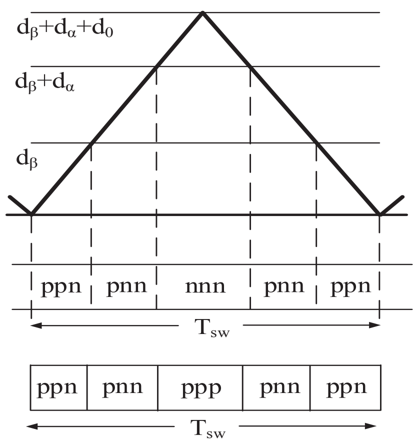

Figure 2.8: Signal generation case 1

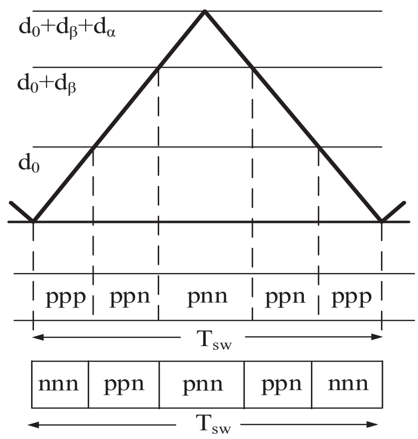

Figure 2.9: Signal generation case 2

By comparing duty ratio $d_\beta, d_\beta + d_\alpha, d_\beta + d_\alpha + d_0$ with carrier wave, the switching states for sector 1 can be generated, as shown in Figure.2.8. Similarly the shuffling of switching states in sector 1 can be obtained by comparing duty ratio $d_0, d_0 + d_\beta, d_0 + d_\beta + d_\alpha$ with carrier wave, as shown in Figure.2.9. Here triangular wave is chosen as a carrier wave to generate symmetrical switching. For sector 2, switching states d_α aligns with *pnn* while d_β aligns with *npn*. In this way, switching states for remaining sectors can be generated. Numerous cases are possible by sub dividing each duty ratio into half, quarter etc. consequently the switching frequency increases, as shown in Figure.2.10 and Figure.2.11.

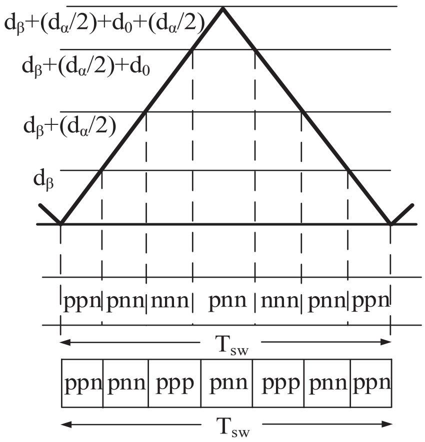

Figure 2.10: Signal generation case 3

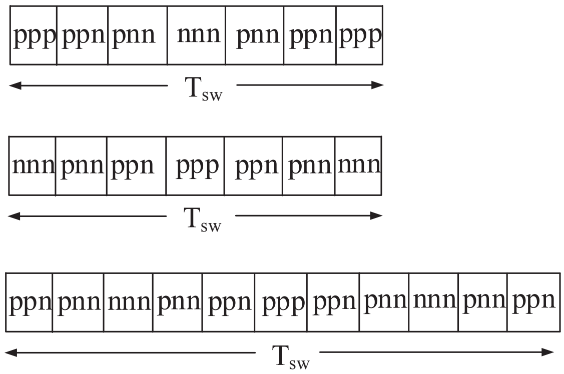

Figure 2.11: Different combination of switching states placement

2.4.2 Current source rectifier

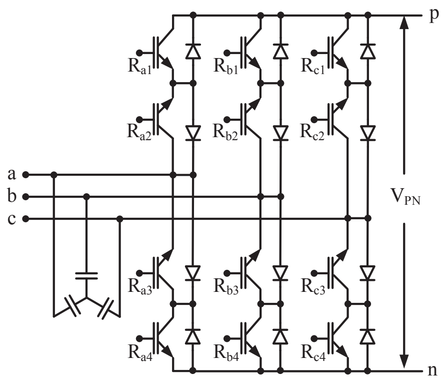

Figure 2.12: Current source rectifier

Current source rectifier (CSR) consists of 12 unidirectional switches represented by (R_{ij}) where $i = a, b, c$; $j = 1-4$, as shown in Figure.2.12, which can also be replaced by 6 bidirectional switches. Since it has 3 input terminals (a, b, c) and 2 output terminals (p, n), space vector diagram for CSR can have $3^2 = 9$ switching states in which 6 are active states and remaining 3 are zero states. Figure.2.13 shows the SVM for CSR with active vectors $I_{ab}, I_{ac}, I_{bc}, I_{ba}, I_{ca}, I_{cb}$ and zero vectors I_{aa}, I_{bb}, I_{cc}. The phasor I^* is the reference input current drawn from the source. The magnitude of active switching vectors are $\frac{2}{\sqrt{3}}I \left(\Rightarrow |I^*| \angle\theta_i = \frac{2}{3}\left(e^{j0}I_a(t) + e^{j\left(\frac{2}{3}\pi\right)}I_b(t) + e^{j\left(\frac{4}{3}\pi\right)}I_c(t)\right)\right)$and for zero

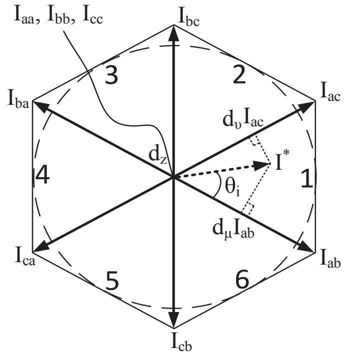

Figure 2.13: Current space vector (CSV) diagram

vectors it is 0. By projecting reference current space vector onto the adjacent active vectors the duty ratio can be obtained. The projection of I^* on the real axis

$$d_\mu I_{ab} cos(\frac{\pi}{6}) + d_\nu I_{ac} cos(\frac{\pi}{6}) = I^* cos(\theta_i - \frac{\pi}{6}) \tag{2.42}$$

Likewise, projection of I^* on the imaginary axis

$$- d_\mu I_{ab} cos(\frac{\pi}{3}) + d_\nu I_{ac} cos(\frac{\pi}{3}) = I^* sin(\theta_i - \frac{\pi}{6}) \tag{2.43}$$

On simplifying eq.(2.42) and eq.(2.43).

$$d_\mu = m_c \frac{sin(\frac{\pi}{3} - \theta_i)}{sin(\frac{\pi}{3})} \tag{2.44}$$

$$d_\nu = m_c \frac{sin(\theta_i)}{sin(\frac{\pi}{3})} \tag{2.45}$$

where $m_c = \frac{I^*}{I}$ = modulation index of rectifier.

$$d_z = d_{aa} = d_{bb} = d_{cc} = 1 - (d_\mu + d_\nu) \tag{2.46}$$

Comparing the duty ratio with carrier waveform the switching states can be generated as shown in Figure.2.14. Various combinations are possible to shuffle the switching states, for an example shown in Figure.2.15 compared to Figure.2.14. In addition, there is a possibility to utilize the active switching states only by eliminating zero switching states such that $d_\mu + d_\nu = 1 \Rightarrow m_c = \frac{1}{cos(\theta_i)}$. By substituting $m_c = \frac{1}{cos(\theta_i)}$ in eq.(2.44) and eq.(2.45), the modified duty ratios are obtained as given in eq.(2.47) and eq.(2.48). Hence, modulation index value of the rectifier is a function of θ_i and therefore separate control variable in terms of m_c is not required when only active vector combinations

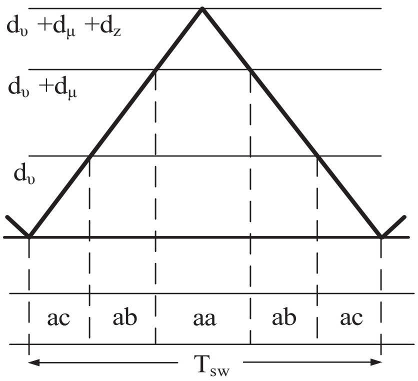

Figure 2.14: Signal generation for CSR case 1

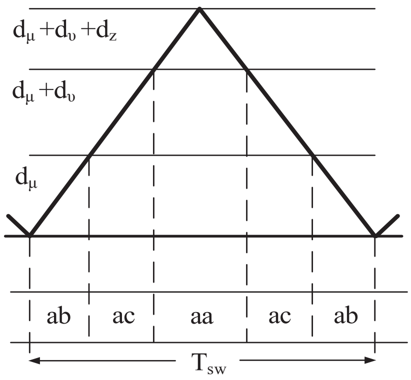

Figure 2.15: Signal generation for CSR case 2

are utilised. Corresponding switching states placement is shown in Figure.2.16.

$$d_{\mu}^{1} = \frac{sin(\frac{\pi}{3} - \theta_i)}{cos(\theta_i)sin(\frac{\pi}{3})} \tag{2.47}$$

$$d_{\nu}^{1} = \frac{sin(\theta_i)}{cos(\theta_i)sin(\frac{\pi}{3})} \tag{2.48}$$

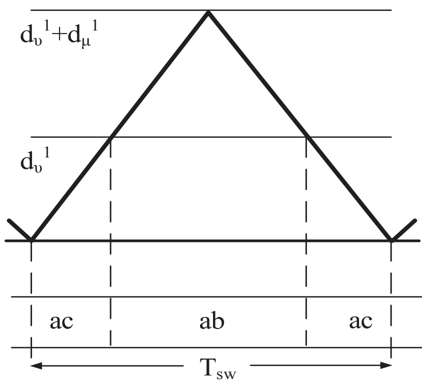

Figure 2.16: Signal generation for CSR without zero vector

2.5 Indirect matrix converter

In section 2.4, it is mentioned that indirect matrix converter (IMC) is a combination of current source rectifier cascaded with voltage source inverter. To generate the switching strategy for IMC, the CSV and VSV corresponding to current source rectifier and voltage source inverter need to coordinate with each other. This coordination is possible by superimposing CSV onto VSV or vice versa. By this coordinated switching, the current path drawn by the load from source would be done through CSR and VSI.

Two cases are possible with coordinated switching zero current switching and zero voltage switching.

2.5.1 Zero current switching

Figure.2.17 shows the superimposition of VSV onto the CSV. Considering a situation when both current and voltage vectors are lying in sector 1, voltage vectors V_1, V_2, V_0 from VSV will occupy a place within the length of vectors I_{ab}, I_{ac}, I_{aa} from CSV. Here $I_{ab,pnn}$ represents combination of *ab* state in rectifier with *pnn* state in inverter. The duty ratio of this combination is achieved by multiplying $d_\mu * d_\alpha \leftrightharpoons ab * pnn$. Similarly other duty ratios are given in eq.(2.49)

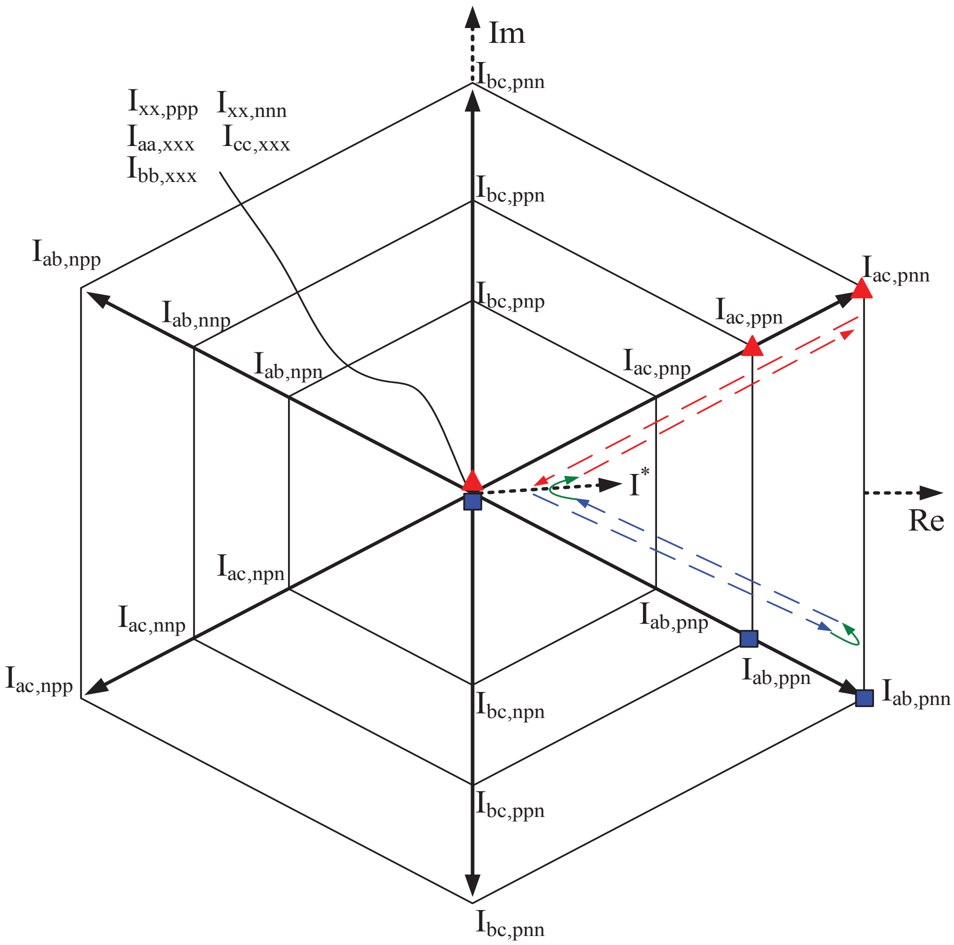

Figure 2.17: Zero current switching

$$
\begin{aligned}
&d_{\mu\alpha} = d_\mu d_\alpha, \quad d_{\nu\alpha} = d_\nu d_\alpha \\
&d_{\mu\beta} = d_\mu d_\beta, \quad d_{\nu\beta} = d_\nu d_\beta \\
&d_{\mu o} = d_\mu d_o, \quad d_{\nu o} = d_\nu d_o \\
&d_{z\alpha} = d_z d_\alpha, \quad d_{zo} = d_z d_o \\
&d_{z\beta} = d_z d_\beta
\end{aligned}
\tag{2.49}
$$

In Figure.2.18 the first row represents the rectifier switching states and the second row represents the voltage switching states. The transition of switching state in rectifier section from *ac* to *ab* is happening concurrently when inverter switching lies in *ppp* only. Here zero state (*ppp*) of inverter represents, load is not drawing any current from source. Since the transition from *ac* to *ab* is taking place at zero current, hence this combination (Figure.2.18) is zero current switching.

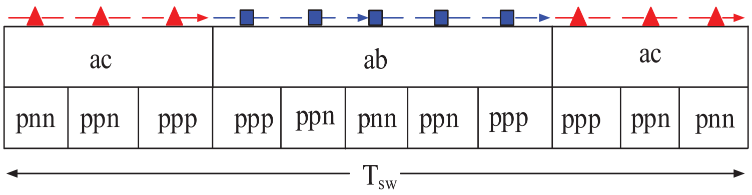

Figure 2.18: ZCS switching placement

2.5.2 Zero voltage switching

Similarly another combination is possible called as zero voltage switching, which can be obtained by superimposing CSV onto VSV as shown in Figure.2.19. The corresponding switching state placement is shown in Figure.2.20. The first row represents the rectifier switching states and the second row represents the voltage switching states. The transition of switching state in inverter section from *ppn* to *pnn* is happening while rectifier section remains in *aa* switching state. Here switching state *aa* represents rectifier section is not drawing current from supply rather providing a free wheeling path across V_{pn} terminals via p-R_{a1}-diode-diode-R_{a4}-n or n-diode-R_{a3}-R_{a2}-diode-p (Figure.2.13).

By utilizing the above switching states placements, commutation can be achieved at zero current and zero voltage at an instant. With SVM, parameters such as voltage transfer ratio, output frequency variation and input power factor correction can be easily controlled [42]. The main advantage of SVM over other modulations is to shuffle

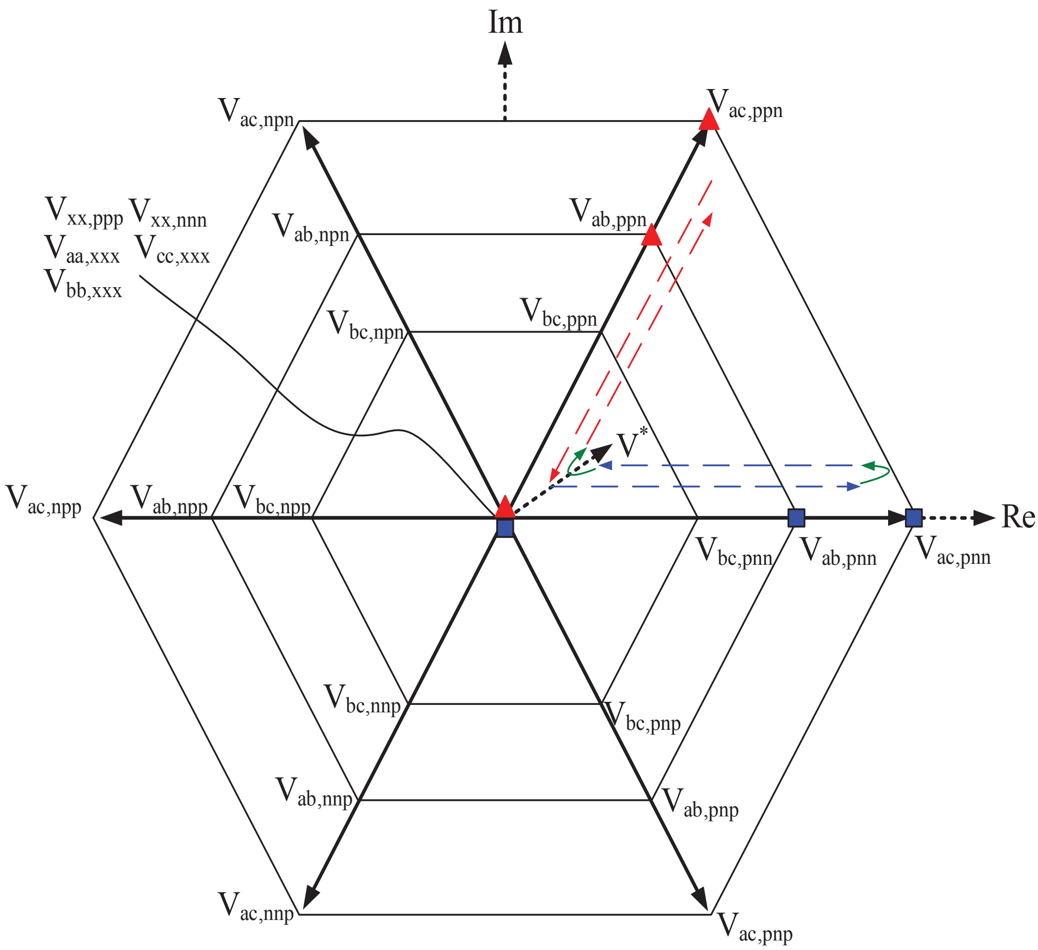

Figure 2.19: Zero voltage switching

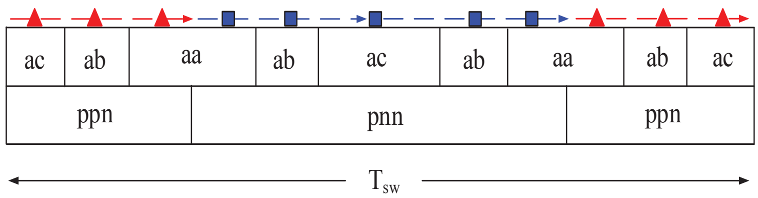

Figure 2.20: ZVS switching placement

the position of switching states in a switching period. Using this feature the common mode voltage reduction, switching loss minimization, reactive power transfer and single step commutation techniques can be implemented. For better understanding, the implementation of SVM for indirect matrix converter is presented in next section.

2.6 Real time implementation of SVM

Through out this dissertation, xilinx-field programmed gate array (Xilinx-FPGA) make NEXYS4 board is used as a processor for real time implementation of modulation techniques. FPGA is a flexible, reliable, dynamic and adaptable processor. As compared to the other processors, such as DSP, dSpace, PLCs. FPGA has parallel processing capability and higher clock frequency. Xilinx-FPGA understands binary coded files which can be generated through Xilinx vivado software. System Generator is add-on software platform with Xilinx vivado, which can be integrated with Matlab simulink environment having dedicated set of toolbox library for logic designs. System Generator creates an environment where models can be created using dedicated blocks which could further be converted into hardware description language (HDL), for use in a Vivado project.

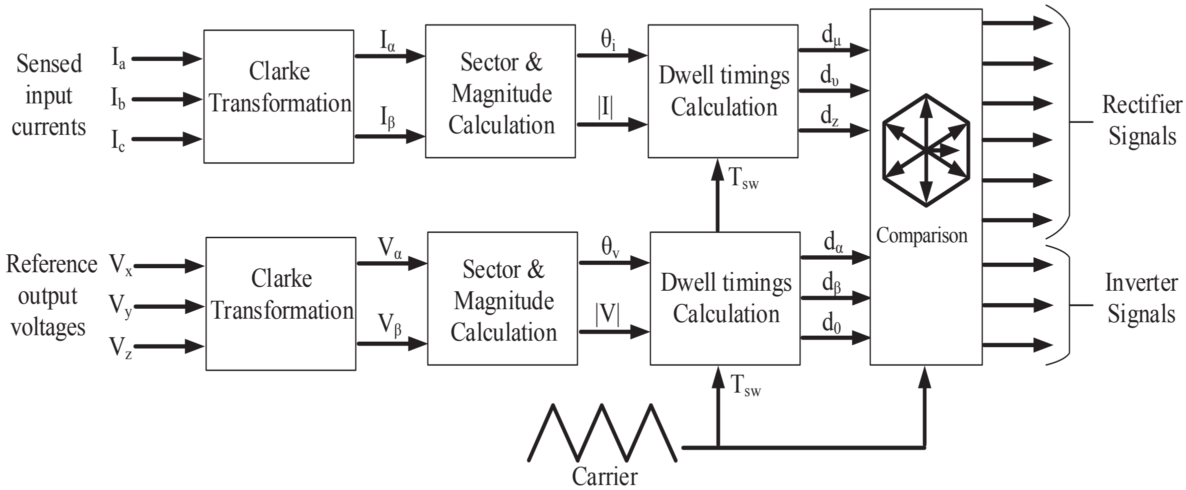

Figure 2.21: Flow of SVM technique for matrix converters

Work flow of Real time SVM for matrix converters is shown in Figure.2.21. To realise the implementation of SVM on system generator, it has been divided into sub-blocks for better understanding. Three analog to digital conversion (ADC) channels are used to obtained sensed input currents in digital form with the help of on board JXADC chip.

- *Clarke transformation*: It transforms the balanced three phase variables into two variables(along real-imaginary axes) using the equation given by eq.(2.50). To realise this equation in system generator, 'CMulit' and 'Addsub' blocks are used as shown in Figure.2.22. Where CMulit block is for constant multiplier and Addsub is used for both addition and subtraction operation. Similar approach is used for reference output voltages(V_x, V_y, V_z) to transform into V_α,V_β variables.

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{2.50}$$

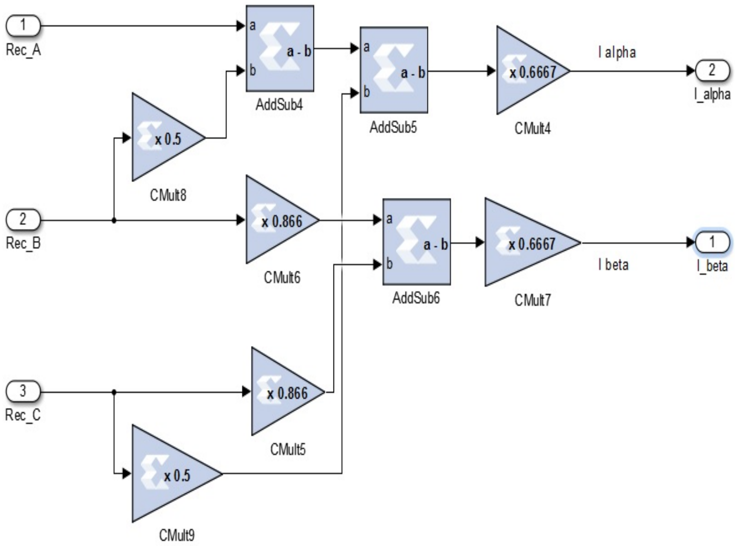

Figure 2.22: I_a, I_b, I_c transformed to I_α, I_β

- *Sector and magnitude calculation*: For rotational vector $I^* \Rightarrow |I|\angle\theta_i$ with angle θ_i and magnitude $|I|$ can be obtained with the variables I_α and I_β through the equations $\theta_i = tan^{-1}(\frac{I_\beta}{I_\alpha})$ and $|I| = \sqrt{I_\alpha^2 + I_\beta^2}$. In xilinx system generator, coordinate rotational digital computer algorithm (cordic) block can be used to obtain both θ_i and $|I|$ at a time. The variable θ_i, output will get in radians format. To adjust it in degree, a scaling factor ($\frac{180°}{\pi} = 57.3$) is used as shown in Figure.2.23. Sector identification can be done by comparing θ_i with constant values $0, 60, 120..$ as shown in Figure.2.24. For example $\theta_i > 0$ & $\theta_i \leq 60 \Rightarrow S_i = 1, \theta_i > 60$ & $\theta_i \leq 120 \Rightarrow S_i = 2$. Similar approach is done for calculating $\theta_v, |V|$ and their sector identification.

- *Dwell timings calculation*: Duty ratio's $(d_\mu, d_\nu, d_z, d_\alpha, d_\beta, d_0)$ are calculated by the equations given as eq.(2.39)-(2.46). Here duty ratio calculations are in the

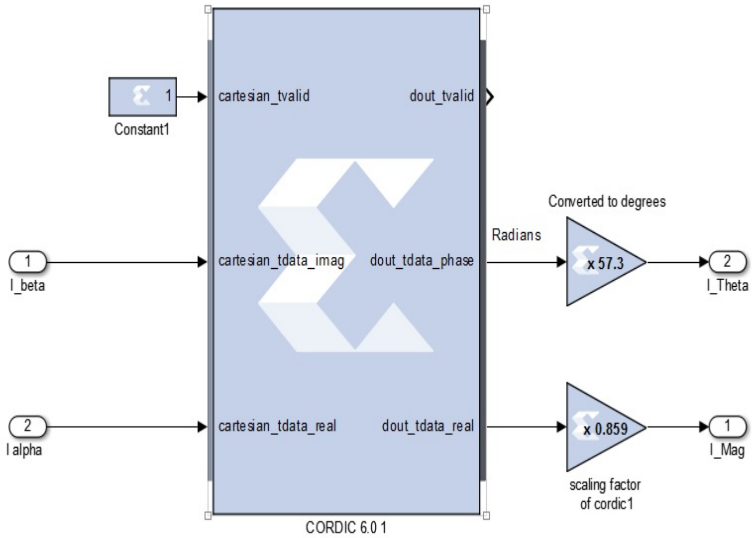

Figure 2.23: I_α, I_β converted to $\theta_i, |I|$

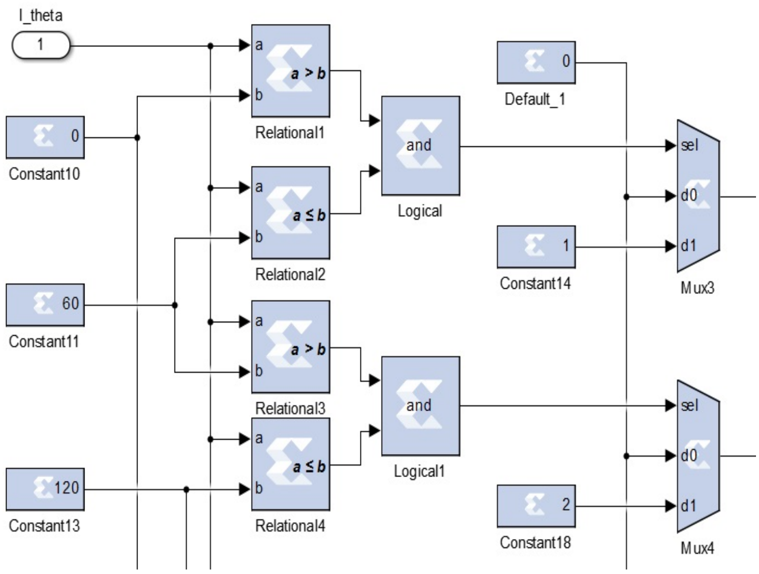

Figure 2.24: Sector calculation

form of trigonometric functions, which can also be realised with cordic block by selecting "sin and cos" from the drop down menu. The output of cordic block can be both $\cos\theta_i$ as a real value and $\sin\theta_i$ as an imaginary value. For example, to realise $di_1 = \cos(f)$ as the output, with input function $f(\theta, S_i) = \theta_i - (S_i - 1) * \frac{\pi}{3}$ is shown in Figure.2.25.

- *Comparison*: To implement zero current and zero voltage switching for matrix converters as explained in previous section requires a coordination in between duty ratio's d_μ, d_ν, d_z, d_α, d_β, d_0. For this, d_ν and d_α are multiplied together to

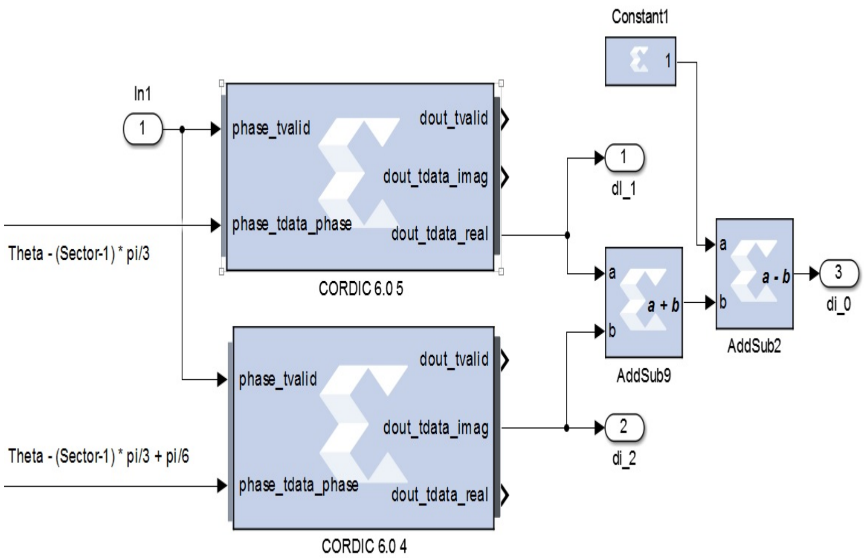

Figure 2.25: Duty calculation

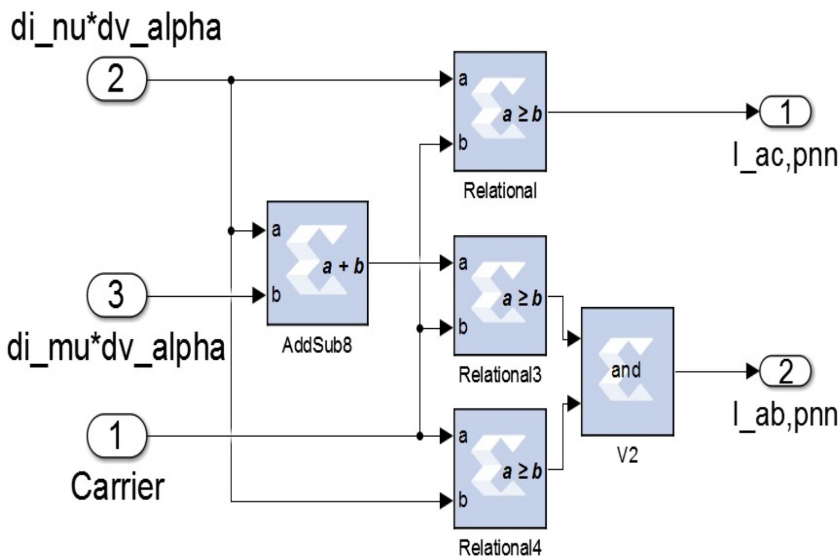

Figure 2.26: Duty ratio compared with carrier wave

form $d_\nu * d_\alpha$ which corresponds to I_{ac} state in rectifier section and pnn state in inverter section. The $d_\nu * d_\alpha$ is compared with carrier waveform (which is triangular in nature) to generate a command to activate corresponding switching state($I_{ac,pnn}$), as shown in Figure.2.26. Switching state $I_{ac,pnn}$, need to send a signal to corresponding switches. It can be possible by a 'constant' block with a storage value of 268 which is equivalent to binary value of 100001100 . In a string of bits 100001100, first six bits represents signals for rectifier switches and remaining three bits represents for inverter top end switches. {100001}

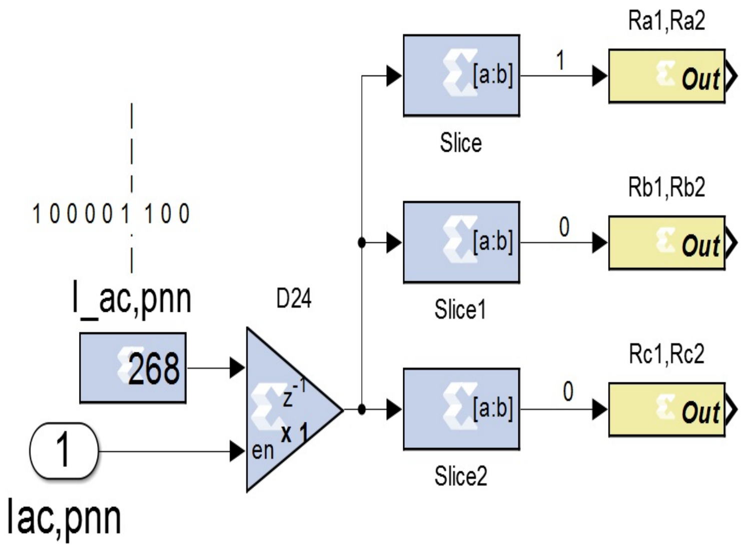

Figure 2.27: PWM generation

$\Rightarrow \{R_{a1-2}, R_{b1-2}, R_{c1-2}, R_{a3-4}, R_{b3-4}, R_{c3-4}\}$, here first bit 1 corresponds to turn ON R_{a1-2} switch, similarly second bit 0 corresponds to turn OFF R_{b1-2} switches. Remaining three bits in a string $\{100\} \Rightarrow \{I_1, I_2, I_3\}$, first bit 1 corresponds to turn ON I_1 switch. Signal generation for remaining switches $\{I_4, I_5, I_6\}$ can be obtained by complementing signals with $\{I_1, I_2, I_3\}$ switches. To extract single bit from a string, 'Slice' block is used. As shown in Figure.2.27, first three bits of 100001100 are extracted with slice block and assigned to output with three 'out' blocks.

Waveforms at each stage of implementation is provided at Appendix B

2.7 Conclusion

This chapter explains the implementation of SVM for indirect matrix converter. The inherent advantage of SVM is shown by shuffling the position of switching states [9]. In addition zero current commutation and zero voltage commutation techniques in IMC is explained [16], [43]. Real time implementation of SVM technique using FPGA processer is discussed using xilinx system generator library block sets.

The SVM discussed in this chapter will be considered as a benchmark for the proposed switched capacitor based USMC, which is presented in the next chapter for enhancing the voltage gain of USMC.