Appendix C

FPGA codes

C.1 Main code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library UNISIM;
use UNISIM.VCOMPONENTS.ALL;
entity design_1_wrapper is
  port (
    ad : out STD_LOGIC_VECTOR ( 0 to 0 );
    be : out STD_LOGIC_VECTOR ( 0 to 0 );
    cf : out STD_LOGIC_VECTOR ( 0 to 0 );
    clk : in STD_LOGIC;
    nst : out STD_LOGIC_VECTOR ( 0 to 0 );
    p : out STD_LOGIC_VECTOR ( 0 to 0 );
    q : out STD_LOGIC_VECTOR ( 0 to 0 );
    r : out STD_LOGIC_VECTOR ( 0 to 0 );
    s : out STD_LOGIC_VECTOR ( 0 to 0 );
    st : out STD_LOGIC_VECTOR ( 0 to 0 );
    t : out STD_LOGIC_VECTOR ( 0 to 0 );
    u : out STD_LOGIC_VECTOR ( 0 to 0 );
    vauxn10 : in STD_LOGIC;
    vauxn2 : in STD_LOGIC;
```

```
    vauxn3 : in STD_LOGIC;
    vauxp10 : in STD_LOGIC;
    vauxp2 : in STD_LOGIC;
    vauxp3 : in STD_LOGIC
  );
end design_1_wrapper;

architecture STRUCTURE of design_1_wrapper is
  component design_1 is
  port (
    be : out STD_LOGIC_VECTOR ( 0 to 0 );
    cf : out STD_LOGIC_VECTOR ( 0 to 0 );
    p : out STD_LOGIC_VECTOR ( 0 to 0 );
    t : out STD_LOGIC_VECTOR ( 0 to 0 );
    u : out STD_LOGIC_VECTOR ( 0 to 0 );
    q : out STD_LOGIC_VECTOR ( 0 to 0 );
    r : out STD_LOGIC_VECTOR ( 0 to 0 );
    s : out STD_LOGIC_VECTOR ( 0 to 0 );
    st : out STD_LOGIC_VECTOR ( 0 to 0 );
    ad : out STD_LOGIC_VECTOR ( 0 to 0 );
    nst : out STD_LOGIC_VECTOR ( 0 to 0 );
    clk : in STD_LOGIC;
    vauxp2 : in STD_LOGIC;
    vauxp3 : in STD_LOGIC;
    vauxn2 : in STD_LOGIC;
    vauxp10 : in STD_LOGIC;
    vauxn3 : in STD_LOGIC;
    vauxn10 : in STD_LOGIC
  );
  end component design_1;
begin
design_1_i: component design_1
```

```
     port map (
      ad(0) => ad(0),
      be(0) => be(0),
      cf(0) => cf(0),
      clk => clk,
      nst(0) => nst(0),
      p(0) => p(0),
      q(0) => q(0),
      r(0) => r(0),
      s(0) => s(0),
      st(0) => st(0),
      t(0) => t(0),
      u(0) => u(0),
      vauxn10 => vauxn10,
      vauxn2 => vauxn2,
      vauxn3 => vauxn3,
      vauxp10 => vauxp10,
      vauxp2 => vauxp2,
      vauxp3 => vauxp3
    );
end STRUCTURE;
```

C.2 sub code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library UNISIM;
use UNISIM.VCOMPONENTS.ALL;
entity design_1 is
  port (
    ad : out STD_LOGIC_VECTOR ( 0 to 0 );
    be : out STD_LOGIC_VECTOR ( 0 to 0 );
```

```
    cf : out STD_LOGIC_VECTOR ( 0 to 0 );
    clk : in STD_LOGIC;
    nst : out STD_LOGIC_VECTOR ( 0 to 0 );
    p : out STD_LOGIC_VECTOR ( 0 to 0 );
    q : out STD_LOGIC_VECTOR ( 0 to 0 );
    r : out STD_LOGIC_VECTOR ( 0 to 0 );
    s : out STD_LOGIC_VECTOR ( 0 to 0 );
    st : out STD_LOGIC_VECTOR ( 0 to 0 );
    t : out STD_LOGIC_VECTOR ( 0 to 0 );
    u : out STD_LOGIC_VECTOR ( 0 to 0 );
    vauxn10 : in STD_LOGIC;
    vauxn2 : in STD_LOGIC;
    vauxn3 : in STD_LOGIC;
    vauxp10 : in STD_LOGIC;
    vauxp2 : in STD_LOGIC;
    vauxp3 : in STD_LOGIC
  );
  attribute CORE_GENERATION_INFO : string;
  attribute CORE_GENERATION_INFO of design_1 : entity is "design_1,IP_Integrator,{x_ip}"
  attribute HW_HANDOFF : string;
  attribute HW_HANDOFF of design_1 : entity is "design_1.hwdef";
end design_1;

architecture STRUCTURE of design_1 is
  component design_1_timeforxadcn_0_0 is
  port (
    clk : in STD_LOGIC;
    vauxp2 : in STD_LOGIC;
    vauxn2 : in STD_LOGIC;
    vauxp3 : in STD_LOGIC;
    vauxn3 : in STD_LOGIC;
    vauxp10 : in STD_LOGIC;
```

```
  vauxn10 : in STD_LOGIC;
  CH2 : out STD_LOGIC_VECTOR ( 11 downto 0 );
  CH3 : out STD_LOGIC_VECTOR ( 11 downto 0 );
  CH10 : out STD_LOGIC_VECTOR ( 11 downto 0 )
);
end component design_1_timeforxadcn_0_0;
component design_1_sant_int_3m_1_0_0 is
port (
  cw : in STD_LOGIC_VECTOR ( 15 downto 0 );
  i_a : in STD_LOGIC_VECTOR ( 11 downto 0 );
  i_b : in STD_LOGIC_VECTOR ( 11 downto 0 );
  i_c : in STD_LOGIC_VECTOR ( 11 downto 0 );
  r_a : in STD_LOGIC_VECTOR ( 11 downto 0 );
  r_b : in STD_LOGIC_VECTOR ( 11 downto 0 );
  r_c : in STD_LOGIC_VECTOR ( 11 downto 0 );
  clk : in STD_LOGIC;
  ad : out STD_LOGIC_VECTOR ( 0 to 0 );
  be : out STD_LOGIC_VECTOR ( 0 to 0 );
  cf : out STD_LOGIC_VECTOR ( 0 to 0 );
  p : out STD_LOGIC_VECTOR ( 0 to 0 );
  q : out STD_LOGIC_VECTOR ( 0 to 0 );
  r : out STD_LOGIC_VECTOR ( 0 to 0 );
  s : out STD_LOGIC_VECTOR ( 0 to 0 );
  st : out STD_LOGIC_VECTOR ( 0 to 0 );
  t : out STD_LOGIC_VECTOR ( 0 to 0 );
  u : out STD_LOGIC_VECTOR ( 0 to 0 );
  nst : out STD_LOGIC_VECTOR ( 0 to 0 )
);
end component design_1_sant_int_3m_1_0_0;
component design_1_sin100_tri_in_m_0_0 is
port (
  clk : in STD_LOGIC;
```

```
    a : out STD_LOGIC_VECTOR ( 11 downto 0 );
    b : out STD_LOGIC_VECTOR ( 11 downto 0 );
    c : out STD_LOGIC_VECTOR ( 11 downto 0 );
    cw : out STD_LOGIC_VECTOR ( 15 downto 0 )
  );
  end component design_1_sin100_tri_in_m_0_0;
  signal clk_1 : STD_LOGIC;
  signal sant_int_3m_1_0_ad : STD_LOGIC_VECTOR ( 0 to 0 );
  signal sant_int_3m_1_0_be : STD_LOGIC_VECTOR ( 0 to 0 );
  signal sant_int_3m_1_0_cf : STD_LOGIC_VECTOR ( 0 to 0 );
  signal sant_int_3m_1_0_nst : STD_LOGIC_VECTOR ( 0 to 0 );
  signal sant_int_3m_1_0_p : STD_LOGIC_VECTOR ( 0 to 0 );
  signal sant_int_3m_1_0_q : STD_LOGIC_VECTOR ( 0 to 0 );
  signal sant_int_3m_1_0_r : STD_LOGIC_VECTOR ( 0 to 0 );
  signal sant_int_3m_1_0_s : STD_LOGIC_VECTOR ( 0 to 0 );
  signal sant_int_3m_1_0_st : STD_LOGIC_VECTOR ( 0 to 0 );
  signal sant_int_3m_1_0_t : STD_LOGIC_VECTOR ( 0 to 0 );
  signal sant_int_3m_1_0_u : STD_LOGIC_VECTOR ( 0 to 0 );
  signal sin100_tri_in_m_0_a : STD_LOGIC_VECTOR ( 11 downto 0 );
  signal sin100_tri_in_m_0_b : STD_LOGIC_VECTOR ( 11 downto 0 );
  signal sin100_tri_in_m_0_c : STD_LOGIC_VECTOR ( 11 downto 0 );
  signal sin100_tri_in_m_0_cw : STD_LOGIC_VECTOR ( 15 downto 0 );
  signal timeforxadcn_0_CH10 : STD_LOGIC_VECTOR ( 11 downto 0 );
  signal timeforxadcn_0_CH2 : STD_LOGIC_VECTOR ( 11 downto 0 );
  signal timeforxadcn_0_CH3 : STD_LOGIC_VECTOR ( 11 downto 0 );
  signal vauxn10_1 : STD_LOGIC;
  signal vauxn2_1 : STD_LOGIC;
  signal vauxn3_1 : STD_LOGIC;
  signal vauxp10_1 : STD_LOGIC;
  signal vauxp2_1 : STD_LOGIC;
  signal vauxp3_1 : STD_LOGIC;
begin
```

```
  ad(0) <= sant_int_3m_1_0_ad(0);
  be(0) <= sant_int_3m_1_0_be(0);
  cf(0) <= sant_int_3m_1_0_cf(0);
  clk_1 <= clk;
  nst(0) <= sant_int_3m_1_0_nst(0);
  p(0) <= sant_int_3m_1_0_p(0);
  q(0) <= sant_int_3m_1_0_q(0);
  r(0) <= sant_int_3m_1_0_r(0);
  s(0) <= sant_int_3m_1_0_s(0);
  st(0) <= sant_int_3m_1_0_st(0);
  t(0) <= sant_int_3m_1_0_t(0);
  u(0) <= sant_int_3m_1_0_u(0);
  vauxn10_1 <= vauxn10;
  vauxn2_1 <= vauxn2;
  vauxn3_1 <= vauxn3;
  vauxp10_1 <= vauxp10;
  vauxp2_1 <= vauxp2;
  vauxp3_1 <= vauxp3;
sant_int_3m_1_0: component design_1_sant_int_3m_1_0_0
     port map (
      ad(0) => sant_int_3m_1_0_ad(0),
      be(0) => sant_int_3m_1_0_be(0),
      cf(0) => sant_int_3m_1_0_cf(0),
      clk => clk_1,
      cw(15 downto 0) => sin100_tri_in_m_0_cw(15 downto 0),
      i_a(11 downto 0) => sin100_tri_in_m_0_a(11 downto 0),
      i_b(11 downto 0) => sin100_tri_in_m_0_b(11 downto 0),
      i_c(11 downto 0) => sin100_tri_in_m_0_c(11 downto 0),
      nst(0) => sant_int_3m_1_0_nst(0),
      p(0) => sant_int_3m_1_0_p(0),
      q(0) => sant_int_3m_1_0_q(0),
      r(0) => sant_int_3m_1_0_r(0),
```

```
      r_a(11 downto 0) => timeforxadcn_0_CH2(11 downto 0),
      r_b(11 downto 0) => timeforxadcn_0_CH3(11 downto 0),
      r_c(11 downto 0) => timeforxadcn_0_CH10(11 downto 0),
      s(0) => sant_int_3m_1_0_s(0),
      st(0) => sant_int_3m_1_0_st(0),
      t(0) => sant_int_3m_1_0_t(0),
      u(0) => sant_int_3m_1_0_u(0)
    );
sin100_tri_in_m_0: component design_1_sin100_tri_in_m_0_0
     port map (
      a(11 downto 0) => sin100_tri_in_m_0_a(11 downto 0),
      b(11 downto 0) => sin100_tri_in_m_0_b(11 downto 0),
      c(11 downto 0) => sin100_tri_in_m_0_c(11 downto 0),
      clk => clk_1,
      cw(15 downto 0) => sin100_tri_in_m_0_cw(15 downto 0)
    );
timeforxadcn_0: component design_1_timeforxadcn_0_0
     port map (
      CH10(11 downto 0) => timeforxadcn_0_CH10(11 downto 0),
      CH2(11 downto 0) => timeforxadcn_0_CH2(11 downto 0),
      CH3(11 downto 0) => timeforxadcn_0_CH3(11 downto 0),
      clk => clk_1,
      vauxn10 => vauxn10_1,
      vauxn2 => vauxn2_1,
      vauxn3 => vauxn3_1,
      vauxp10 => vauxp10_1,
      vauxp2 => vauxp2_1,
      vauxp3 => vauxp3_1
    );
end STRUCTURE;
```