Appendix B

Waveforms at each stage implementation of SVM
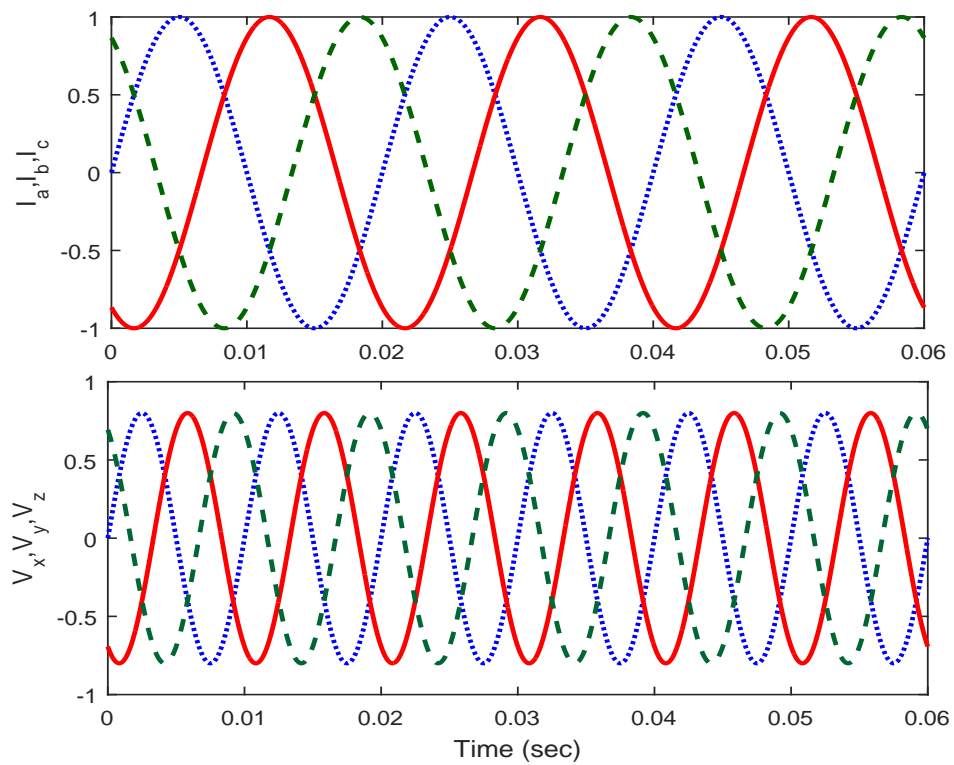

Figure B.1: Input currents$(50Hz)$(top) and desired output voltages$(100Hz)$(bottom)
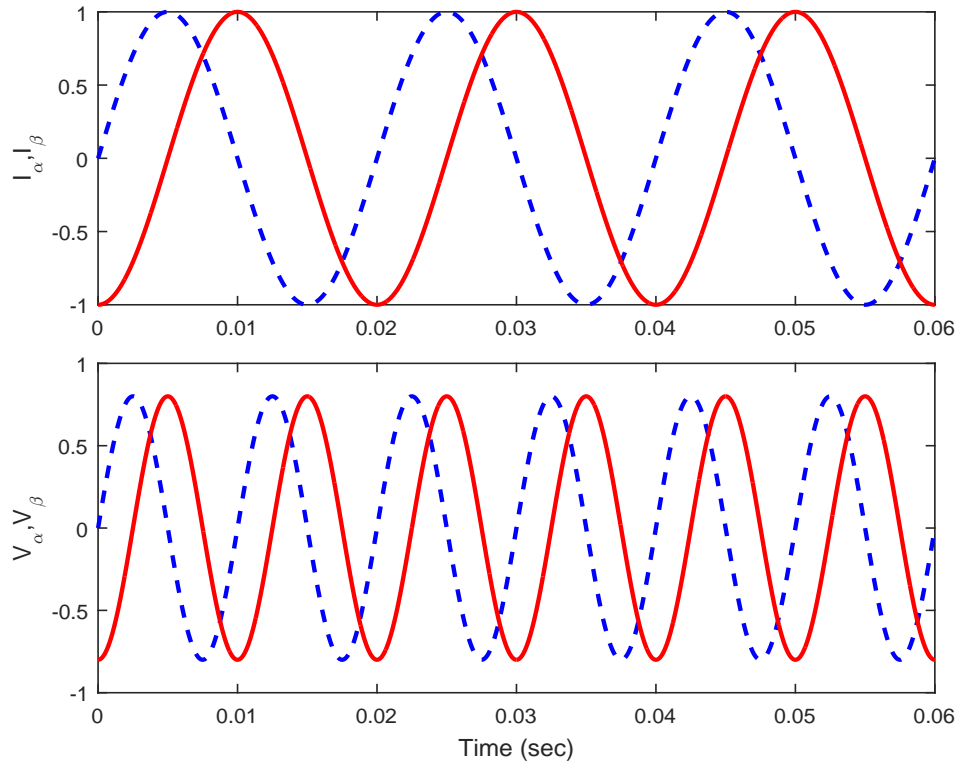
Figure B.2: I_α, I_β(top) and V_α, V_β(bottom)

Figure B.3: Theta θ_i(top) and θ_v(bottom)
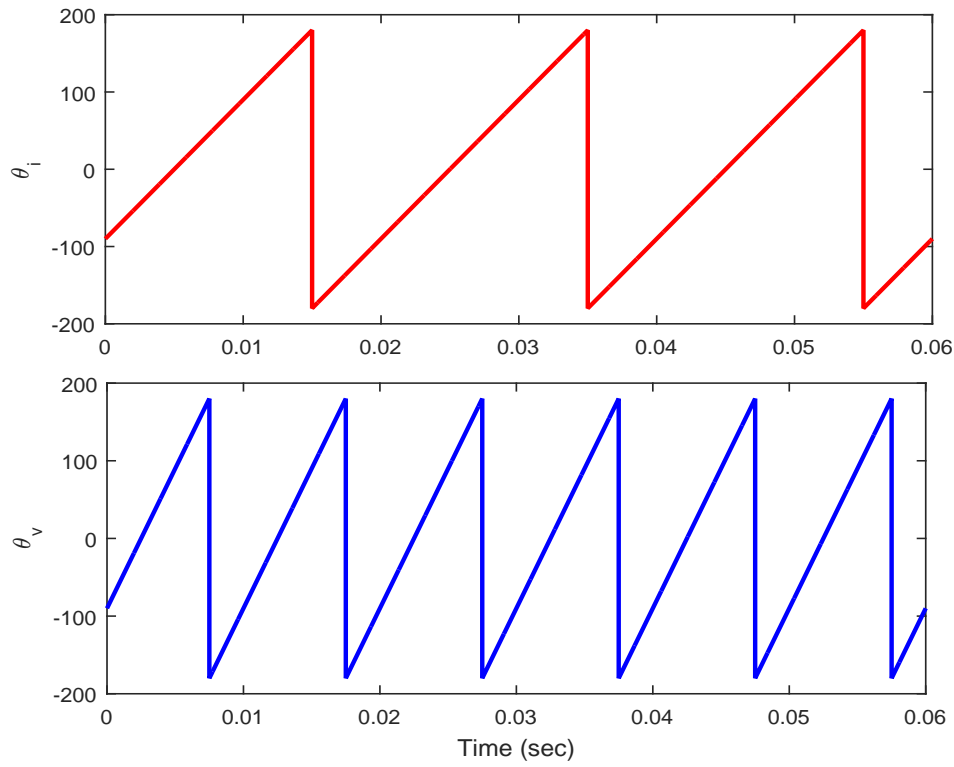
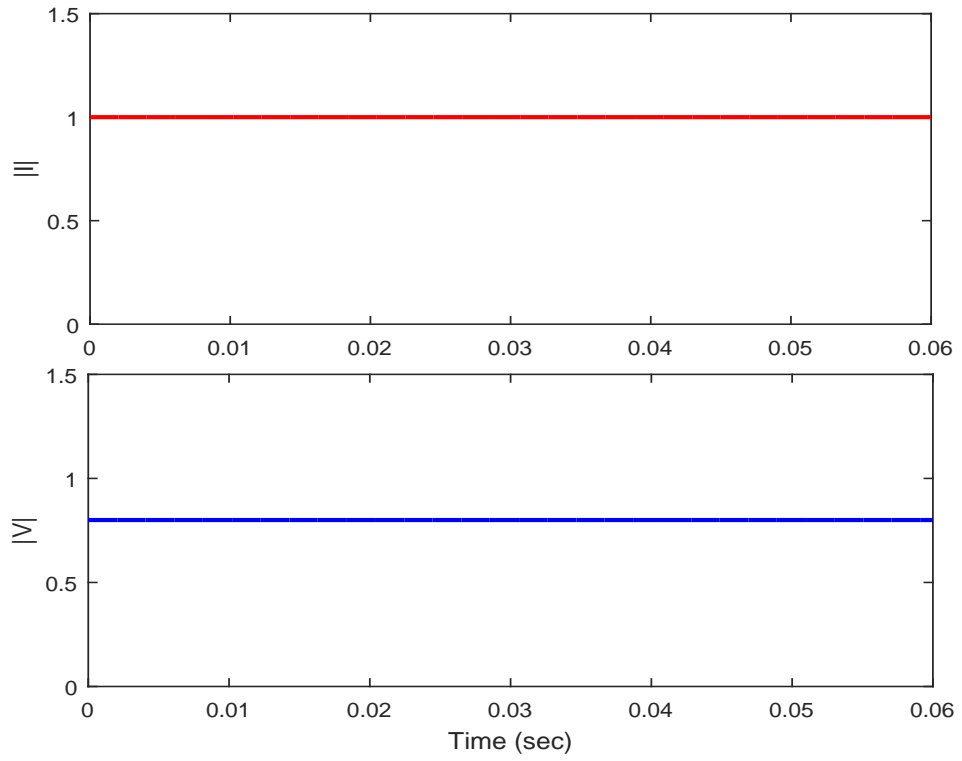**Figure B.4:** Magnitudes $|I|$(top) and $|V|$(bottom)
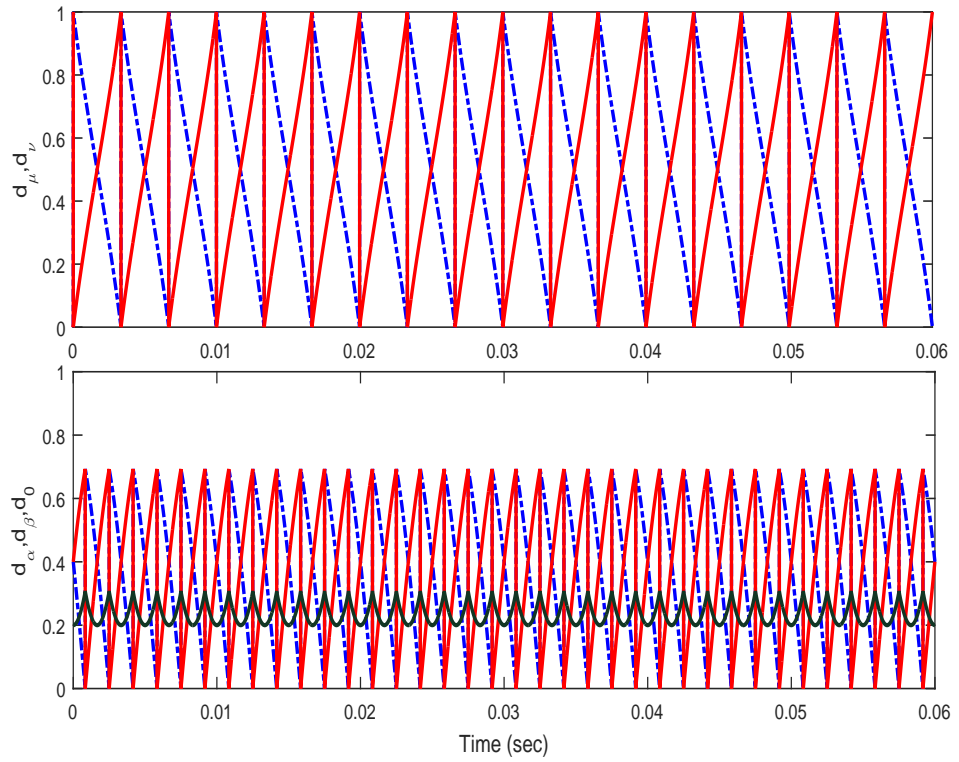
Figure B.5: Duty ratio's $[d_\mu$(red)$,d_\nu$(blue)](top) and $[d_\alpha$(red)$,d_\beta$(blue)$,d_0$(green)](bottom)
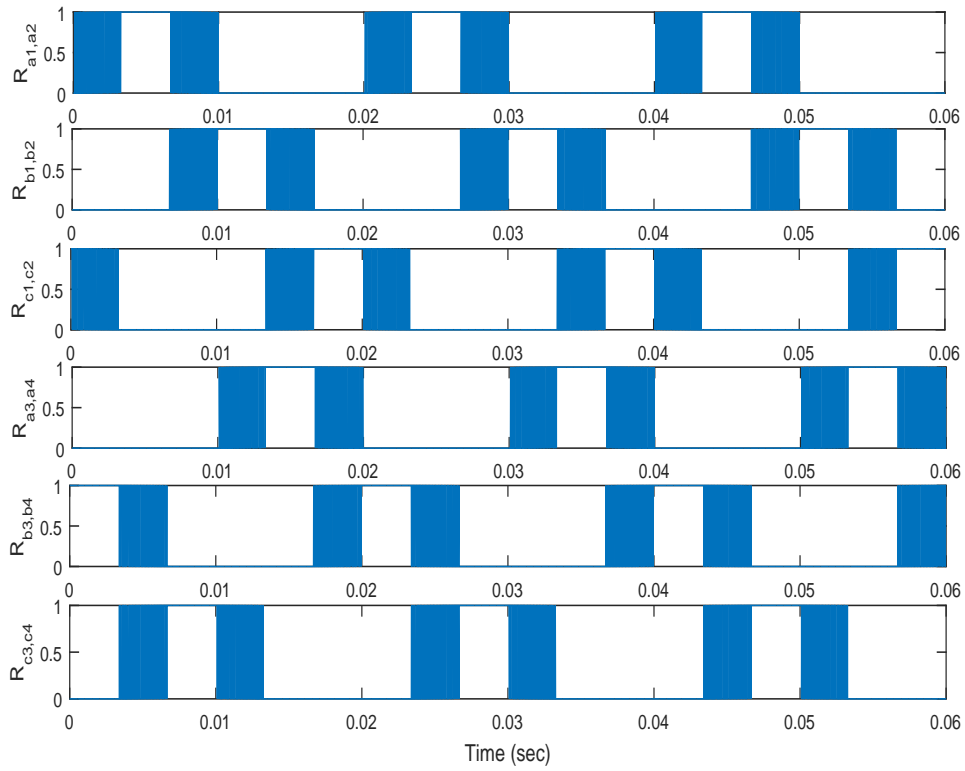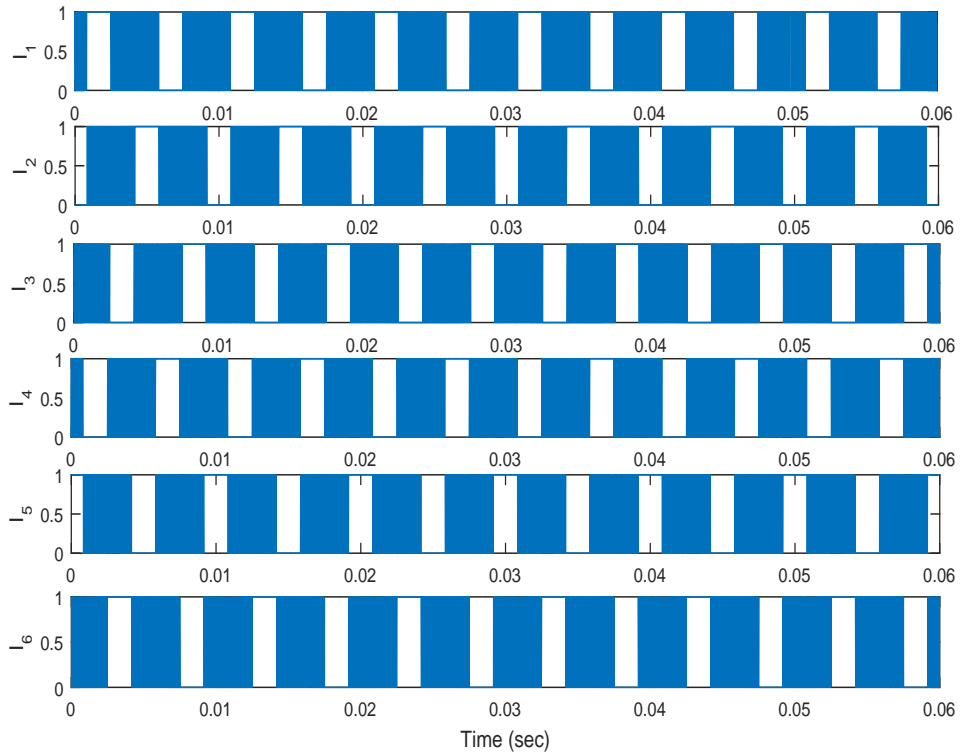
Figure B.6: Rectifier switching signals

Figure B.7: Inverter switching signals

122