Chapter 5

5.1 Introduction

In the twenty-first century, graphene, a single layer two dimensional (2D) allotrope of carbon atoms, has attracted immense attention in the electronics world due to its unusually high carrier mobility.[186, 187] Along with this, it's chemical stability, lightweight, and excellent optoelectronic properties have added more flavor to explore this material in different areas of electronics.[74] However, unlike conventional semiconductors, large-area single-layer graphene (SLG) is semimetal in nature with zero band gap.[74] The valence and conduction bands of SLG meet to form a cone-shaped at the K points (named Dirac point) of the Brillouin zone.[188] Because of having zero band gap, field-effect transistors (FETs) made off with larger channel length cannot be switched off, which makes it unsuitable for logic applications.[74, 189] The large channel length devices can be used in power handling owing to its efficient operation at higher voltage without breaking down the junction and also have low noise, which is very beneficial for analog devices. Long channel length devices are promising in many areas, such as for light sensing (photodetector), sensing of bio-analytes (biosensor), etc.[190, 191] Unfortunately, long channel length graphene devices are not common due to its semi-metallic nature, which limits the use of graphene as a semiconductor in FETs, photodetector, sensor, etc. Hence, the opening of bandgap in graphene is a crucial step for its realistic application. To date, several efforts have been made to open the band gap in graphene. Mainly three types of efforts have been reported: by confining electron in quasi one- dimensional graphene nanoribbons,[192, 193] through biasing of bilayer graphene[194-196] and by applying strain to graphene through dual-gate biasing.[197, 198] In addition to

these three major efforts, ionic or molecular-doping and chemical functionalization have also been reported for the opening band gap in SLG.[199-201] Particularly, a number of theoretical[202, 203] and experimental studies[204, 205] suggest that lithium-ion (Li^+) intercalation can open band gap of ~0.85 eV in SLG, which is very encouraging for graphene logic circuit in future.[206] However, the effect of such kind of Li^+ incorporation in SLG transistor has not been experimentally verified.

Besides the bandgap issue, till date fabrication method of GFETs is also very expensive and tedious. In most of the earlier reported GFETs work, only different lithography processes had been employed to fabricate source/drain contact in the micrometer or lesser sized channel length (L) FETs, which is costly and time-consuming process. For cost-effective fabrication like printing or physical vapor deposited (PVD) shadow mask process can reach up to several 10 μm channel length. However, due to the semimetal nature of graphene, it is practically not possible to fabricate such a large channel length GFET by using these deposition methods.[207] Therefore, instead of a large number of reports on GFET, we hardly found any cost-effective GFET fabrication for large-area applications. Thus, a new technique should be adopted to fabricate devices for the 2D system (e.g., graphene), which is different from the conventional wet-chemistry based photolithography that leads to the adverse effects on the novel properties of graphene.

In this thesis chapter, I have described a simple, cost-effective method to fabricate large channel length SLG thin film transistor that shows good current saturation with low operating voltage. Both the low operation voltage and the current saturation of GFET has been achieved by utilizing the Li^+ ion of ion-conducting Li_5AlO_4 gate dielectric. Large area graphene has been grown by conventional chemical vapor deposition (CVD) method and ion-

conducting Li_5AlO_4 by the sol-gel method. Silver electrode (Ag) with a molybdenum oxide (MoO_x) interface has been used as a source and drain electrode that has been deposited by a thermal evaporation process. Distance between source and drain was taken as large as in mm scale that has been varied from 0.2 mm to 5.7 mm. All of these GFETs show typical p-channel transport with an optimum device performance by a GFET of channel length1.65 mm. For comparison, such kind of mm-scale channel length GFETs have been fabricated using conventional SiO_2 gate dielectric, and none of them show any significant variation of drain voltage even with a very high variation of gate voltage. This comparison indicates that the mobile Li^+ ion of Li_5AlO_4 gate dielectric is playing the key role in the current saturation of the devices.

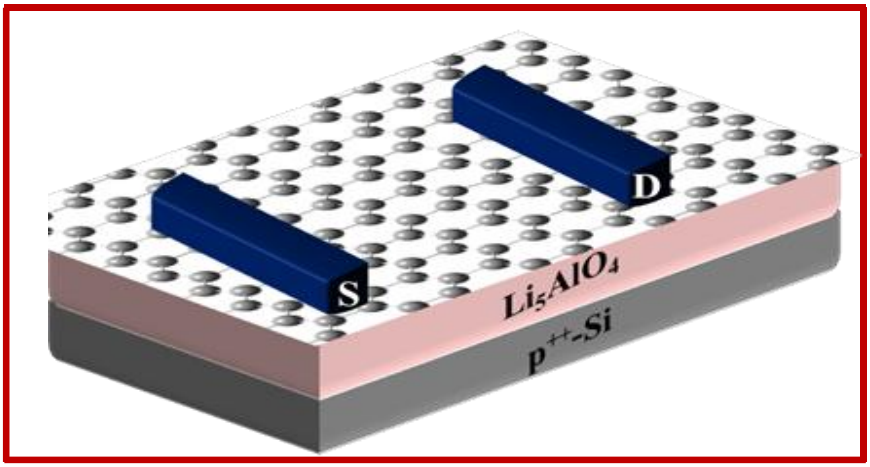

Figure 5.1: *Schematic illustration showing the fabricated GFET device.*

5.2 Experimental

5.2.1 Synthesis of graphene

Large-scale, high-quality graphene film was grown on Cu substrate (thickness 25 µm, purity 99.8%, Alfa Aesar) through liquid precursor based chemical vapor deposition (CVD) technique.[208, 209] Prior to the loading of Cu substrate (2 x 2 cm^2) into the CVD chamber,

it was cleaned in an ultrasonic bath by using organic solvents (acetone and isopropanol). After loading the cleaned Cu substrate into a quartz tubular furnace of diameter 2 inches, it was purged with hydrogen (H_2) gas at a constant flow rate of 100 sccm through mass flow controller (MFC, Alicat Scientific, USA). Then the temperature of the furnace was raised to the process temperature of 980 ºC under a constant heating rate of 20 ºC/min. Before the growth process, Cu foil was annealed for 30 min at 980 ºC. Further, the growth of graphene was started by injecting vapor of organic liquid n-hexane (Molychem, India, as a liquid precursor for carbon) for 4 min into the furnace. After completion of the reaction, the furnace was cooled down to room temperature under the ambiance of high purity (99.95%) H_2 gas.

5.2.2 Transfer of graphene

In order to carry out the structural/ morphological characterizations and device fabrication, graphene grown on Cu substrate was transferred on dielectric-coated highly doped silicon (p^+-Si) or conventional p^+-Si/SiO_2 substrate. In the typical transferring process, Cu substrate with 'as grown' graphene was spin-coated with poly-methyl methacrylate (PMMA) solution at 1000 rpm for 1 min, followed by baking at 100 ºC for 5 min. Further, graphene supported with PMMA film was separated from Cu foil by etching out the Cu in dilute nitric acid (10% HNO_3) solution. The graphene layer supported with PMMA was carefully washed multiple times in DI water and is then fished out on the desired substrate. Finally, the PMMA film was easily removed through acetone, leaving behind a good quality graphene layer on the substrate.

5.2.3 Material synthesis for dielectric thin film

As mentioned earlier, GFETs was fabricated on top of an ionic dielectric that contains mobile Li^+ ion **(figure 5.1)**. This ionic dielectric has been synthesized by low cost and environment-

friendly sol-gel techniques.[210] Specifically, in this work, the crystalline Li_5AlO_4 gate dielectric has been used that plays a key role in reducing the operating voltage within 2V. The synthesis and the deposition method of this dielectric for the application of low operating voltage transistor fabrication have been reported earlier by our group.[97] In this synthesis process, aluminum tri secondary butoxide [$Al(OC_4H_9)_3$] and lithium acetate (CH_3COOLi) have been used as precursor materials. To begin this process, a precursor sol of alumina with 300 mM concentration was prepared by Yoldas process [211, 212]. A separate lithium acetate solution of 300 mM was prepared by using 2-methoxy ethanol as solvent. Afterward, these two precursor solutions were mixed to each other with the desired amount to maintain the ratio of Li and Al of 5:1 in the final ceramic product. The mixture was stirred for 30 minutes under ambient atmosphere and temperature to prepare a clear solution. This solution was filtered through a syringe filter of diameter 0.45 μm to remove the unwanted bigger particles from the solution. After filtration, the precursor solution was used for thin-film dielectric fabrication.

5.2.4 Graphene field-effect transistor fabrication

All bottom-gate top-contact GFETs were fabricated on heavily doped (p^+-Si) silicon substrate. Before the fabrication of these types of devices, the p^+-Si-wafers (15 mm x 15 mm) were cleaned by soap solution followed by cleaning in three different solutions, i.e. (1) water, (2) acetone and (3) isopropanol for 10 min each in an ultra-sonication bath. After the wet cleaning process, all wafers were dried by passing dry air and finally exposed by oxygen-plasma to remove unwanted organic material (hydrocarbons), which accumulates on Si-substrate. After O_2 plasma cleaning, Si-substrate becomes hydrophilic in nature. This type of cleaning is an essential step in sol-gel film fabrication because it permits high uniformity of

the thin film by making it free from pinholes and trap states. After the cleaning process, the precursor sol of ionic gate dielectric Li_5AlO_4 was spin-coated on p^+-Si substrates at 4500 rpm for 50s under the ambient atmospheric condition and subsequently kept on a preheated hot plate at 70 ^oC for two minutes to remove the solvent and make the film dry. After drying, the samples were annealed in the furnace for 30 minutes at the temperature of 350 ^oC. The same process was repeated two more times, and finally, all thin film samples were annealed at 500 ^oC for 30 minutes under the ambient atmospheric condition to obtain polycrystalline α-phase of Li_5AlO_4. Graphene layer, which works as an active channel of GFETs, was deposited on the top of the Li_5AlO_4 layer by following the standard polymer assisted graphene transfer method. In addition, graphene films were also transferred on 300 nm oxide coated doped Si wafer (p^+-Si/SiO_2). Finally, a silver electrode (Ag) with a molybdenum oxide (MoO_x) interface was deposited on both types of the substrate by thermal evaporation that has been used as a source and drain electrodes of GFET. These source and drain electrodes were fabricated by the shadow-mask process under a pressure of 7.0 x 10^{-6} mBar. Six different large channel length GFETs were fabricated with fixed channel width (W) of 9 mm but with variable channel lengths (L) ranging from 0.2 mm to 5.7 mm. Accordingly, W/L ration of these GFETs were varied from 118 to 1.57.

5.3 Results and Discussions

5.3.1 Surface Morphology of graphene film

The optical micrograph of graphene film has been shown in **figure 5.2 a),** which indicates the graphene film is homogeneous in a large area with some wrinkles over its surface. The SEM image **(figure 5.2 b))** also shows that graphene film is mostly very flat with some wrinkles formation, which occurs due to the difference in thermal expansion between

graphene films and Cu foil during the cooling stage.[213] As mentioned earlier, for the TEM investigation, graphene film was transferred from Cu foil to a lacey carbon-coated TEM grid. TEM analysis reveals that graphene film is quite uniform with few folded layers in few regions **figure 5.2 c)**.

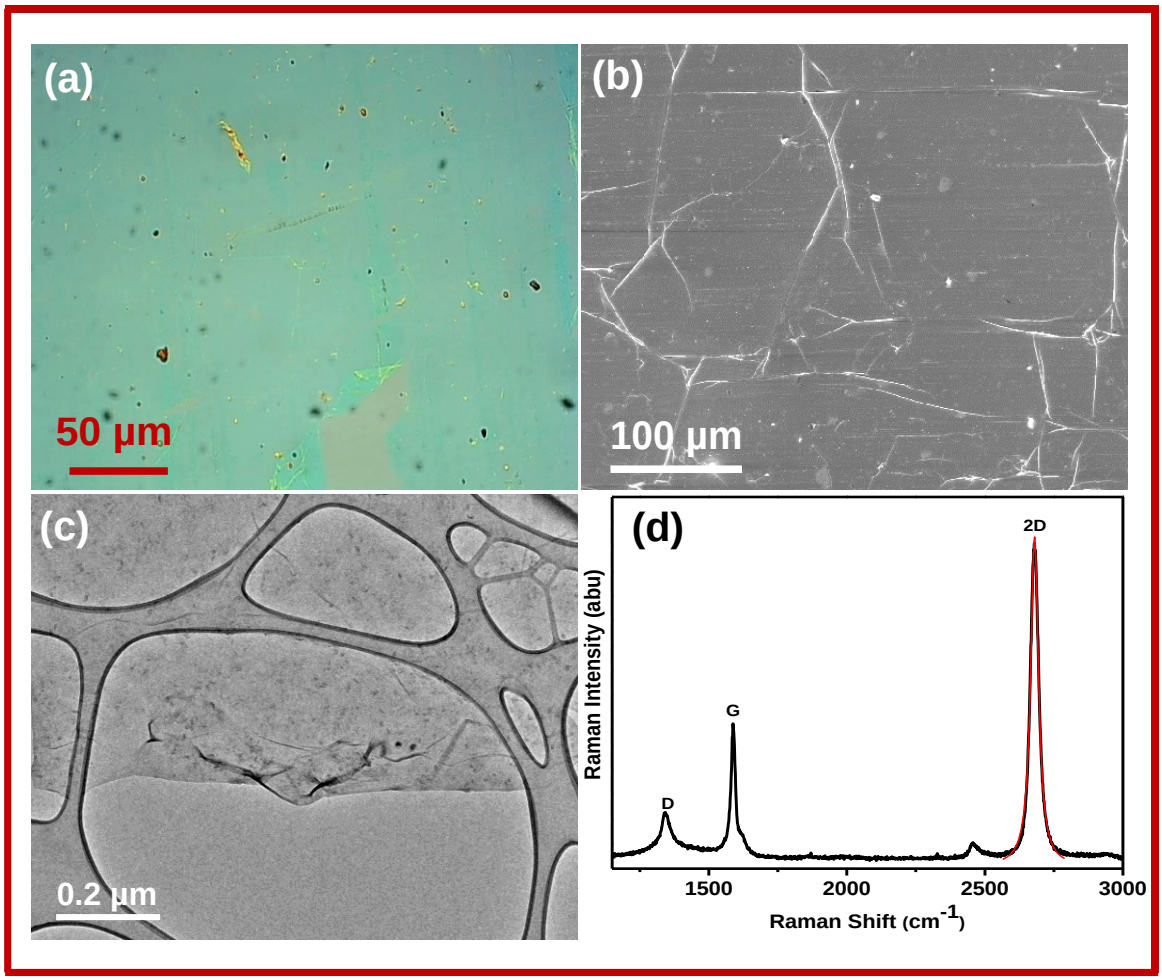

Figure 5.2: a) *Optical micrograph of graphene sheet transferred on p^+-Si/SiO_2 substrate,* ***b)*** *SEM micrograph of graphene sheet* ***c)*** *TEM image of a graphene sheet on lacey carbon-coated TEM grid where lighter region corresponds to the monolayer graphene while darker region corresponds to the folded graphene layer, and* ***d)*** *Raman spectrum of graphene.*

Raman spectrum of the graphene film on p^+-Si/SiO_2 was recorded using 532 nm laser excitation and has been shown in **figure 5.2 d)**. The most prominent peaks in the Raman spectrum have been observed around ~1340 cm^{-1} ~1588 cm^{-1} and ~2680 cm^{-1}, which correspond to the D, G, and 2D bands of graphene, respectively. The intensity ratio of D and

G peaks is found to be ~ 0.3, which suggest that the synthesized graphene is of excellent quality. Further, the 2D band is fitted well with the Lorentzian function with FWHM ~ 25±2 cm^{-1}. In addition to this, the intensity ratio of 2D and G band is found to be I_{2D}/I_G ~ 2.3, which confirms the existence of single-layer graphene in the particular region.[214, 215]

5.3.2 GFET Characterizations

The characteristics of GFETs were investigated under ambient atmospheric conditions. As mentioned earlier, single layer GFETs were fabricated with a fixed channel width, but with the variable channel length, and hence its W/L ratio varies from 118 to 1.57. During all the electrical characterizations, drain voltage (V_D), and gate voltage (V_G) both were varied within a range of 2V. **Figure 5.3** shows the output (drain current vs. drain voltage) and transfer characteristics (drain current vs. gate voltage) of six GFETs that were fabricated on p^+-Si/Li_5AlO_4 substrate. These characteristics indicate the p-channel behavior of all individual devices. However, there is a big difference in the device characteristics of different GFETs. **Figure 5.3 (a-f)** shows the output characteristics (I_D vs. V_D) with different channel lengths that point out the gradual improvement of current saturation as the channel length varied from 0.2 mm to 1.65 mm. Concerning this current saturation, the best result was observed for the channel width of 1.65 mm when the V_D swept from 0 V to -2V, and V_G varied from 0.5V to -2V. Although this current saturation, deteriorate as soon as the channel length increases. During this characterization, GFET on p^+-Si/SiO_2 substrate has also been tested. However, none of those GFETs show any gate voltage-dependent current rather than showing a metallic conduction event at very high gate voltage like -40V (**figure 5.4 a)**). This observation implies that GFETs fabrication with such a long channel length is only possible with such a kind of ionic gate dielectric.

Similarly, **figure 5.3 (g-l)** shows the transfer characteristics of the respective GFETs, which show that the on/off ratio and the Dirac point of these devices varied significantly with channel length. Out of these six characteristics, the high on/off ratio of ~3 was observed for the device with a channel length of 1.65 mm. In addition to this, transfer characteristics show that all GFETs have positive Dirac point. This positive shift of Dirac point originated from the impurity of the graphene film and dielectric/graphene interface trap state.[216] The least value of Dirac point is also seen for GFETs with 1.65 mm channel width. Effective carrier mobility (μ) of these GFETs are calculated from the following equations,[217]

$$I_D = \mu \frac{W}{L} C V_{ds} (V_G - V_{th}) \qquad \text{..... (1)}$$

Where,I_D, V_G, V_{th} are the drain voltage, gate voltage, and threshold voltage of GFET, respectively. Whereas C is the capacitance per unit area of the gate dielectric, W and L are channel width and length, respectively. The measured capacitance per unit area of Li_5AlO_4 dielectric is 350 nf cm^{-2} at 50 Hz frequency, which is used to calculate charge carrier mobility (**figure 5.4 b)**). The hole mobility for 0.2 mm channel length is 49 $cm^2 V^{-1} s^{-1}$ and increases up to 312 $cm^2 V^{-1} s^{-1}$ for 1.65 mm channel length. However, a further increase of L values decreases the carrier mobility gradually, which reaches to 30 $cm^2 V^{-1} s^{-1}$ for 5.7 mm channel length. The variation of calculated hole mobility with channel length is shown in **figure 5.5 a)**. In addition to mobility, the Dirac point also shifted with the variation of channel length. The variation of Dirac point with channel length is shown in **figure 5.5 b)**. The Dirac point becomes gradually lower with channel length varying from 0.2 mm to 1.65 mm and then shifted towards more positive voltage with channel length varying from 2.85 mm to 5.7 mm.

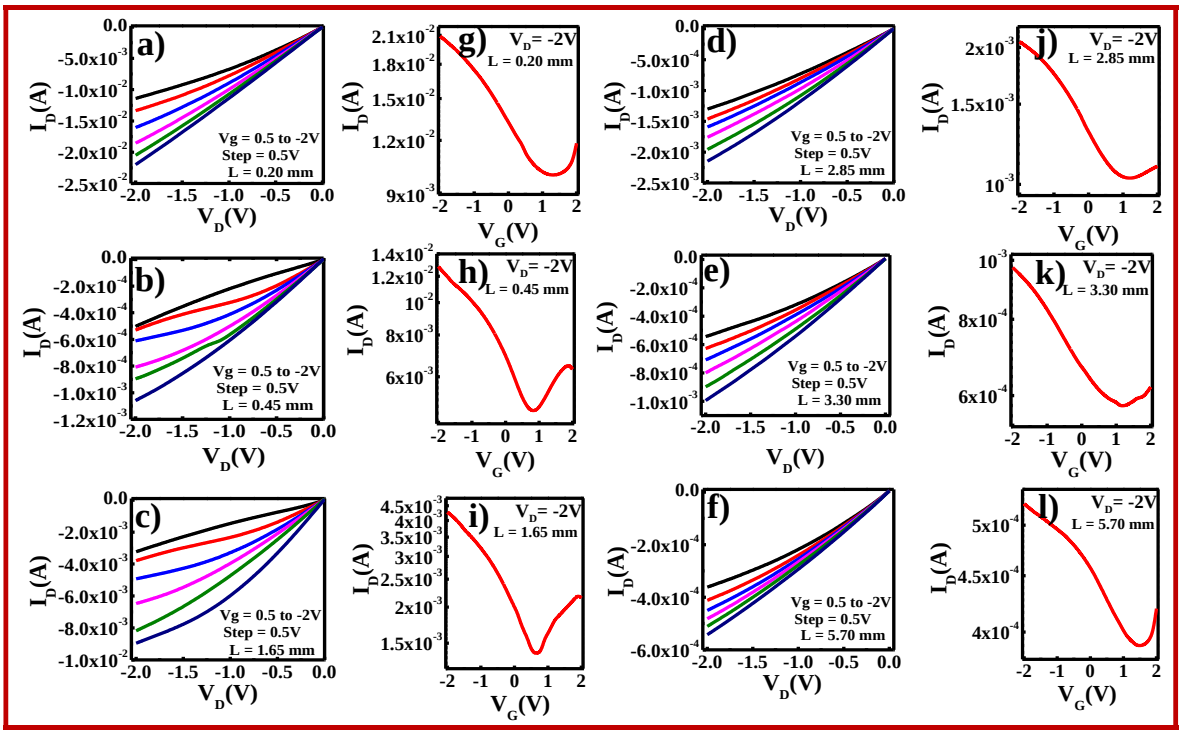

Figure 5.3: *Output characteristics of graphene transistors with different channel lengths* ***(a-f)*** *and transfer characteristics of graphene transistors of corresponding channel lengths* ***(g-l)****, respectively.*

As mentioned earlier, Li^+ doping is an effective way to open the band gap of graphene. To check the effect of Li^+ ion on the graphene sheet, we also fabricated the same device with different channel lengths on p^+-Si/SiO_2 substrates. Still, we did not get any saturation data, which is expected because large-area graphene always acts as a semimetal, which indicates the conducting nature of graphene (**figure 5.4 a)**). Therefore, these comparative studies of GFETs on p^+-Si/$Li_5AlO_4$and p^+-Si/SiO_2 substrates indicate that the Li^+ of Li_5AlO_4 dielectric plays a key role in the fabrication of larger channel length GFETs. Again, instead of having the ambipolar nature of graphene, the hole likes conduction, i.e., p-GFET characteristics are arising due to oxygen and water adsorption on the graphene surface.[216, 218] In these studies, the optimum value of carrier mobility is arising due to two combined effects. One of them is the contact resistance of the source and drain electrodes, which decrease with channel length. Therefore, the carrier mobility of GFETs is supposed to increase with channel length.

However, increasing channel length increases the scattering of carries from ripples, interfaces, and the defect states of graphene. Additionally, the carrier can be trapped in the dielectric/graphene interface. Thus charge carrier scattering and charge trapping phenomena reduce effective mobility with channel length. Therefore, the combined effects of these two phenomena limit us to reach the best performance GFETs with 1.65 mm channel length.

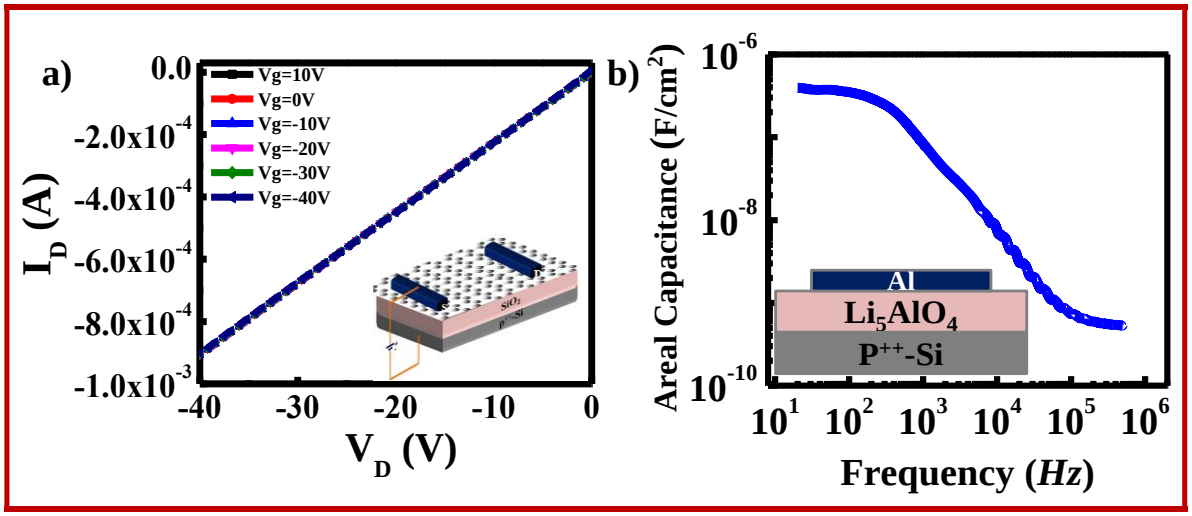

Figure 5.4: a) *Output characteristics for a Graphene field-effect transistor (GFET) using SiO_2 as a gate dielectric* ***b)*** *Capacitance vs. frequency (C-f) curve of Li_5AlO_4 dielectric thin film with a device structure of Al/Li_5AlO_4/p^+-Si.*

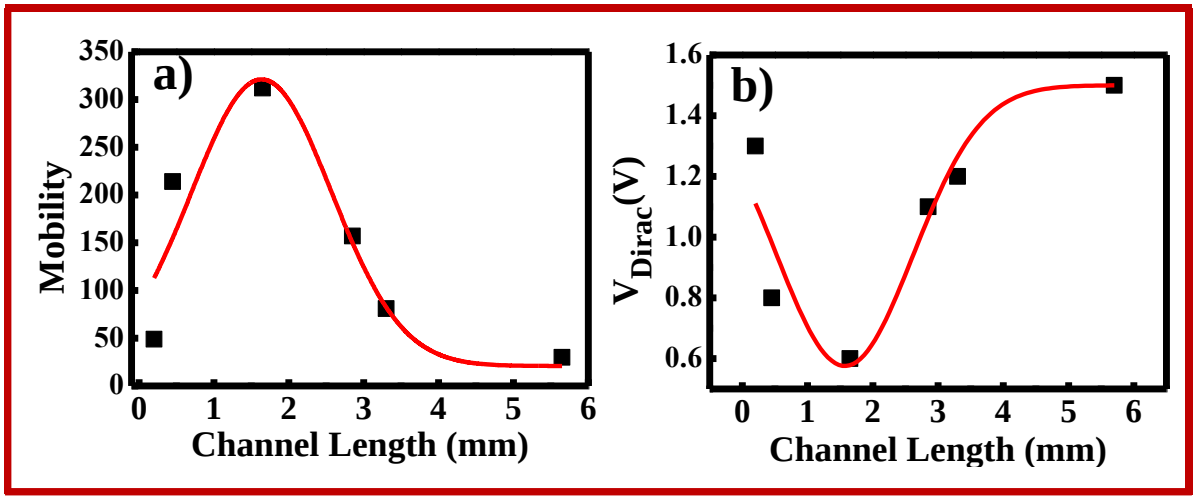

Figure 5.5: a) *Variation of mobility with channel length* ***b)*** *Variation of a shift in Dirac point with channel length.*

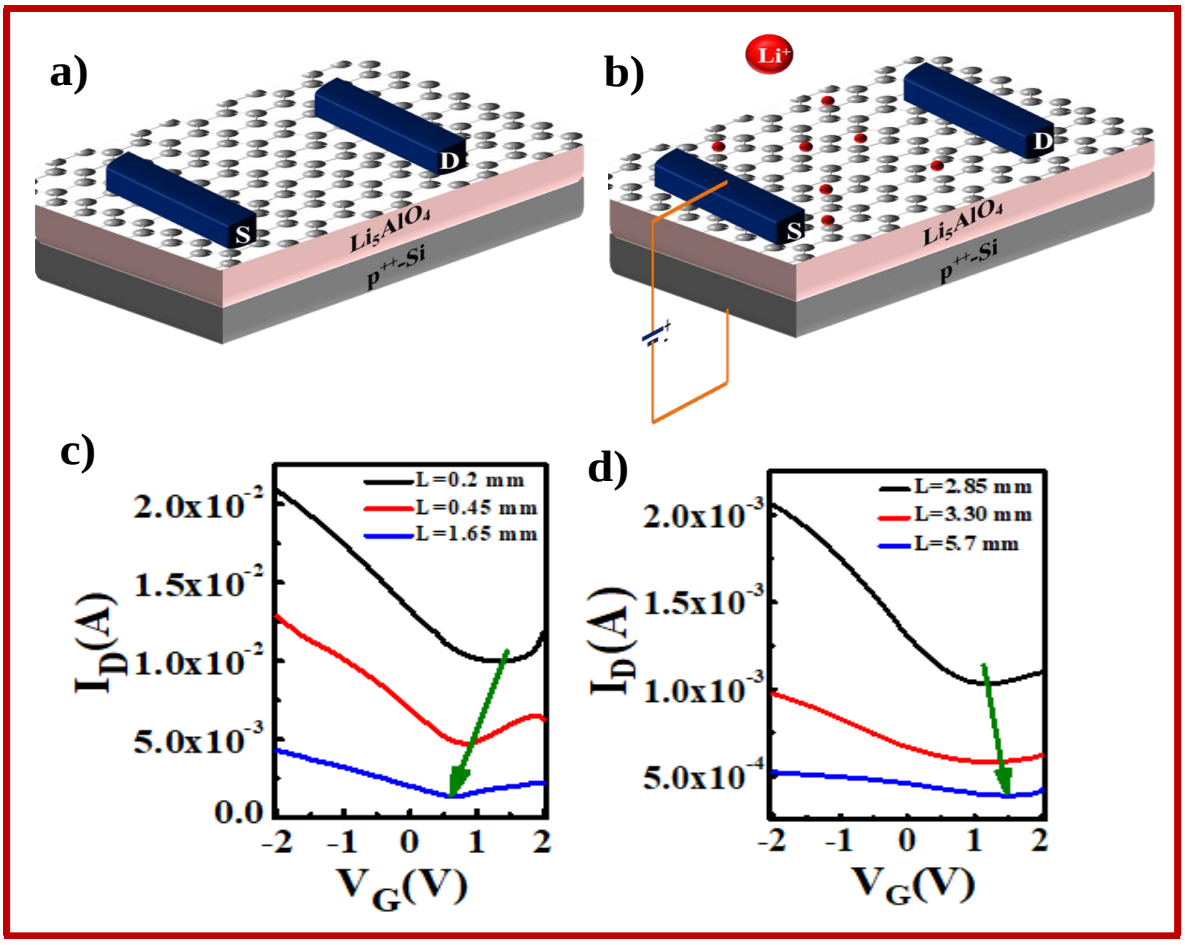

Figure 5.6: ***a)*** *Schematic illustration of the device structure of back-gated graphene transistors,* ***b)*** *Channel length-dependent* Li^+ *ion effect in graphene transistors,* ***c)*** *and* ***d)*** *Transfer characteristics of back-gated graphene transistors at* V_D *= -2V with different channel lengths, respectively.*

To realize the opening of the energy band gap in the graphene layer, which enhances the performance of GFETs device, we suggest the ion-transport (Li^+) mechanism and schematically presented in **figure 5.6 a)** and **figure 5.6 b)**. The origin of the graphene bandgap is only possible because of Li^+ ion, which traps in the graphene layer. Since the gate dielectric Li_5AlO_4 is polycrystalline in nature, and the mobile Li^+ ions are not bound in an ordered structure. The atomic radius of Li^+ ion is also very small, so it has the option to move anywhere in the crystal lattice. Therefore, after graphene deposition, some lighter Li^+ ion moves up and easily traps in the voids of graphene, which provide a room to Li^+ ion. Such

kind of intercalation of Li^+ has been reported in a large number of literature.[206],[205, 219] As we increase the channel length from 0.2 mm to 1.65 mm, Li^+ ion find a large space to trap in graphene layer and energy band gap of graphene increases simultaneously, resulting in the increase in current saturation, on/off ratio and mobility. However, further, an increase in channel length, degrade the device performance with a decrease in mobility, current saturation, and on/off ratio because of dominating charge carrier scattering and trapping phenomena. The variation of on/off ratio with channel length is shown in **figure 5.6 c)** and **figure 5.6 d)**.

5.4 Contact resistance of GFETs

Since contact resistance (R_C) of source/drain (S/D) electrode of graphene transistor plays a crucial role in the performance of the device; therefore, transfer length method (TLM) has been used to extract this parameter. According to this TLM method, total channel resistance R_{tot} of GFET is related by following equation[220],

$$\mathbf{R_{tot} = (R_S/W)L + 2R_C/W} \quad \text{.....(2)}$$

Where R_S and R_C are the sheet resistance and contact resistance, respectively. R_{tot} of each GFETs was determined from the linear part of I_D-V_D curve at $V_G = 0V$. Variation of R_{tot} with different channel lengths has been plotted in **figure 5.7 a),** which indicates that the total channel resistance of GFET gradually increases from 0.825 KΩ to 2.490 KΩ when the channel length varies from 0.2 mm to 5.7 mm. The sheet resistance (R_S) of single-layer graphene was determined by the four-probe method, which is equal to 0.292 KΩ/ sq. By using these sets of R_{tot} and R_S values, R_C values of each GFETs were extracted by equation (2), and the variation of R_C with different channel length has been plotted in **figure 5.7 b)**. As

it is observed that initially, R_C decreases from 0.162 KΩ to 0.135 KΩ when the channel length increases from 0.2 mm to 1.65 mm. However, R_C increases rapidly with a further increase in channel length. The variation of R_{tot} and R_C with different channel lengths has been summarized in **Table 5.1**. Again it can be noted that our best performance GFET was obtained with this least R_C device of 1.65 mm channel length. Therefore, it can be concluded that the performance of these GFETs strongly depends on the contact resistance of the devices.

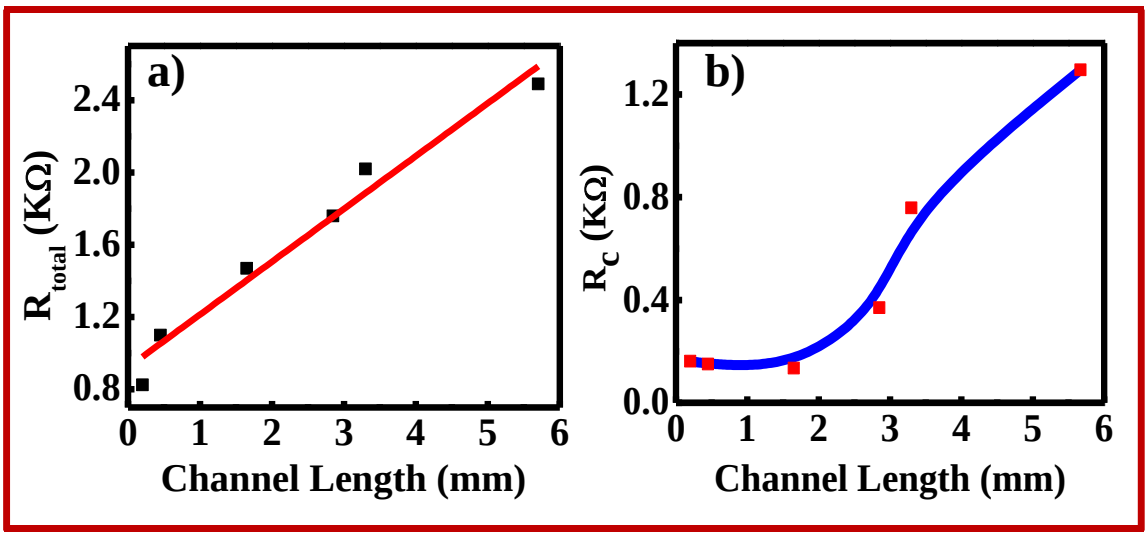

Figure 5.7: a) *Variation of total resistance with the different channel length, and* ***b)*** *Variation of contact resistance of device with different channel length.*

Table 5.1: Summary of R_{tot} and R_C of different channel length GFETs

Device no	**Channel length L (in mm)**	**W/L**	**Total Resistance (R_{tot}) in KΩ**	**Contact Resistance (R_C) in KΩ-cm**
1	0.20	118	0.825	0.162
2	0.45	20	1.142	0.151
3	1.65	5.5	1.471	0.135
4	2.85	3.15	1.760	0.371
5	3.30	2.72	2.020	0.759
6	5.70	1.57	2.490	1.296

5.5 Transconductance

The transconductance of GFET is an important parameter which characterizes the amplifying performance of devices. This transconductance of GFETs depends on source-drain voltage as well as on the dimension of the device. A number of groups reported a large transconductance of GFETs that normalized by channel width [221, 222], but a reasonable comparison is still missing because all these devices were measured at the different electric fields and source-drain bias. Unfortunately, current saturation is not usually visible in GFET as compared to conventional TFT, and transconductance increases with increasing source-drain bias. Here, we have proposed long channel length-dependent normalized Transconductance at a fixed channel width, to benchmark amplifying behavior of GFET. The intrinsic transconductance of long channel GFET working in the linear region can be calculated by the following equation

$$g_m = \mu C \frac{W}{L} V_{ds} \ldots\ldots\ldots (3)$$

Where μ is carrier mobility, C is the capacitance of dielectric, V_{ds} is drain-source voltage, W is channel width, and L is channel length. If we normalize it by dimension and bias of the device, then the transconductance is related to the gate capacitance and carrier mobility as follows,

$$g_N = g_m \frac{L}{WV_{ds}} = \mu C \ldots\ldots\ldots (4)$$

Where g_N is normalized transconductance.

It ought to be noticed that C is the total capacitance of two capacitors, which is connected in series. One of them is an oxide capacitor of the gate (Li_5AlO_4), and the other one is a quantum capacitor of the graphene channel. Since quantum capacitance is much larger than the oxide capacitance, therefore for simplicity, we replaced total capacitance C by oxide capacitance C_{ox}. [221, 223] The transconductance is directly derived from transfer characteristics, as shown in **figure 5.8 a)** and **b)**, respectively. Although our device mobility is not that high as previously reported, which is mainly due to long channel length FET, the transconductance value is quite high. The maximum normalized transconductance of the device is 5.32 mS with 1.65 mm channel length at a bias of -2V, which indicates the high efficiency of the gate oxide and graphene channel. As we increase the channel length from 0.2 mm to 1.65 mm, the value of transconductance gradually increases, which is expected. Afterward, transconductance decreases with increasing channel length up to 1.01 mS with a channel length of 5.7 mm. Further, various device parameters of GFETs fabricated with different channel lengths have been summarized in **Table 5.2**.

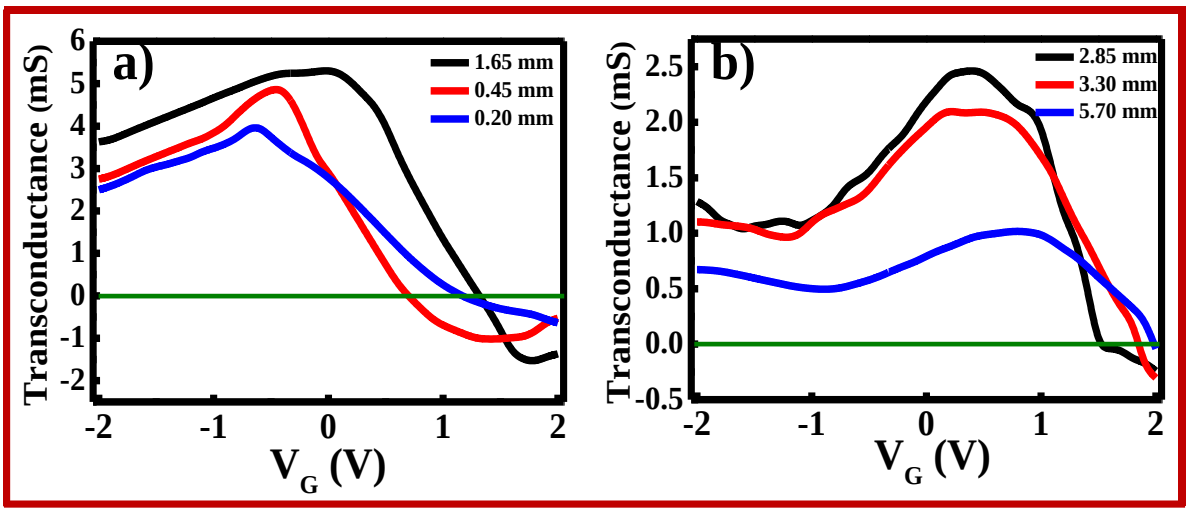

Figure 5.8: a) *Transconductance of the devices with channel length varies from 0.2 mm to 1.65 mm and* ***b)*** *channel length varying from 2.85 mm to 5.7mm as a function of back-gate voltage under a bias of -2V.*

Table 5.2: Summary of the various parameters of GFETs device.

Device no.	Channel length (L in mm)	W/L	Dirac Point Voltage (V)	I_{on}/I_{off}	Hole Mobility (μ) ($cm^2 V^{-1} sec^{-1}$)	Normalized Transconductance (mS)
1	0.20	118	1.3	2.1	49	3.99
2	0.45	20	0.8	2.8	214	4.89
3	1.65	5.5	0.6	3	312	5.32
4	2.85	3.15	1.1	2	157	2.47
5	3.30	2.72	1.2	1.7	81	2.08
6	5.70	1.57	1.5	1.4	30	1.01

5.6 Conclusion

In conclusion, this chapter has demonstrated a new fabrication method of low operating voltage large channel length graphene FET with current saturation using ion-conducting oxide gate dielectric (Li_5AlO_4). These GFETs required only 2V to operate with high performance. A systematic study with variable channel length revealed that high on/off ratio and mobility is achieved with a channel length of 1.65 mm. The Dirac point voltage of the GFETs is also minimized up to 0.6V with a channel length of 1.65 mm. Interestingly, similar channel length GFETs with conventional p^+-Si/SiO_2 shows only the metallic behavior without any gate voltage dependence variation of current. This observation indicates that the Li^+ ion of Li_5AlO_4 ionic gate dielectric plays an important role and switches the metallic nature of graphene to the semiconducting nature, which was predicted earlier by theoretical studies. Further, we have also demonstrated channel length-dependent normalized transconductance of GFETs, and the high transconductance value of 5.32 mS has been

achieved with 1.65 mm channel length. Combining with the growth of large-area CVD graphene, this simple sol-gel based ionic gate dielectric could open up a thrilling opportunity for long channel length fabrication of high-performance graphene transistor.