Chapter 4

4.1 Introduction

Complementary metal-oxide-semiconductor (CMOS) technology is used prevalently for constructing different integrated circuits in microprocessors, microcontrollers, static RAM, image sensors, data converters, and highly integrated transceivers in various types of communications.[148, 149] Two important characteristics of CMOS devices are high noise immunity and low static power consumption that makes CMOS as unbeatable technology for modern electronics. This CMOS circuit required complementary and symmetrical pairs of p- and n-channel thin-film transistors (TFTs) for logic functions.[150-152] However, if the deposition conditions of the p- and n- channel TFTs are not compatible, then it is quite difficult to fabricate a highly dense CMOS circuit in a single substrate.[151, 153] In such a scenario, ambipolar TFT can play an important role that shows both electron and hole conduction in a single TFT, based on the gate bias.[153, 154] Besides this ambipolar CMOS inverter fabrication, ambipolar charge transport of TFT is widely used for the fabrication of light-emitting transistor,[155, 156] flash memory[157-159] and artificial synaptic emulation.[160] So far, several reports have been shown that individual single-nanostructured based transistors can show good ambipolar behavior [161-163], but these transistors fail to give a solution for large areas and scalable fabrication. In this contest, thin film-based ambipolar transistors can play a better role and have the capacity for mass production. To date, most of the reported thin film ambipolar transistor has been fabricated by using organic small molecule and polymer semiconductor.[164-166] However, the main difficulties of these organic/polymer-based TFTs are its low carrier mobility and poor

atmospheric stability for electron transport.[153, 158, 166] Relatively, lower-cost metal oxide semiconductors show much high environmental stability with higher carrier mobility. Although, it's really hard to find an oxide semiconductor with good hole mobility, which limits the progress of oxide ambipolar TFT fabrication. So far, SnO_x is the only reported oxide semiconductor that is capable of fabricating ambipolar TFT.[167] Although, in most of these cases, it requires a complex device architecture with a control deposition technique. Therefore, for low-cost portable electronics, it's urgent to develop high-performance oxide ambipolar TFT by solution-processed technique with low operating voltage. Those low cost and low voltage ambipolar oxide TFT will be capable of fabricating cost-effective, stable, and energy-efficient CMOS inverter for portable electronics.

Lowering the operating voltage of a TFT is a crucial issue for developing low operating voltage CMOS inverter, which is required for portable optoelectronics devices. Till now many efforts have been given to developing low voltage TFT by using different high-κ oxide dielectric including Ta_2O_5[115], Y_2O_3[116], TiO_2[117, 118], ZrO_2[119, 120], HfO_x[121], $HfLaO_x$[122], $LaAlO_3$[123]. In addition to oxide dielectric, polymer ion-gel, and self-assembled monolayer (SAM) have been successfully utilized for low operating voltage organic TFT. However, such kind of ion-gel or SAM dielectric is not compatible with a higher temperature fabrication process, like solution-processed oxide semiconductor. In this situation, ion-conducting oxide dielectric shows the best performance for low operating voltage transparent TFT fabrication.[29, 99, 130, 168-171] Therefore, for high performance cum low operating voltage ambipolar TFT fabrication, oxide semiconductor with ionic oxide dielectric is one of the best combination. In addition to that, such kind of ambipolar TFT can be environmentally stable due to its intrinsic oxide nature.

Tin oxide is commonly found as an n-type semiconductor. Although, the hole carrier can be introduced to the valance band of SnO_2 mainly in two different ways. One of them is to create Sn vacancies, which can introduce hole carriers to the valance band of SnO_2, commonly achieved by sputtering method deposition.[172-174] The other way is by chemical doping with group IIIA elements like indium (In), gallium (Ga), which can occupy an Sn site in SnO_2 lattice.[175-178] Based on those earlier reports, SnO_2 TFTs have been fabricated by choosing two ion-conducting oxide dielectrics that can introduce p-doping to the dielectric/semiconductor interface to enhanced hole conduction of SnO_2. One of them is $LiInO_2$, and the other one is $LiGaO_2$, which can dope In and Ga respectively to an interfacial channel of SnO_2. To identify the differences, Li_2ZnO_2 has been chosen as a third ionic dielectric that contains divalent Zn atom, also has no role in introducing hole conduction in SnO_2. Comparative electrical characterization shows a clear n-channel behavior of all these TFTs. Moreover, all those devices work within the 2V operating voltage range, which is due to the common features of the ion-conducting gate dielectric.[29, 130] However, TFT with $LiInO_2$ and $LiGaO_2$ dielectric show ambipolar behavior, whereas a device with Li_2ZnO_2 dielectric shows unipolar n-channel behavior. Most interestingly, the device with $LiInO_2$ dielectric shows balance carrier transport with high electron and hole mobility within 1V operating voltage, which has been used to fabricate low voltage CMOS inverter.

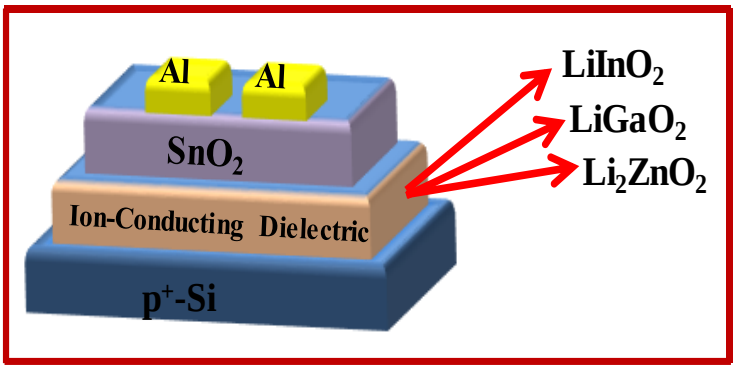

Figure 4.1: *Schematic view of the device structure.*

4.2 Result and discussion

4.2.1 Thermal Analysis

The thermal behavior $LiInO_2$ was analyzed by thermogravimetric analysis (TGA) and differential thermal analysis (DTA) study. For this experiment, the precursor powder sample was prepared by evaporating the solvent of a mixed solution of lithium acetate and indium chloride. These studies have been performed in a nitrogen (N_2) atmosphere at a flow rate of 20 ^oC /minute. **Figure 4.2 a)** shows the TGA result in combination with DTA in which weight loss ensues in two steps. The first weight loss started from room temperature to 120 ^oC, corresponding to the residual water, trapped solvent, and moisture, which are well supported by DTA peak. This weight loss is ~8 % of the total amount. The second weight loss started from 470 ^oC and ended with 550 ^oC, and the sharp, intense DTA exothermic peak is observed in this temperature range, which indicates the crystallization of sol-gel $LiInO_2$ powder. There is a negligible weight loss between the temperatures range of 550 ^oC to 800 ^oC. This nature of DTA suggests the crystallization process of $LiInO_2$ is occurring ~550 ^oC at the highest rate. The thermal behavior of $LiGaO_2$ is shown in **figure 4.2 b)**, which indicated the crystallization of this dielectrics is 550 ^0C, and the crystallization temperature of dielectric Li_2ZnO_2 is also 500 ^oC which has been reported in our earlier paper.[99]

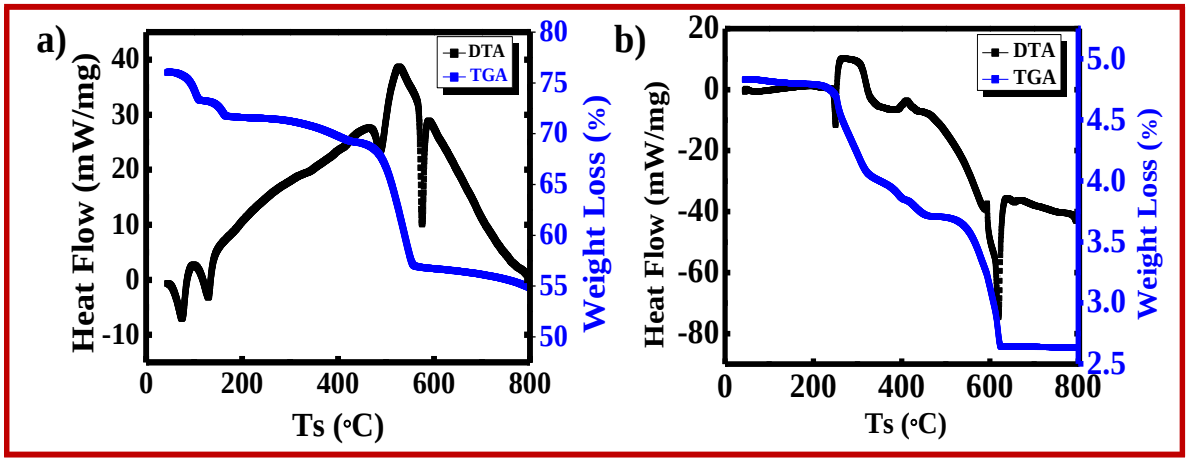

Figure 4.2: *Thermal gravimetric analysis (TGA) and differential thermo-gravimetric analysis (DTA) curves of precursor powder* ***a)*** *$LiInO_2$ and* ***b)*** *$LiGaO_2$.*

4.2.2 Structural Properties

Grazing Incidence X-ray Diffraction (GIXRD) measurement was used to check the structural property of $LiInO_2$ thin film. For this measurement, the thin-film sample was prepared on a glass substrate and annealed at 550 ^oC for 1 hr. **Figure 4.3 a)** shows the GIXRD data of $LiInO_2$ thin film annealed at 550 ^oC. The diffraction peaks that originated from reflection planes of (103), (211), and (204) at peak 2θ angles near about 35.51, 48.14 and 58.18 respectively, recognized the tetragonal crystal phase of $LiInO_2$ which has been verified by JCPDS data (No. 76-0427). These sharp diffraction peaks suggest that 550 ^oC annealing temperature is enough to achieve the crystalline phase of $LiInO_2$ dielectric thin film. The GIXRD data for $LiGaO_2$ and Li_2ZnO_2 thin films are shown in **figure 4.3 b) and c)**, respectively. **Figure 4.3 b)** shows that the $LiGaO_2$ is crystalline in nature and preferred crystalline orientation from reflection planes of (002) and (040) at peak 2θ angles near about 35.8 and 57.8, respectively.[179] Similarly, from **figure 4.3 c)**, clear reflection from (120) and (112) planes are observed for Li_2ZnO_2 that has been reported in our earlier work. [99]

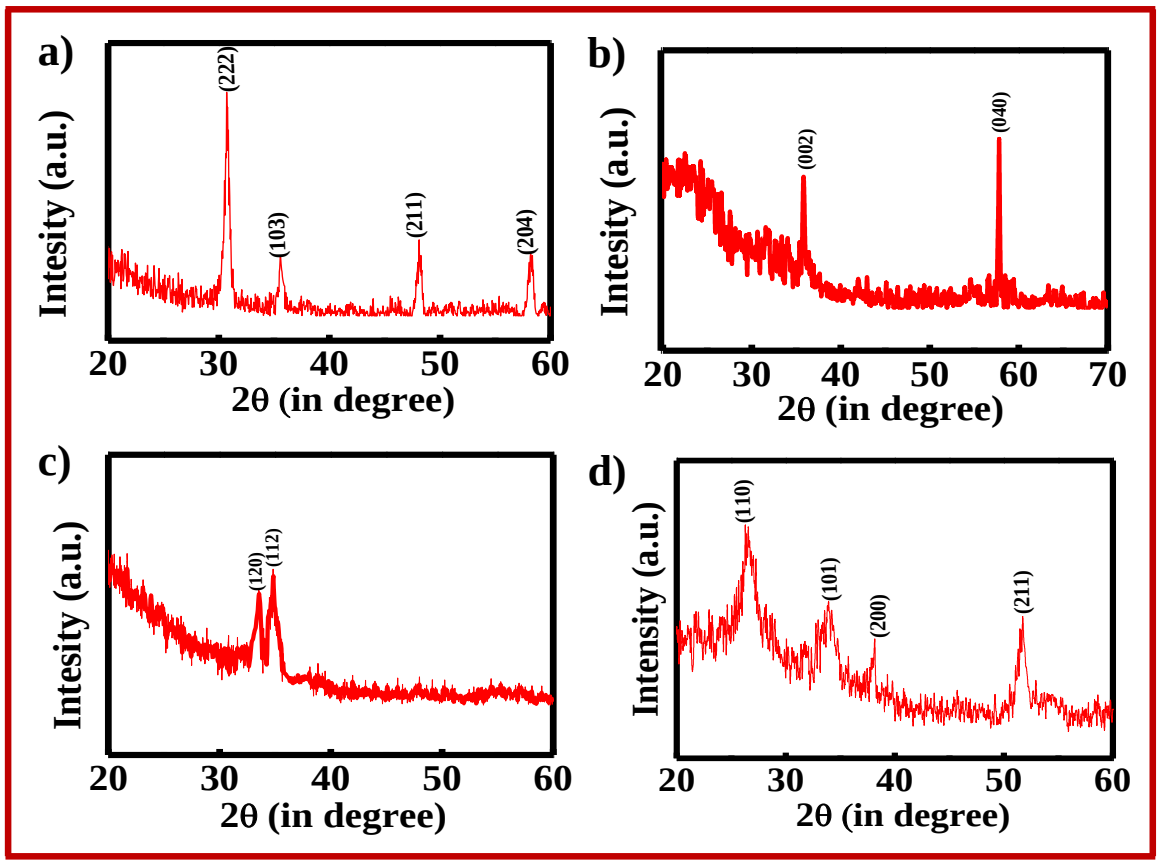

Figure 4.3: *GIXRD analysis of* ***a)*** *$LiInO_2$ and* ***b)*** *$LiGaO_2$ thin film at 550 °C annealing temperature and GIXRD analysis of* ***c)*** *Li_2ZnO_2 and* ***d)*** *SnO_2 thin film at 500 °C annealing temperatures, respectively.*

Figure 4.3 d) represents Grazing Incidence X-ray Diffraction (GIXRD) analysis of SnO_2 thin film prepared on a glass substrate annealed at 500 °C for 30 minutes. The diffraction peak of SnO_2 was assigned as 26.56^0, 33.92^0, $38.08^{0,}$ and 51.72^0 originated from reflection planes (110), (101), (200), and (211), respectively, suggest the tetragonal phase of SnO_2.[180]

4.2.3 Surface Morphology

For TFT, the dielectric/semiconductor interface plays a crucial role in device performance. Therefore, atomic force microscopy (AFM) was used to study the surface morphology of dielectric thin film (p^+-Si/ $LiInO_2$) annealed at 550 °C as shown in **figure 4.4 a)**. From AFM exploration, the root means square (rms) value of $LiInO_2$ thin film is extracted approximately

5 nm, which is acceptable for solution-processed TFT. The 3-D image of $LiInO_2$ thin-film AFM **figure 4.4 b),** also suggests that the film is dense and void-free. Similarly, AFM studies of $LiGaO_2$ and Li_2ZnO_2 thin films have been performed, which are shown in **figure 4.4 c)** and **figure 4.4 e)**, respectively. These two pictures indicated the rms roughness for these two films are ~3 and 6 nm, respectively.

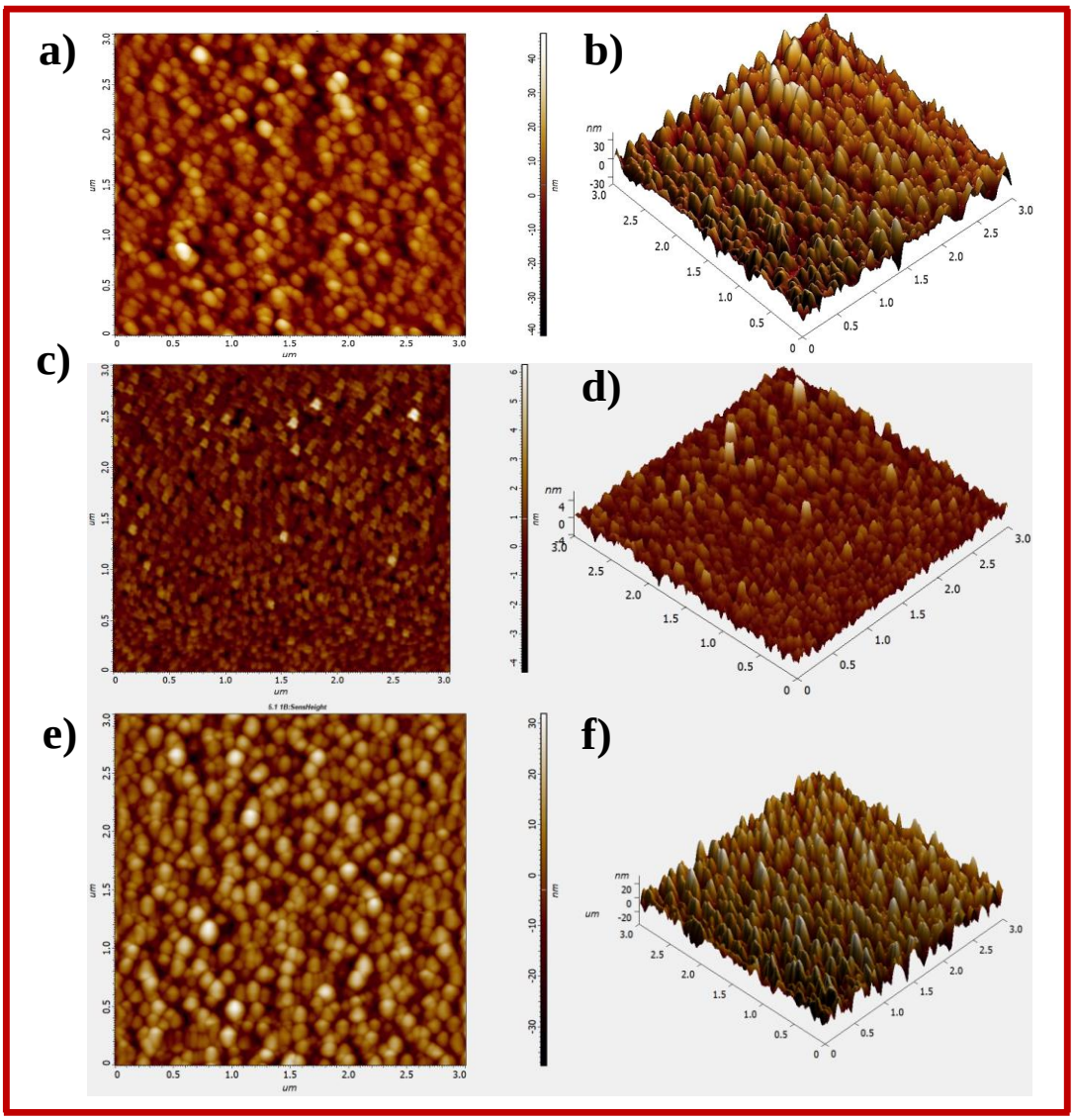

Figure 4.4: *Surface morphologies (scan surface area 3 x 3 µm) of the solution-processed $LiInO_2$ dielectric thin films for $LiInO_2/p^+$-Si surface* ***a)*** *2-D topography* ***b)*** *3-D topography, for $LiGaO_2/p^+$-Si surface* ***c)*** *2-D topography* ***d)*** *3-D topography, and for Li_2ZnO_2/p^+-Si surface* ***e)*** *2-D topography* ***f)*** *3-D topography, respectively.*

4.2.4 Optical Properties of $LilnO_2$ and $LiGaO_2$ Thin Films

The optical transmittance spectra of sol-gel derived $LiInO_2$ thin film was recorded in the wavelength range 300–900 nm. **Figure 4.5 a)** showed the spectral transmittance spectra of $LiInO_2$ film coated on a quartz substrate that was annealed at 550 ^oC for one hour. It was noticed that the dielectric sample has low transmittance in the ultra-violet region (300–400 nm) but high average transmittance($\approx$ 84%) in the visible region (400–850 nm). Higher transmittance in the visible region specifies the dielectric film is very smooth with low defect density and voids, which is very beneficial for the fabrication of high-performance TFT with low leakage current. For that reason, $LiInO_2$ thin film can be a suitable candidate to use as a gate dielectric for high-performance TFT. The optical band gap energy of the $LiInO_2$ thin film sample was calculated by extrapolating linear region of the plot $(\alpha h\upsilon)^2$ vs. $h\upsilon$ **(figure 4.5 b)**, where $h\upsilon$ is the incident photon's energy and α is the optical absorption coefficient. The extracted value of the energy band gap of $LiInO_2$ is 3.6 eV, which is the same as previously reported.[181] The optical transmittance spectra and Tauc's plot of $LiGaO_2$ thin films are given in **figure 4.5 c)**, which looks very similar to nature with $LiInO_2$. However, the extracted band gap of $LiGaO_2$ is 5.5 eV **figure 4.5 d)**, which is much higher than $LiInO_2$ thin film. The optical band gap of Li_2ZnO_2 is much lower (3.3 eV), which has been reported in our earlier work.[99]

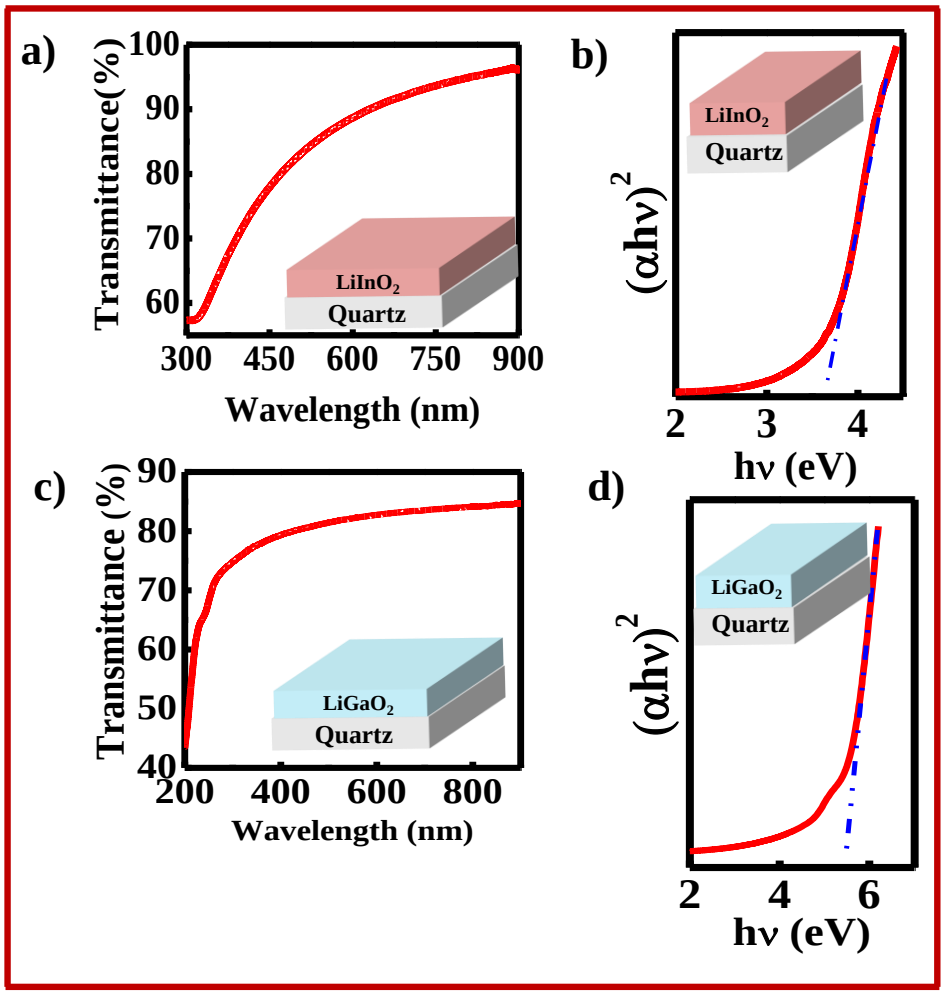

Figure 4.5: *Optical transmittance spectra of the solution-processed dielectric thin film annealed at 550 °C* ***a)*** *$LiInO_2$/quartz (inset) and* ***c)*** *$LiGaO_2$/quartz (inset), The Tauc's plot corresponding to dielectric thin film* ***b)*** *$LiInO_2$ and* ***d)*** *$LiGaO_2$, respectively.*

4.2.5 Dielectric and Electrical characterizations

To understand the electrical properties of the deposited dielectric thin films, current-voltage (I - V) measurements have been carried out using a metal-insulator-metal device architecture (p+-Si/dielectric/Al). The leakage current density of 550 °C annealed $LiInO_2$ dielectric thin film at 2 V is only 2.4 x 10^{-8} A/$cm^{2,}$ which is very low as compared to other previously reported dielectrics **figure 4.6 a)**.[99, 168] This low leakage current density is the signature of the highly-dense dielectric thin film with very less defect density. Apart from this, the breakdown voltage of the device is ~ 16 V, which is around sixteen-time higher than the

normal operating voltage of the device (≤ 1 V). Thus, the above observations are fruitful evidence to use $LiInO_2$ as a gate dielectric for ambipolar TFTs.

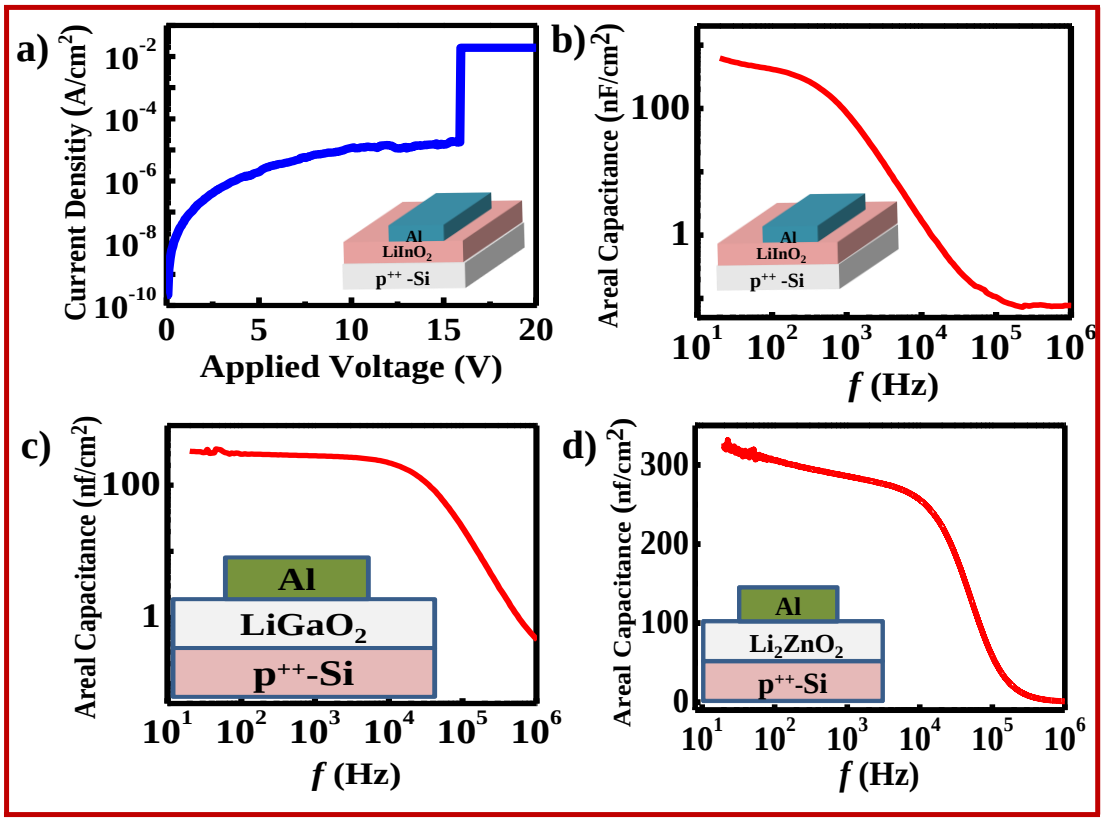

Figure 4.6: a) *Leakage current density vs. applied voltage of $LiInO_2$ thin film annealed at 550 °C with p^+-Si/$LiInO_2$/Al device structure and capacitance vs. frequency curves of solution-processed ionic dielectric* ***b)*** *$LiInO_2$* ***c)*** *$LiGaO_2$ and* ***d)*** *Li_2ZnO_2, respectively.*

The dielectric behavior of $LiInO_2$ was examined in detail with the same device structure (p^+-Si/$LiInO_2$/Al) by measuring frequency-dependent capacitance (C - *f*) within the range of 20 Hz to 1 MHz as shown in **figure 4.6 b)**. The capacitance of the $LiInO_2$ film decreases with frequency, particularly above 10^3 Hz because of its strong depends on ionic polarization due to the movement of Li^+, which is a relatively slow process. The measured capacitance per unit area of fabricated $LiInO_2$ thin film is 478 nF/cm^{2,} which is significantly higher than the thermally grown SiO_2 with similar thickness. This higher capacitance per unit area value of $LiInO_2$ thin film indicates its suitability as a gate dielectric for low operating voltage TFT

fabrication. Similarly, frequency-dependent capacitance characterization has been performed for $LiGaO_2$ and Li_2ZnO_2 thin films; those are shown in **figure 4.6 c)** and **figure 4.6 d)**, respectively. The measured capacitance per unit area for $LiGaO_2$ and Li_2ZnO_2 thin films are 350 $nF/cm^{2,}$ and 312 $nF/cm^{2,}$ respectively.

4.3 Device Fabrication

Three different types of SnO_2 TFTs have been fabricated by using $LiInO_2$, $LiGaO_2$, and Li_2ZnO_2 dielectric thin film, respectively, with a bottom-gate top-electrode geometry which we called as TFT1, TFT2, and TFT3 respectively. All these devices have been fabricated on top of heavily doped p-type Si (p^+-Si) substrates of dimension 15 mm x 15 mm (**figure 4.7 a)**). In the beginning, all these substrates were passes through routine cleaning in four different solutions, as previously reported.[168] After routine cleaning, all the substrates were dried by passing dry air and immediately exposed to oxygen plasma for 5 min to remove unwanted organic residue (hydrocarbons) from the Si substrate and make the substrate hydrophilic. Such a hydrophilic surface offers smooth and pinhole-free thin film formation during spin coating, which supports diminishing the trap state on the dielectric surface. Before spin coating, all precursor solutions were filtered through a syringe filter (PVDF-0.45µm) due to which film quality was improved. Afterward, the solution of the dielectric precursor of $LiInO_2$ was spin-coated at 4000 rpm for 50 seconds on the top of Si substrates under ambient atmospheric conditions. To remove the precursor solvent, the spin-coated film was kept on a hot plate at 80 ^oC for two minutes, followed by the annealing process (350 ^oC) in a muffle furnace for half an hour. This process was repeated two more times. Finally, the dielectric thin film coated on Si substrate was annealed at 550 ^oC in a furnace for one hour to obtain the polycrystalline phase of $LiInO_2$ under ambient atmospheric

condition. Similarly, for TFT2 and TFT3, $LiGaO_2$ and Li_2ZnO_2 thin films are deposited in a similar process by three successive coatings followed by annealing process at 550 ^oC and 500 ^oC for one hour and half an hour, respectively. Solution-processed tin oxide (SnO_2) that was used as a metal oxide semiconductor of TFTs was coated on top of the ionic gate dielectric. In this deposition process, a 300 mM precursor solution of SnO_2 was spin-coated onto three different ion-conducting dielectric films for three different types of TFTs fabrication, which were kept on a preheated hot plate at 120 ^oC for 2 minutes to remove the solvent. After that, dried thin films were transferred to a preheated furnace at 500 ^oC for a period of 30 minutes to obtain a polycrystalline film of SnO_2 on the dielectric surface.

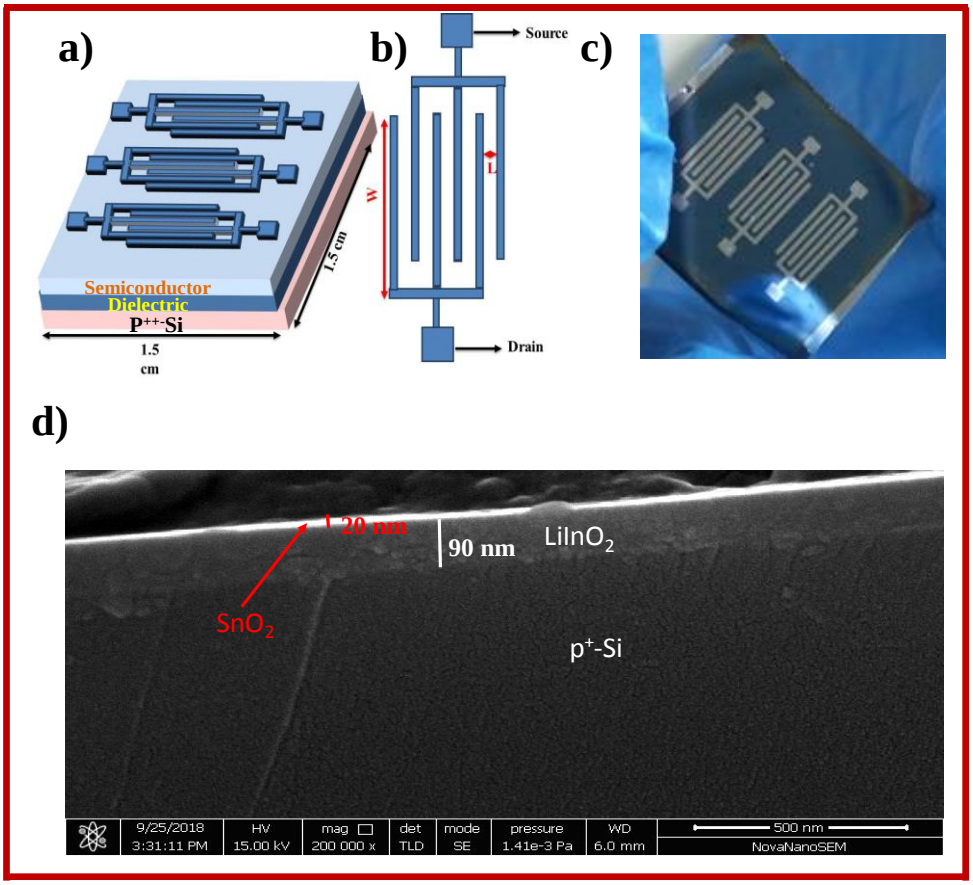

Figure 4.7: a) *Schematic view of the device structure,* ***b)*** *interdigitated mask with width (W) to channel length (L) ratio of 118 (23 mm/0.2 mm),* ***c)*** *photograph of actual devices with three TFT fabricated on 15 mm x 15 mm substrate and* ***d)*** *cross-sectional SEM image of TFT with $LiInO_2$ gate dielectric, respectively.*

In this annealing process, some In or Ga ion has been thermally diffused from the dielectric layer to the interfacial SnO_2 semiconductor, which introduced shallow acceptor levels to the conducting channel of TFT. As a result, hole conduction arises in the TFT characteristics. Finally, aluminum metal has been deposited on the top of SnO_2 thin film by shadow mask process in a thermal evaporator that works as a source and drain electrodes of the devices. The width to length ratio of all TFTs was 118 (W/L=23.6 mm/0.2 mm, **figure 4.7 b)**). The photograph of the actual image is shown in **figure 4.7 c)**. A cross-sectional scanning electron microscopic (SEM) study has been performed to check the thickness of the gate dielectric and the semiconductor. **Figure 4.7 d)** shows the cross-sectional SEM image of TFT1 that indicates the thickness of $LiInO_2$ and SnO_2 are 90 nm and 20 nm, respectively.

4.4 Transistor Charectrization

To identify the device performance of three ion-conducting oxides ($LiInO_2$, $LiGaO_2$, and Li_2ZnO_2) as a gate dielectric, three different TFTs were fabricated on highly doped Si (p^+-Si) substrate, by using polycrystalline SnO_2 as a channel semiconductor **(figure 4.1)**. As mentioned earlier, we named these three TFTs with $LiInO_2$, $LiGaO_2$, and Li_2ZnO_2 dielectrics as TFT1, TFT2, and TFT3, respectively. **Figure 4.8** shows the output and transfer characteristics of all three TFTs under low voltage operation. The applied gate voltage (V_G) was swept from -0.5V to 2V for n-channel operation with drain voltage (V_D) variation from 0V to 1V. On the other hand, for p-channel operation, V_G was varied from 0.5V to -2V with a variation of V_D from 0V to -1V. **Figure 4.8 a)** and **figure 4.9 a)** show the output characteristics of TFT1 under n-channel and p-channel operation, respectively, which shows drain current (I_D) saturate under < 1V operation, which is advantageous for low power electronics. Additionally, these data indicate that the nature of drain current amplification

under n- and p-channel operation is very much similar to the same threshold voltage that results in almost the same saturation drain current at $|V_G| = 2V$ for both types of operation which is the signature of the balanced ambipolar transistor. **Figure 4.8 d)** and **figure 4.9 c)** shows the transfer characteristics for n- and p- channel operation of TFT1 and the drain current increases with either positive (for n-channel) or negative gate bias (for p-channel) under $|V_D| = 1V$ which implies that this transistor "turns on" under both types of gate bias. Similar characterizations have been done for TFT2 and TFT3. **Figure 4.8 b)** and **figure 4.9 b)** show the output characteristics of TFT2 for n-channel and p-channel transport, respectively. Similarly, **figure 4.8 e)** and **figure 4.9 d)** show the transfer characteristics for n-channel and p-channel transport, respectively. These data indicated that TFT2 shows dominating n-channel transport and weak p-channel transport. On the other hand, TFT3 shows pure n-channel transport, which has been identified from their output and transfer characteristics that are shown in **figure 4.8 c)** and **figure 4.8 f)**, respectively. Instead of having their different charge transport nature, output characteristics of all these TFTs show good current saturation below 2V operating voltage, indicates common noble features of the ion-conducting oxide gate dielectric. It is observed that the drain current (I_D) of all three devices are over two orders of magnitudes higher than the gate leakage current (I_G), which implies that the channel current of those devices is not interfered by gate leakage current. The transfer characteristics with gate leakage current (I_D/I_G vs. V_G) under n-channel operation have been given in **figure 4.8**. The gate leakage current of three different dielectric $LiInO_2$, $LiGaO_2$, and Li_2ZnO_2 can be seen in **figure 4.8 g)**, **figure 4.8 h),** and **figure 4.8 i)**, respectively.

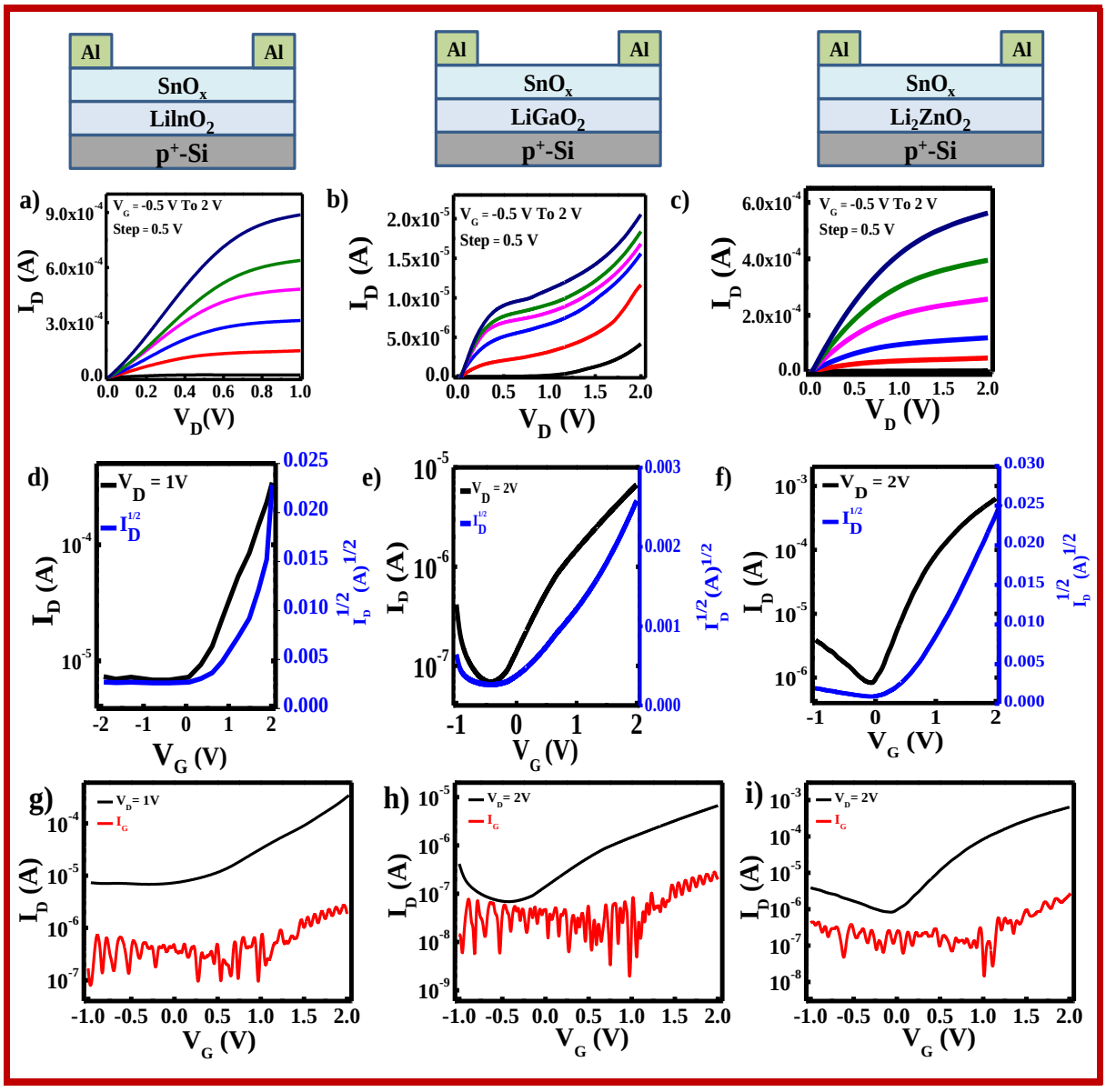

Figure 4.8: a) *Output and* ***d)*** *transfer characteristics of the SnO_2 TFT with $LiInO_2$ dielectric annealed at 550 °C,* ***b)*** *Output and* ***e)*** *transfer characteristics of the SnO_2 TFT with $LiGaO_2$ dielectric annealed at 550 °C and* ***c)*** *Output and* ***f)*** *transfer characteristics of the SnO_2 TFT with Li_2ZnO_2 dielectric annealed at 500 °C with device architecture Al/SnO_2/$LiInO_2$/p^+-Si, Al/SnO_2/$LiGaO_2$/p^+-Si and Al/SnO_2/ Li_2ZnO_2/p^+-Si respectively, under n-channel operation and transfer characteristics with gate leakage current (I_D/I_G vs. V_G) under n-channel operation* ***g)*** *$LiInO_2$,* ***h)*** *$LiGaO_2$ and* ***i)*** *Li_2ZnO_2, respectively.*

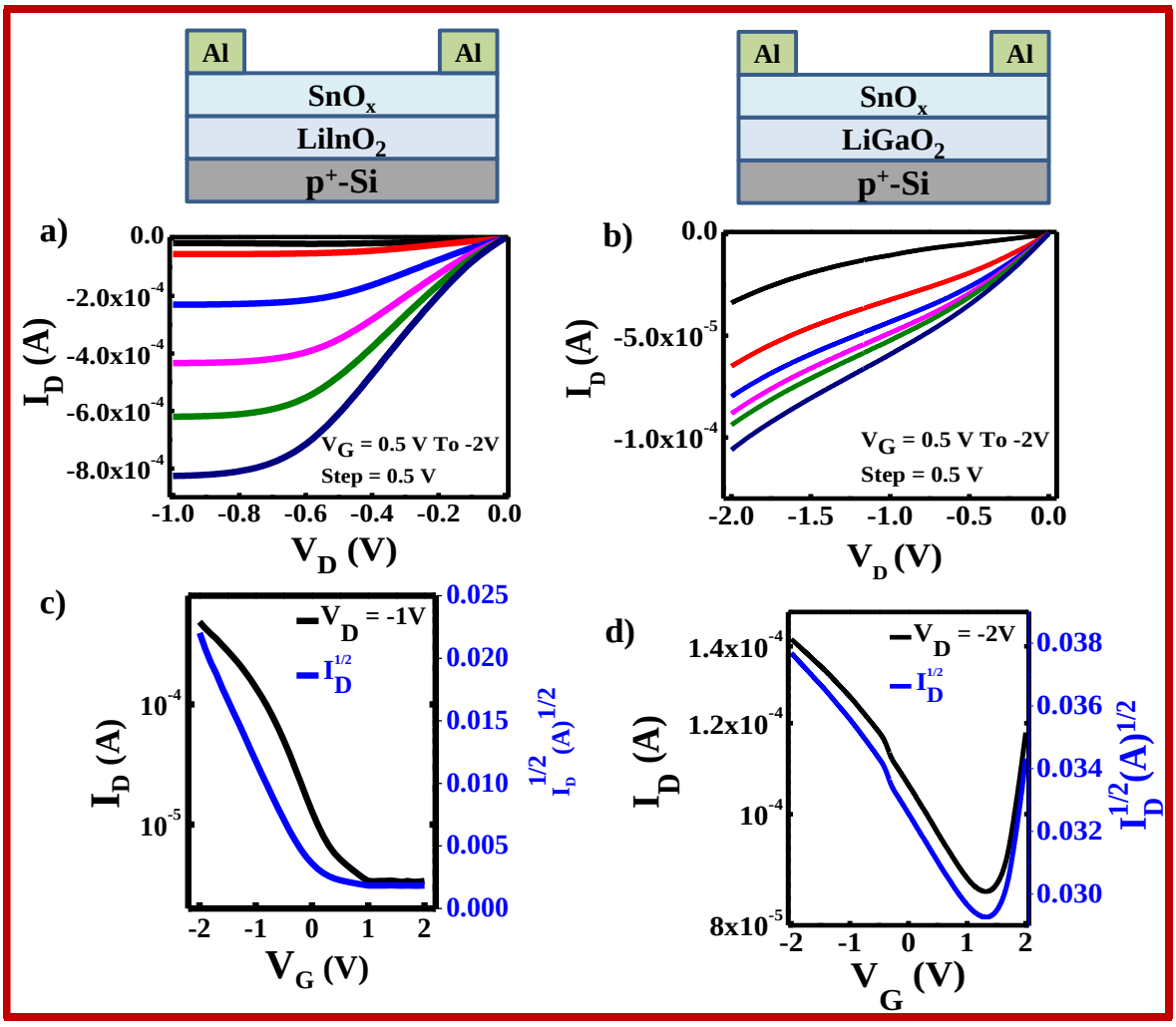

Figure 4.9: a) *Output and* ***c)*** *transfer characteristics of the SnO_2 TFT with $LiInO_2$ dielectric annealed at 550 ^oC,* ***b)*** *Output and* ***d)*** *transfer characteristics of the SnO_2 TFT with $LiGaO_2$ dielectric annealed at 550 ^oC with device architecture $Al/SnO_2/LiInO_2/p^+$-Si, and $Al/SnO_2/LiGaO_2/p^+$-Si under p-channel operation, respectively.*

The effective mobility of the carrier (μ) and sub-threshold voltages (SS) of this TFT is calculated from the following equations;

$$I_D = \mu C \frac{W}{2L}(V_G - V_T)^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

$$SS = \left[\frac{d(\log I_D)}{dV_G}\right]^{-1} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

Where I_D, C, V_G, V_T are saturation drain current, capacitance per unit area, gate voltage, and threshold voltage. Since the TFT operation was performed in direct voltage, the capacitance at a lower frequency (50 Hz) is taken into account for the calculation of mobility to avoid overestimation. The threshold voltage of the device can be calculated by fitting a straight line on $I_D^{1/2}$ vs. V_G plot of transfer characteristics. The extracted carrier mobility and threshold voltage for n-channel and p-channel operations of TFT1 are 7 $cm^2 V^{-1} s^{-1}$, 0.2V and 8 $cm^2 V^{-1} s^{-1}$, 0.3V respectively. To the best of our knowledge, as an ambipolar transistor, these are the highest achieved mobilities among all reported organic/polymer or oxide devices.

Moreover, those above mobility suggests that there is a balance injection of both types of charge carriers (i.e., electron and hole), which is very necessary for CMOS electronics, are not commonly found in earlier organic/polymer or inorganic oxide-based ambipolar TFT. In addition to carrier mobility, two other parameters determine TFT device quality. One of them is the current on/off ratio, and the other one is the device's sub-threshold swing (SS). The on/off ratio of the device with n-channel and p-channel operation is 60 and 1.5 x 10^2, respectively. On the other hand, the subthreshold swing of the device is 1.31 V dec^{-1} (for n-channel) and 0.97 V dec^{-1} (for p-channel), respectively. Again as an ambipolar TFT, these on/off ratio are quite high, and SS values are significantly low, which are required CMOS inverter circuit. In addition to TFT1, TFT2 also shows a very good n-channel behavior with electron mobility, on/off ratio, and ss values 0.35 $cm^2 V^{-1} s^{-1}$, 10^2 and 1.46 V/decade, respectively. However, this device show p-channel behavior with a hole mobility of 0.59, on/off ratio of 2, and SS value of 1.12 V/decade. However, the electron and hole mobility of TFT2 is more than one order lower w.r.t TFT1. In contrast, TFT3 shows only n-channel behavior with electron mobility of 16 $cm^2 V^{-1} s^{-1}$, on/off ratio of 10^3 and SS value of 0.41

V/decade, which indicates a very good n-channel transistor but doesn't show any p-type transport in the channel. The device parameters of all these TFTs are summarized in **Table 4.1**. The comparative study of these three different TFTs indicates that the device with $LiInO_2$ dielectric shows the best ambipolar field-effect transistor behavior with very high mobility at the low operating voltage with good on/off ratio and low subthreshold swing. This outstanding performance of TFT1 indicates that this combined dielectric/semiconductor device architecture great potential to give a big boost of ambipolar TFT research.

To realize this comparative electrical behavior, we proposed a dielectric/semiconductor interfacial doping phenomenon, which has been described in **figure 4.10**. An n-type oxide semiconductors have high electron affinity. The charge neutrality point of these oxide semiconductors is commonly existed in mid-gap or above the mid-gap that limits the p-doping of these semiconductors. However, the hole conduction of an oxide semiconductor is possible if the activation energy of the acceptor level is low enough. As per the earlier report, group IIIA elements work as an acceptor of SnO_2 semiconductor.[182] Out of these different group IIIA elements, In and Ga have been theoretically predicted to introduce shallow acceptor with an activation energy of 580 and 760 meV **figure 4.10 a) and figure 4.10 b)**. [65, 183] Besides, experimental reports also show that the initial addition of In or Ga doping increases the resistance of the SnO_2 semiconductor by two orders of magnitude. During this period, conduction due to electron steeply decreases, and hole conduction introduces, which reaches the peak value for the highest level of doping ($\sim 10^{17}/cm^2$).[183] However, after crossing the maximum level of doping concentration, resistivity rapidly decreases, and hole conduction disappears, which is due to the formation of In_2O_3 or Ga_2O_3 secondary phases in the SnO_2 thin film that works as a pure n-type semiconductor.[183] In our present work,

during the annealing process of SnO_2 semiconductor, In or Ga has been thermally diffused to the SnO_2 through the SnO_2/ion-conducting dielectric interfaces, which introduced shallow acceptor to the interfacial SnO_2 **figure 4.10 c)**.[184] Again, we should keep in mind that the conducting channel of TFT is formed in the dielectric/semiconductor interfacial layer of the device.[153, 185] Therefore, this shallow acceptor introduce hole conduction to the channel of TFT1 and TFT2. As it mentions earlier, acceptor activation energy due to In doping is relatively lower than Ga,[183] **(figure 4.10 a) & b))** therefore, compared to TFT2, TFT1 shows better hole conduction and shows a more balanced electron and hole transport. However, this acceptor doping can not be introduced by the group IIB Zn atom.[99]. Thus, TFT3 doesn't show any hole conduction.

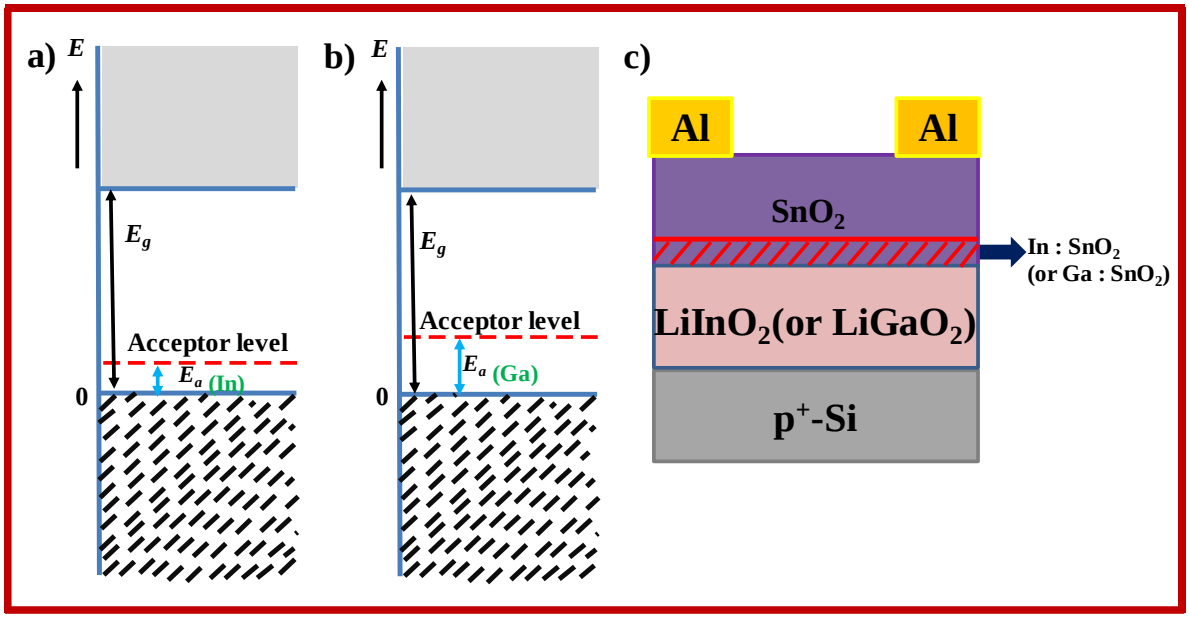

Figure 4.10: *Schematic of deep acceptor level with tin oxide (SnO_2) for* ***a)*** *In,* ***b)*** *Ga, respectively and* ***c)*** *schematic presentation of dielectric/semiconductor interfacial doping.*

Table 4.1: The summary of different device parameters of three SnO_2 TFTs fabricated with three different ion-conducting oxide dielectrics

Device no.	Dielectric	Dielectric Annealed temperature	C (nF/cm^2) at 50 Hz	V_{Th} (V)	ON/OFF	Subthreshold swing (SS) (V/decade)	Mobility (μ) ($cm^2\ V^{-1}\ sec^{-1}$)
1.	$LilnO_2$ (n-operation)	550 °C	478	0.2	60	1.31	7
2.	$LilnO_2$(p-operation)	550 °C	478	0.3	1.5×10^2	0.97	8
3.	$LiGaO_2$ (n-operation)	550 °C	350	-0.4	10^2	1.46	0.35
4.	$LiGaO_2$ (p-operation)	550 °C	350	1.1	2	1.12	0.59
5.	Li_2ZnO_2 (n-operation)	500 °C	312	0.3	10^3	0.41	16

To verify the applicability of this SnO_2 based TFTs in CMOS circuit, an inverter was built by connecting two TFT1 side-by-side with identical channel dimensions for both TFTs (L=0.2 mm, W=23.6 mm). In this inverter, the gate electrodes of both TFTs are common that serves as the input terminal V_{in} as shown in **figure 4.11**. **Figure 4.12 a)** and **figure 4.12 b)** represents the inverter characteristic at supply drain voltage V_D of +1V and -1V, respectively. When the supply voltage V_D was kept at +1V, V_{in} was varied from 0 to 2V. Under this condition, TFT1 works as a p-channel transistor of a regular CMOS inverter while TFT2 operates as the n-channel device. Therefore, in positive gate bias, TFT1 operates in depletion mode and doesn't conduct current that results in a high V_{out}. Under this biasing,

inverter works in the first quadrant, and the output voltage V_{out} vs. V_{in} plot exhibit a maximum gain of 13, which is shown in **figure 4.12 c)**. On the other hand, if the V_D is biased with -1V and V_{in} varies from 0 to -2V (**figure 4.12 d)**), the inverter works with a gain of 12, which is represented in the third quadrant with n- and p-channel function exchanged between the two devices. The most advantageous side of this study is its low operating voltage with its reasonably good gain. As was shown, this inverter needs only $|V_D| = 1V$ whereas, $|V_{in}|$ needs to vary from 0 to 2V. The performance of such a solution-processed low operating voltage inverter is rarely reported in the literature.[62]

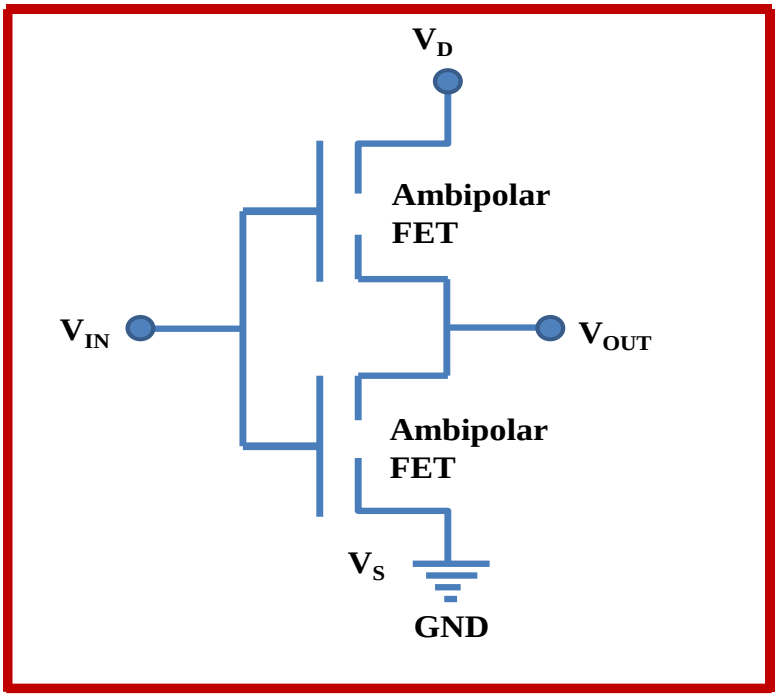

Figure 4.11: *Schematic demonstration of the electrical networks for the inverter based on two identical ambipolar transistors.*

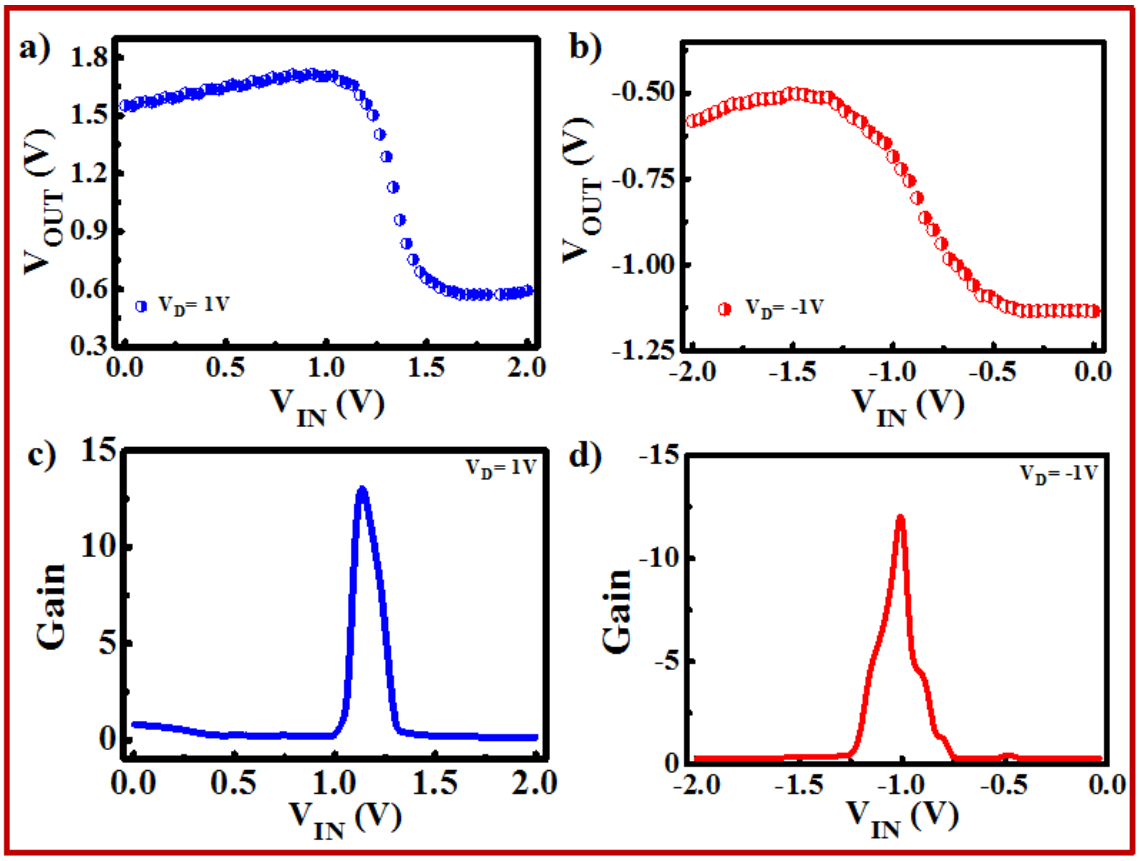

Figure 4.12: *Inverter characteristics for* ***a)*** *first and* ***b)*** *third quadrants with supply voltages (V_{DD}) of ± 1V, respectively, and corresponding gain of the complementary inverter* ***c)*** *first and* ***d)*** *third quadrants under the supply voltages (V_{DD}) of ± 1V, respectively.*

4.5 Conclusion

In summary, $LiInO_2$ and $LiGaO_2$ ion-conducting oxide gate dielectrics containing trivalent In and Ga, respectively, have been developed by a low-cost solution-processed technique and have been successfully applied as a gate dielectric in oxide-based ambipolar TFT. The electrical conductivity of these dielectric thin films shows the insulating nature, which is an essential condition for using these ion-conducting oxide thin films as a gate dielectric of TFT. During semiconductor (SnO_2) thin-film fabrication on top of the ionic dielectric, the interfacial SnO_2 layer gets p-doped by those trivalent atoms resulting in hole conduction characteristic of the TFT. This phenomenon has been justified comparing with a reference

TFT having Li_2ZnO_2 dielectric that doesn't show any p-type conduction. Our comparative electrical data reveals that TFTs with $LiInO_2$ and $LiGaO_2$ dielectric is ambipolar. Moreover, this $LiInO_2$ dielectric based TFT can be operated at 1V and shows balanced ambipolar TFT behavior with a high electron and hole mobility values of 7 $cm^2\ V^{-1}\ s^{-1}$and 8 $cm^2\ V^{-1}\ s^{-1}$, respectively with an on/off ratio $>10^2$ for both operations. A low-voltage CMOS inverter has been successfully demonstrated in this work by utilizing the ambipolar TFTs developed here. Overall, this new technique of fabricating low operating voltage ambipolar oxide TFT opens up a new direction for developing high-performance ambipolar TFT.