Chapter 1

The main motivation of the current thesis is to synthesize the low band gap, ion-conducting oxide dielectric using a cost-effective sol-gel process for the application in low operating voltage thin film transistor (TFT). Specifically, my target was to develop low operating voltage ambipolar oxide and graphene transistor using those ion-conduction gate dielectric and their application for CMOS and chemical sensors. Besides, I have also fabricated n-type oxide TFT using an ion-conducting dielectric.

In this introduction chapter, I have discussed key components of TFT, different device architecture, the working principle of TFT, device parameters, etc. Since this thesis work mainly focused on developing high-k dielectric for the application of low operating voltage TFT, therefore, I have discussed different high-k dielectric, charge polarization mechanisms of dielectric and foremost criteria of high-k dielectrics for the implementation of low operating voltage TFT. Besides, I have discussed different semiconducting materials, including metal oxide and graphene. A summary has been given on the development of solution-processed low voltage TFT. At the end of this introduction, the scope of the thesis has been discussed.

1.1 Key components of a TFT

From the beginning of the discovery, transistors are a single dominant feature in the microelectronics industry as a building block for logical circuits, and this makes an innovative impression on every aspect of human life. J. E. Lilienfeld is commonly credited with the invention of the first field-effect transistor, and the idea was patented in 1934[1], but the first working TFT was reported by Paul K. Weimer at Radio Corporation of America

(RCA) laboratories in 1960.[2] RCA announced the development of the first LCD (liquid crystal display) using TFT in the later 1960s.[2] Such TFTs are the unipolar device that uses a single form charge carrier to conduct current, i.e., electron or hole. This conduction is regulated by an electric field applied to the gate electrode, which in turn activates the amplification of the signal. The TFTs are designed using three key components i) a dielectric layer, ii) a semiconductor layer, and iii) metallic electrodes (source (S), drain (D), and gate (G)) as shown in **figure 1.1**. In the dielectric layer, gate dependence charge polarization is formed to achieve current modulation in the semiconductor channel. The accumulated charge carriers are then can be injected or extracted through the metallic source/drain electrode.

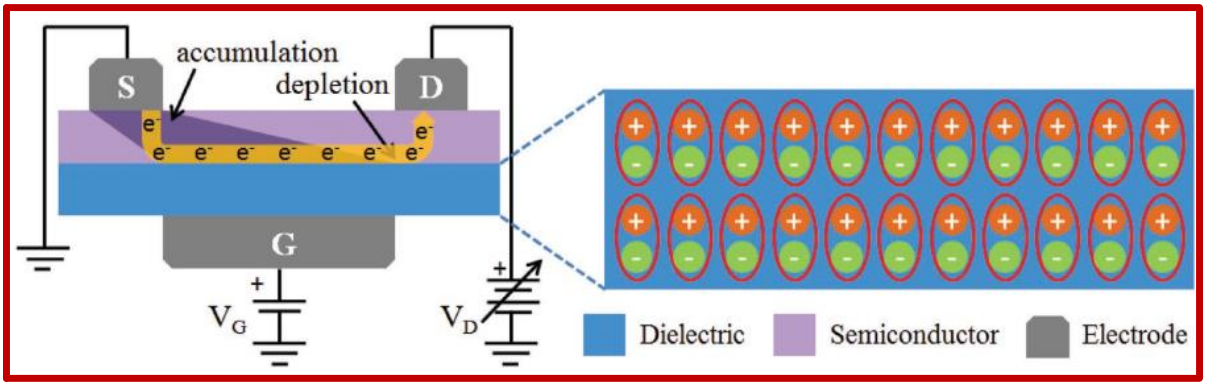

Figure 1.1: *Schematic diagram and charge transportation in TFT channel under the applied electric field with bottom gate top contact geometry.*

1.2 Different device configuration of TFT

Depending upon geometry, there are four basic structures of TFT a) staggered top gate (STG), b) staggered bottom gate (SBG), c) coplanar top gate (CTG), and d) coplanar bottom gate (CBG), as shown in **figure 1.2**. There are different advantages and disadvantages to each geometry; however, transistors of the same material with different geometries may have very different behaviors. The staggered bottom gate (SBG) is used frequently to fabricate high-performance TFT, which is due to the smaller contact resistance of source/drain electrodes that helps easy charge injection to the channel. Besides, the manufacturing steps of

this device structure is easier with respect to the other structures. Because of these reasons, in this thesis, I have worked mostly with this SBG geometry.

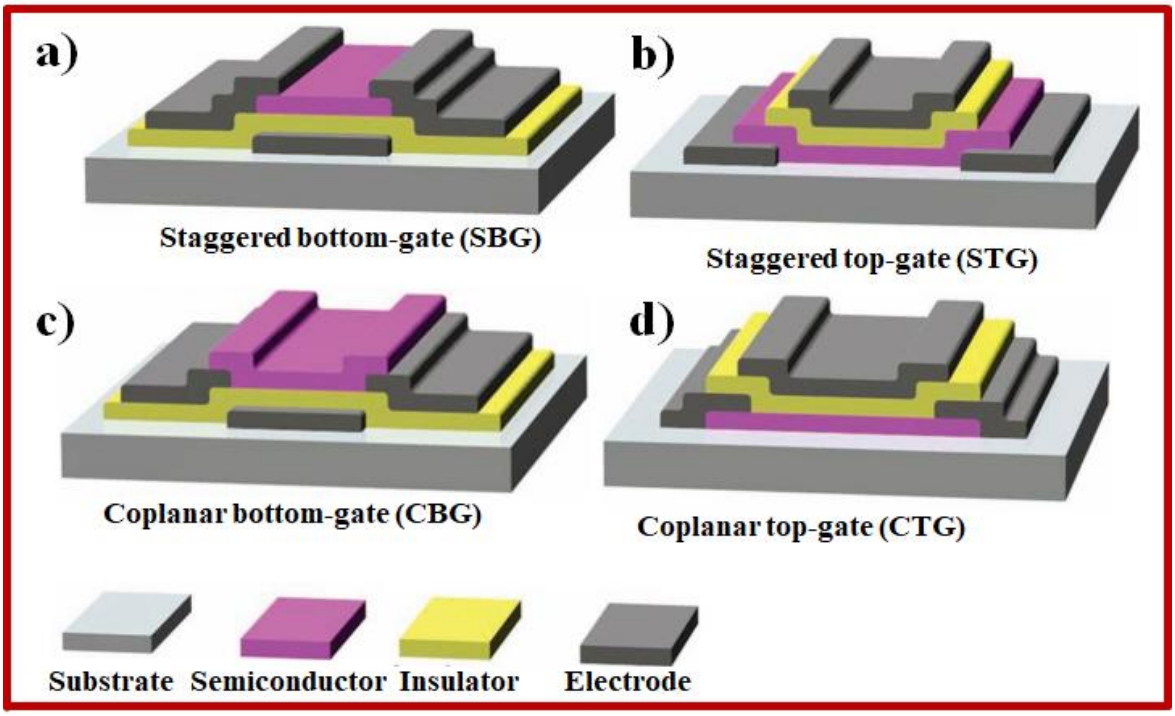

Figure 1.2: *Schematic diagram of the configuration of TFT* ***a)*** *staggered bottom gate* ***b)*** *staggered top gate* ***c)*** *coplanar bottom gate and* ***d)*** *coplanar top gate, respectively.*

1.3 Operation principle of TFT

In comparison to the metal–oxide–semiconductor field-effect transistor (MOSFET), which usually works in depletion mode, thin-film transistors are primarily used in accumulation mode. Using the positive or negative gate voltage (V_G), the polarization of charge in dielectric materials is electrostatically carried out while the source voltage is usually grounded. At the dielectric-semiconductor interface, such polarization permits the accumulation of charge carriers (electrons or hole) in n- or p-type semiconductors, respectively. Therefore, a conducting channel between source and drain is formed due to such accumulation of charge carriers in the semiconductor.[3] The accumulated charge carrier density is approximately proportional to the gate voltage and the capacitance of an

insulator. A drain voltage (V_D) regulates the drain current (I_D) in the active layer between the drain and the source electrode. If $V_D < (V_G-V_T)$, a uniform charge carrier density is formed in the channel. The current-voltage (I-V) relationship in a TFT can be derived using the ohmic current gradual channel approximation and analyzed using an equation (1) that leads to the linear region.[4]

$$\boldsymbol{I_{D,Lin} = \frac{W}{L}\mu_{Lin}C_i(V_G - V_T - \frac{V_D}{2})V_D} \quad \text{..... (1)}$$

Where, W, L, and μ are referred to as channel width, channel length, and charge carrier mobility. On the drain side, the channel is pinched-off, saturating the drain current at a specific V_D value that is $V_D > (V_G-V_T)$. The saturation region drain current can be calculated with the help of equation (2) as given below, which is generally preferred in most of the TFTs [4]

$$\boldsymbol{I_{D,Sat} = \frac{W}{2L}\mu_{Sat}C_i(V_G - V_T)^2} \quad \text{..... (2)}$$

1.4 Device parameters of a TFT

Depending on the polarity of charge carrier, TFT can be divided into three types such as; i) n-channel TFT, where dominating charge carrier are the electrons, ii) p-channel TFT, where dominating charge carrier are holes and iii) ambipolar TFT, where both charge carrier, i.e., electron and hole are present at the channel of TFT as shown in **figure 1.3**. Type of charge conduction of an ambipolar TFT can be altered by changing the polarity of the applied gate and drain voltage, and depending upon on those biasing, a single TFT can work either as n-type or p-type TFT.

Generally, current-voltage characteristics of TFTs are described in two ways named as output characteristics and transfer characteristics. For constant V_G, the variation of I_D with V_D is

called the output characteristics of a TFT. The quality of TFT is demonstrated by a consistent linear and saturation region of I_D and by progressive enhancements of I_D with V_G. On the other hand, for constant V_D, the variation of I_D with V_G is called the transfer characteristics of a TFT, which gives us all essential parameters of the device such as on/off ratio, threshold voltage, carrier mobility, and sub-threshold swing.

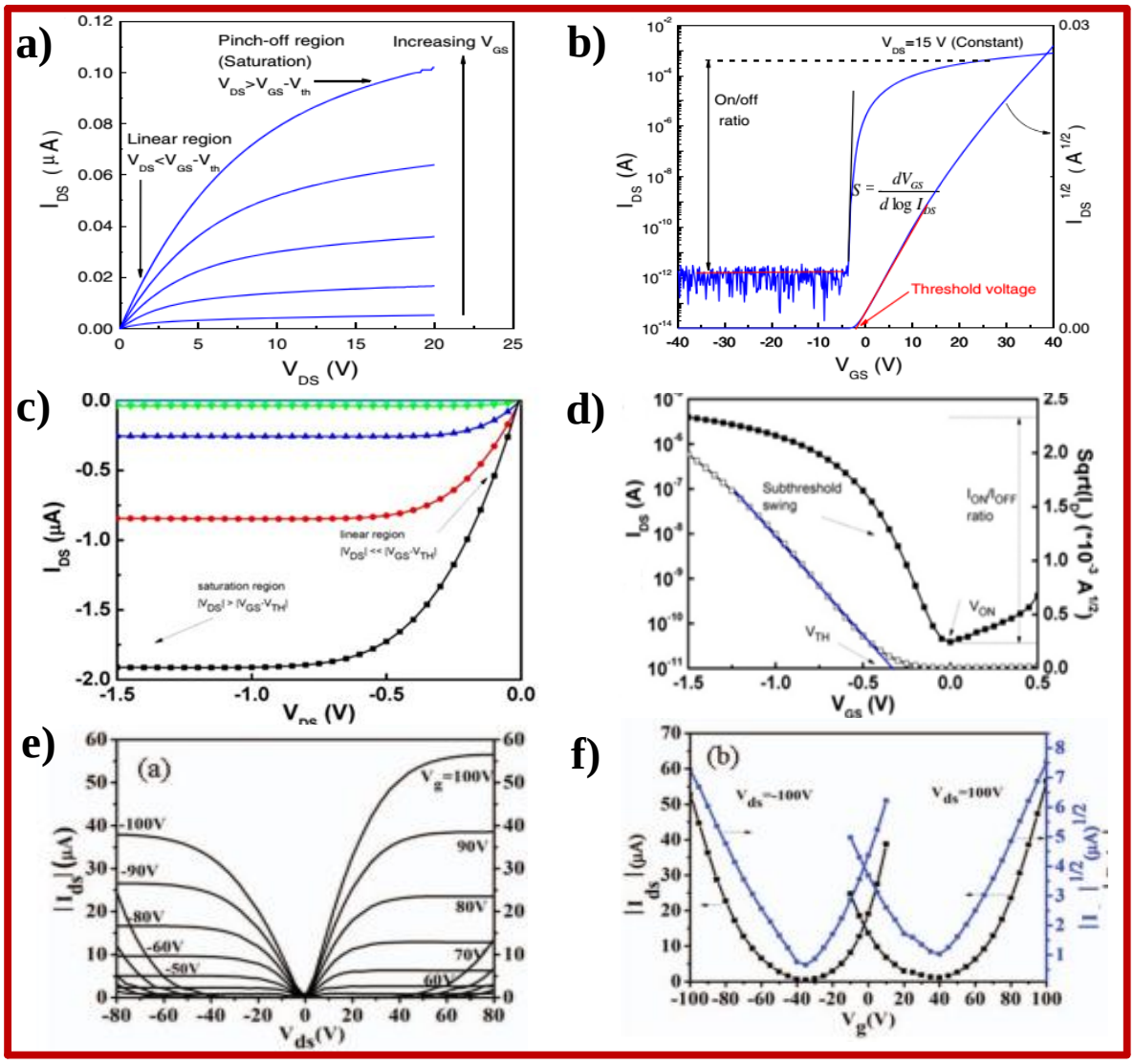

Figure 1.3: *Typical* ***a), c), e)*** *output and* ***b), d), f)*** *transfer characteristics of an n-type, p-type and ambipolar oxide TFT, respectively.* [5, 6]

1.4.1 Carrier mobility (μ) of a TFT

Carrier mobility (μ) is the most critical parameter of the TFT, which measures the transportation of the charge carriers in the device. In thin-film content, various dispersion parameters may affect μ value, such as lattice thermal vibrations, ionized impurities and lattice mismatch at grain boundaries, including unwanted impurities within crystal frameworks. Mostly in a TFT, carrier movement in the channel is restricted to a narrow region near the dielectric/semiconductor interface.[7] Mobility can be easily calculated by differentiating equation (1) and (2) in linear and saturation regimes. Mobility is extracted by the following equation within the linear region;

$$\mu_{Lin} = \frac{L}{WC_iV_D}\left(\frac{\partial I_{D,Lin}}{\partial V_G}\right)$$

In the same way, mobility in the saturation region can be calculated as

$$\mu_{Sat} = \frac{2L}{WC_i}\left(\frac{\partial \sqrt{I_{D,Sat}}}{\partial V_G}\right)^2$$

1.4.2 On/Off ratio of a TFT

The on/off ratio is an important parameter of TFT, which can be extracted from the transfer characteristics and defined as the ratio of highest (on-state) to lowest (off-state) drain current at the flat band gate voltage. The highest value of I_D is governed by semiconductor material as well as the capacitance value of gate dielectric while the lowest I_D is usually given by the gate leakage current (I_G), the sheet resistance of the channel and by the noise level of the

measurement apparatus. The on/off ratio will often be as large as possible to get good switching behavior of TFT and commonly find the range of 10^3 to 10^8.

1.4.3 Sub-threshold swing (SS) of a TFT

Sub-threshold swing (SS) is defined as the requirement of V_G to change the order of I_D by one decade. SS reflects the transistor switching speed, i.e., how easily a transistor switches from 'off' to 'on' state. The SS value of a TFT can be determined using equation (3) from the transfer curve [8]

$$\mathbf{SS} = \left[\frac{\mathbf{d(\log I_D)}}{\mathbf{dV_G}}\right]^{-1} \quad \text{......} \quad \mathbf{(3)}$$

1.4.4 Interface trap density(N_{ss}^{max})

Interface trap density(N_{ss}^{max}) related to the sub-threshold slope, which tells about the preeminence among dielectric and semiconductor. The expression of $N_{ss}^{max}$is given below[9]

$$\mathbf{N_{SS}^{max}} = \left[\frac{\mathbf{SS \times \log e}}{\mathbf{kT/q}} - \mathbf{1}\right]\frac{\mathbf{C}}{\mathbf{q}} \quad \text{......} \quad \mathbf{(4)}$$

Here SS is subthreshold swing, K is Boltzmann constant, T is absolute temperature, C is the capacitance of dielectric, and q is the elementary charge.

To achieve high carrier mobility, the value of (N_{ss}^{max}) should be smaller, which can be possible from an excellent dielectric/semiconductor interface formation. From equation (4), it is clear that (N_{ss}^{max}) depends on the capacitance of the dielectric layer and SS of the device. Since the accumulation of charge carriers at the interface is directly proportional to the capacitance of the dielectric, hence greater the capacitance, the higher the accumulation.

1.4.5 Threshold Voltage (V_T) of a TFT

The minimum V_G that requires to start accumulation of charge carrier at the interface to form a conducting channel is known as threshold voltage (V_T), which can be calculated by extrapolating the straight line of $I_{DS}^{1/2}$ vs. V_G curve. There are different parameters on which threshold voltage V_T of TFTs depend, e.g., nature of dielectric material, the thickness of the semiconductor film, and dielectric/semiconductor interface trap state, etc.[10]

1.5 High-k dielectrics

Silicon dioxide (SiO_2) is a complimentary gift from nature to MOSFET society, with nearly all the ideal gate dielectric properties.[11, 12] However, the major drawback of this dielectric is that the lower dielectric constant (κ), which requires high operating voltage to operate the device and restricts its application to low-power portable electronics. Moreover, semiconductor industries need the miniaturization of the complementary metal-oxide-semiconductor (CMOS) transistors for which the thickness of the SiO_2 gate insulator needs to be below 1 nm in the next generation of transistors with a channel dimension of less than 45 nm.[13] Under this thickness, the current gate leakage significantly increases due to the effect of quantum mechanical tunneling.[11, 12] This is a limiting factor that can not easily be solved without the quest for new device structures or dielectric materials.[14] The use of high-k dielectrics material is one of the most promising options to solve this issue. The term high-k dielectric refers to a material that has a significantly greater dielectric constant (κ) than SiO_2. The replacement by metal oxides of higher dielectric constant for SiO_2 gate dielectrics led to the research on a wide variety of materials of superior quality compared to SiO_2. The introduction of substantially thicker high-k dielectrics but keeping the similar capacitance per unit area, permits enhanced device performance having in high current at low

operation voltages which is useful for low power consumption devices.[15] The capacitance of dielectric can be calculated according to the **equation (5)**

$$C = \frac{k\varepsilon_0 A}{d} \qquad \text{……} \quad (5)$$

Where C is the capacitance of the dielectric, k is dielectric constant, A is an area of the electrode, and d is stated as dielectric thickness.

1.6 Dielectric charge polarization mechanism and dielectric polarization between two electrodes

Generally, the dielectrics are insulator and can be polarized in the presence of the electric field. Therefore, when an insulator is placed under the electric field because of the lack of free carrier (electron and hole), DC current can not flow through these materials; as an alternate, different types of charge polarization phenomena occur. This phenomenon is known as dielectric polarization. The different mechanisms of polarization of the materials are summarized and shown in **figure 1.4.** As described, this dielectric polarization can be due to the electronic polarization, ionic polarization, and the orientation of the molecule of the gate dielectric. Besides, chain relaxation counter ions, space charges, and the electrode or electric double-layer (EDL) polarization can also cause dielectric polarization phenomena.[16-18] Nevertheless, in the entire frequency spectrum of external bias, all those polarization mechanisms are not equally involved. The figure shows all different polarization pathways with their active frequency spectrum.[3]

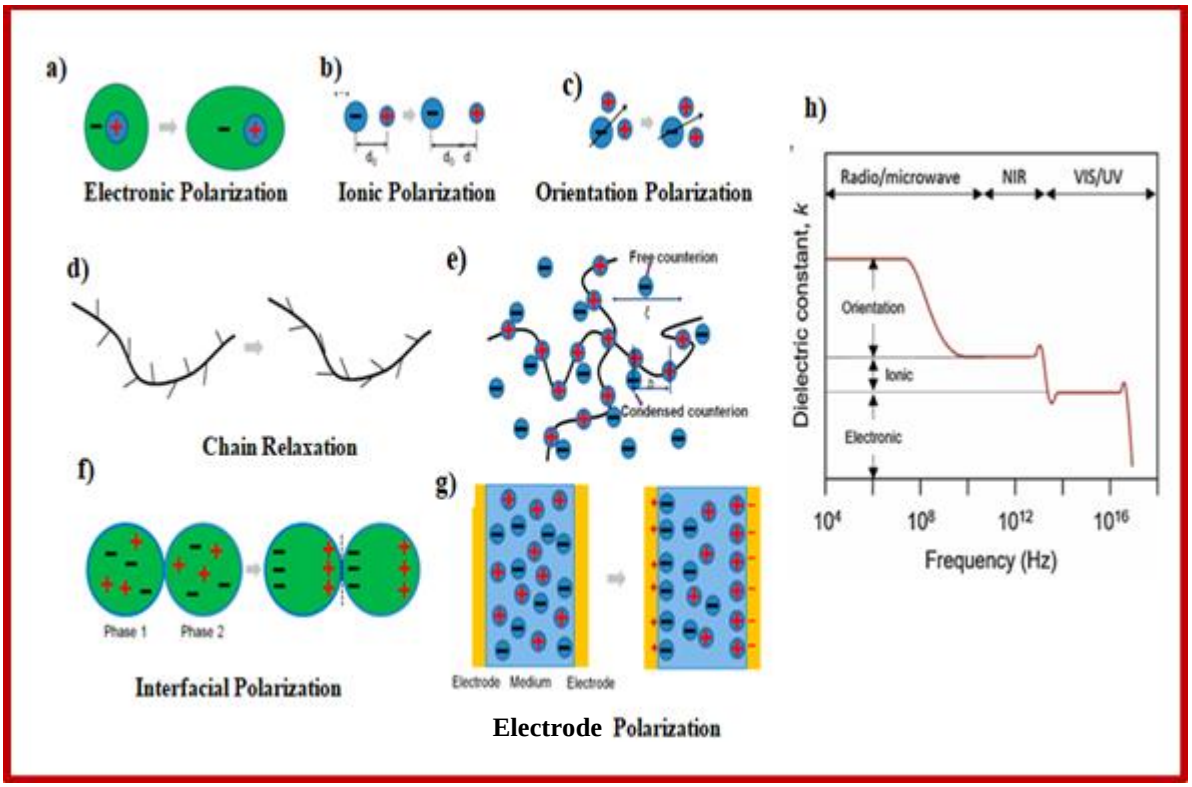

Figure 1.4: *Different polarization mechanism of dielectric;* ***a)*** *electronics polarization,* ***b)*** *ionic polarization,* ***c)*** *orientation polarization,* ***d)*** *chain relaxation,* ***e)*** *free counter ion polarization in an electrolyte,* ***f)*** *interfacial polarization,* ***g)*** *electrode or EDL polarization and* ***h)*** *the influence of the different polarization mechanism to the dielectric constant with several frequency regions, respectively.*

Dielectric insulators between two electrodes are distinguished by the lack of charge transport under an applied electric field. The mechanism of a dielectric is similar to a parallel plate capacitor, as shown in **figure 1.5**. In the absence of electric field, charge distribution is random, but under the electrical field, polarization occurs throughout the dielectric material by adding a positive bias to the bottom metal plate resulting in the form of a net dipole moment distributed across the thickness, producing a surface charge density at the top and bottom of the dielectric. The polarization phenomenon which occurs in the dielectric can be seen in **figure 1.5.**

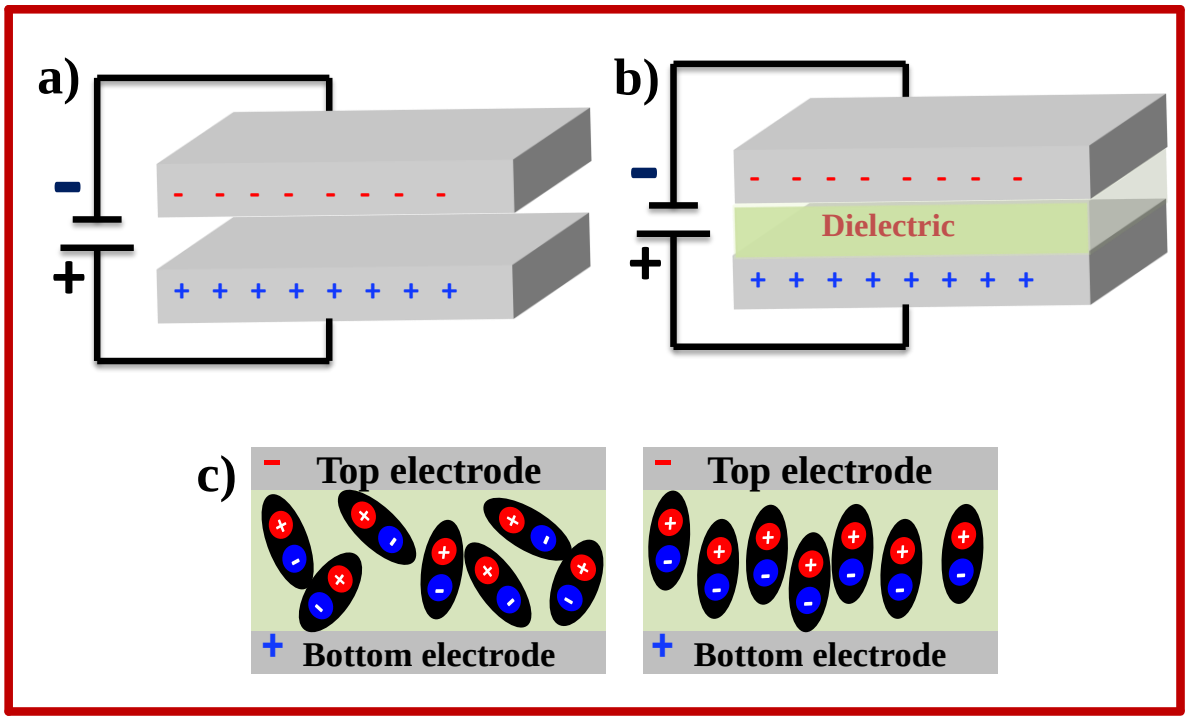

Figure 1.5: *Schematic diagram of the basic mechanism of parallel plate metal-insulator-metal capacitor* ***a)*** *without dielectric layer,* ***b)*** *with a dielectric layer, and* ***c)*** *dipole polarization mechanism under the absence and presence of an applied electric field, respectively.*

1.7 Criteria to choose high-k dielectric

The energy band gap of dielectric materials has an inverse relation with the dielectric constant (κ) of the materials. On the other hand, lower band gap materials have a tendency of having higher leakage current through the band edge offset. Therefore, for developing a new dielectric, the tradeoff between the energy band gap and the dielectric constant need to be realized. **Figure 1.7** shows the variation of different dielectric materials as a function of its dielectric constant. J. Robertson et al. outlined the conditions that a candidate for gate oxide would follow.[19] For an ideal gate oxide dielectric, all criteria must be followed by that dielectric. The specifications of a new oxide for CMOS and memory applications (unlike TFTs) are six-fold as shown in **figure 1.6**.

1. Dielectric constant (κ) must be sufficiently high for rational scaling years. The required dielectric oxide constant should exceed 10, ideally 25-30, for gate dielectric applications. Nevertheless, the k- is compensated for by the band offset.[20] The k-value of dielectric appears to differ in reverse with the bandgap.

2. The oxide interacts directly with the material of the channel and must, therefore, be thermodynamically stable. Since channel material is governed by interface reactivity over the electrical properties of electronic devices, no high-k reactivity can occur with channel material to avoid parasitic interfacial layers.

3. It has to be kinetically stable and consistent with the temperature range for processing. Devices can also be handled with an annealing cycle post-deposition. The high-k dielectric will remain stable, without any structural change.

4. It must serve as an insulator to reduce carrier injection into its bands by providing band offsets with a semiconductor of more than 1 eV.

5. It needs to form an excellent electric interface with the material in the channel to ensure a low trap density of the structure.[14]

6. There must be a few electrically active defects in bulk. Usually, high-quality products have high densities associated with stoichiometric defects such as oxygen vacancies because of their manufacturing temperature.

Figure 1.6: *Benchmarks to select the high-k dielectric for a thin film transistor.*

1.8 Dielectric for low operating voltage TFT

Over the past decade, different synthesis techniques have been developed for growing high-k dielectric those out form the performance of TFTs. These newly developed dielectrics can be divided into several categories, e.g.: high-k metal oxide dielectrics[21-25], ion-gel dielectrics[26-28], ion-conducting oxide dielectrics[29-32], self-assembled monolayer (SAM)[33-35], self-assembled multilayer nanodielectrics (SANDs)[36-38], polymer electrolyte dielectrics[39-41], and nanostructured and nanocomposite dielectrics.[42-45] Among these listed dielectrics, SAM is used extensively in the fabrication of organic/polymer low-voltage as well as mechanically flexible TFT. Also, SANDs are another common dielectric for the manufacturing of organic TFT, similar to SAM. Ion-gel dielectrics were used more frequently to produce organic/polymer TFTs, which show some extra

benefits over SAM or SANDs dielectrics. All of these three dielectrics, however, are not a very good choice for the fabrication of high-temperature processed metal-oxide TFT. In this regard, ion-conduction metal oxide dielectrics are one of the best choices over other high-k dielectrics. These ion-conduction dielectrics can be deposited by a solution-processed technique. Moreover, these dielectrics are fabricated from low cost, eco-friendly and earth-abundant materials. This type of dielectric always includes light-weight metal ions (such as Na^+, Li^+, $K^{+,}$ etc.) that are capable of moving freely through the crystal channel, and because of this, the dielectric thin film can be easily ionically polarized by external bias. Instead of having excellent ionic conductivity, such dielectric materials are electronically highly insulating and have a wider band gap. These are combining special features makes this class of materials as a unique choice of gate dielectric for fabricating low voltage TFTs.

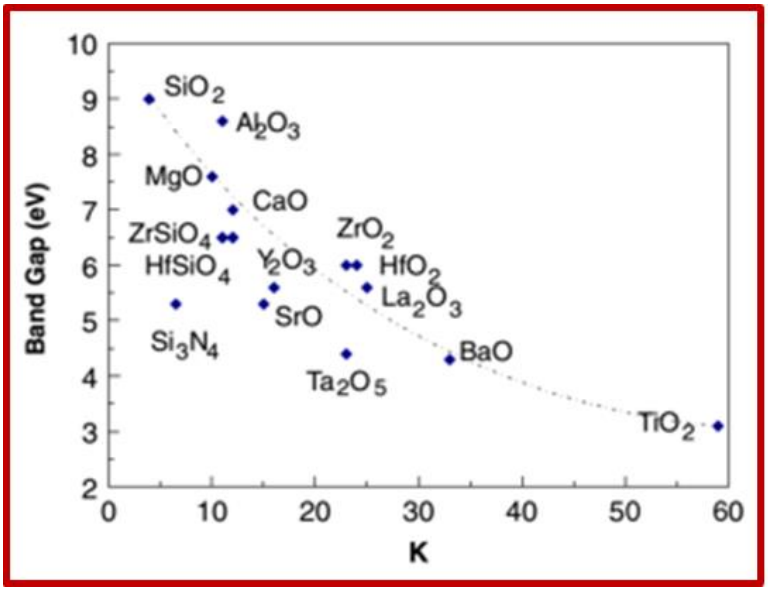

Figure 1.7: *Schematic of dielectric constant vs. measured bandgap of the several metal oxide dielectric.[46]*

1.9 Metal oxide semiconductor

The high carrier mobility of a semiconductor is not the most extreme design requirement, and single crystal silicon is not the leading semiconductor for application in large-area electronics due to their higher manufacturing costs. Relatively, polycrystalline and amorphous silicon/oxide semiconductors and organic/polymer semiconductors are the most preferred choices.[47, 48] In 1954, tin-doped indium oxide (In_2O_3: Sn), which is commonly known as indium tin oxide (ITO), was published as the first transparent conducting oxide (TCO) material.[49] From then, consistent efforts have been given to study the electric conductivity of metal-oxide materials, which reveals the existence of a number of an amorphous oxide semiconductor (AOS). These AOS are potential candidates as a transparent semiconductor for TFT materials that have made a remarkable development, especially in the case of display applications in a relatively short time.[50, 51] Besides this, a metal oxide semiconductor has unique properties, e.g., high optical transparency, low processing temperature, and outstanding eco-friendly/thermal stability. Also, AOSs do not have grain boundaries, thus avoiding the main restriction of mobility in polycrystalline semiconductors, which is an enormous advantage for process integration and particularly for large-area applications.

AOS composed of post-transition metal cations with $(n-1)d^{10}ns^0$, where n>4. The electronic configurations organize a new subclass of transparent conductors since they acquire relatively high electron mobilities despite their amorphous character. The valence band and conduction band are produced by highly directional sp^3 orbitals in silicon. However, in single crystalline silicon, high charge carrier mobility (>1000 $cm^2\ V^{-1}s^{-1}$) is ascribed to a massive overlap of sp^3 orbitals and large conduction band spreading in the periodic single-crystal structure. Nevertheless, amorphous Silicon (α-Si: H) has the minute overlap of sp^3 orbitals is

inappropriate for conduction band spreading and thus limits the mobility to < 1 $cm^2 V^{-1} s^{-1}$. In contrast, for AOS materials, the conduction band minimum (CBM) creates the electron conduction pathway, which is collected from vacant metal cation s-states. When the spatial area of these s-states is greater than the interatomic distances, AOSs displays the electron mobilities comparable to those of the corresponding crystalline phase.[52, 53] The principal quantum number (n) primarily depicts the spatial overlap of the s-state; therefore, heavy post-transition metal cations with $(n–1)d^{10}ns^0$ electronic configurations, where n > 4, are ideal AOS candidates. Both In^{3+} and Sn^{4+}, with the same $[Kr](4d)^{10}(5s)^2$ electronic configuration, meet this requirement.

Similar to all other semiconductors, the electronic properties of metal oxides semiconductors are most accurately described by their band structures. However, the interaction between the metal and oxygen orbitals leads to more complicated electronic structures and also a significant disparity between electron and hole conduction in any given species. In a covalent semiconductor such as silicon (Si), the conduction band minimum (CBM) and the valence band maximum (VBM) are attributed to the anti-bonding (sp^3 s*) and bonding (sp^3 s) states of Si hybridized orbitals. Therefore, the band gap is given as the energy difference of the sigma*–sigma levels.[54] In contrast to this, metal oxide semiconductors are valence compounds with a high degree of ionicity within their chemical bonding. This ionicity creates an electronic structure that differs from covalent semiconductors.

For hole conduction in metal oxide, the VBM has to be considerably more dispersive, and the effective hole mass needs to be significantly smaller, which is quite difficult for most of the metal oxide semiconductors. One family of materials that are currently attracting significant interest is the Cu(I) based compounds and includes cuprous oxide Cu_2O, delafossites $CuMO_2$

(M = Al, Ga, or In), and oxychalcogenides LaCuOCh (Ch = S, Se, or Te).[55, 56] A common feature in this Cu (I) compounds is the contribution of Cu 3d states near the VBM that, in contrast to the more common n-type metal oxides, could lead to smaller hole effective masses (value shown in **Table 1.1** for Cu_2O), and hence improved hole-transporting properties. Another promising candidate is stannous oxide SnO, in which the Sn 5s and O 2p hybridization in the VB also leads to good p-type conductivity.[57] Because of these essential characteristics, Cu_2O and SnO have found applications in thin-film transistors and logic circuits.[58, 59] Although the electronic band structures in many metal oxides should allow for charge transport, their significant band gaps generally prevent the thermal generation of carriers leading to low intrinsic carrier densities. Therefore, other mechanisms are needed to improve and explain their conductivity. For instance, it has been found experimentally that electrical conduction is generally associated with non-stoichiometry of metal oxide systems. As an example, conductivity in n-type metal oxides (In_2O_3, SnO_2, and ZnO) can be increased when the materials are grown under metal-rich/oxygen-deficient conditions. Oxygen vacancies (VO) and metal interstitials (Mi) are thus potential candidates for electron donors in these systems. Likewise, p-type conductivity is related to metal vacancies (VM) or oxygen interstitials (Oi). However, a complete description of the origin of conductivity would require: (1) thermodynamic considerations to determine whether any of these defects are stable under normal conditions; and, (2) electronic structure calculations to investigate whether the energy level of each defect is shallow enough to contribute to the conductivity.

Table 1.1: *Electronic properties of common metal oxide semiconductors [60]*

Oxide	Optical bandgap (eV)	Effective mass[a] (in units of free electron mass, m_o) Electron	Hole
n-Type			
ZnO	3.41	$m_e = 0.24$	$m_{h\perp} = 0.8$ $m_{h\parallel} = 5$
In_2O_3	3.38	$m_e = 0.3$	N/A
SnO_2	3.50	$m_{e\perp} = 0.30$ $m_{e\parallel} = 0.23$	$m_{h\perp} = 3.3$ $m_{h\parallel} = 2.3$
p-Type			
Cu_2O	2.17	$m_e = 0.99$	$m_{lh} = 0.58$
SnO	2.7[b]	N/A	N/A
CuSCN[c]	3.9[d]	$m_{e\perp} = 2$ $m_{e\parallel} = 1$	$m_{lh\perp} = 0.5$ $m_{lh\parallel} = 0.8$

For the most commonly discussed binary and ternary semiconducting metal oxides, namely In_2O_3, SnO_2, ZnO, IZO and IGZO metal (M) ns and oxygen (O) 2p orbitals contribute to the formation of CBM and VBM, respectively, giving rise to a highly dispersive CBM and, a localizing VBM.[60, 61] This leads to smaller effective masses for electrons, and therefore better electron transport in comparison to hole transport, i.e., the main reason for the predominantly n-type conductivity observed in the vast majority of metal oxide semiconductors reported to date. SnO_2 is quite different among these semiconductors, which generally works as an n-type semiconductor due to the oxygen vacancy. SnO_2 and SnO are the two phases of tin oxide, which generally work as an n-type and p-type semiconductor, respectively.[62] However, as per the earlier report, group IIIA elements work as an acceptor of SnO_2 semiconductor.[63] Out of these different group IIIA elements, such as In and Ga, have been theoretically predicted to introduce shallow acceptor with an activation energy of 580 and 760 meV, respectively.[64, 65] Besides, experimental reports also show that the

initial addition of In or Ga doping increases the resistance of the SnO_2 semiconductor by two orders of magnitude. During this period, conduction due to electron steeply decreases, and hole conduction introduces, which reaches the peak value for the highest level of doping (~$10^{17}/cm^2$).[64] However, after crossing the maximum level of doping concentration, resistivity rapidly decreases, and hole conduction disappears, which is due to the formation of In_2O_3 or Ga_2O_3 secondary phases in the SnO_2 thin film that works as a pure n-type semiconductor. **Figure 1.8** lists 15 post-transition metal elements with (n-l)$d^{10}ns^0$ (n≥4) configuration. Among them, Ag, Au, and Ge are expensive metals. Cd, Hg, Tl, Pb, and As are excluded from the AOS application due to their high toxicity. Cu^{+2} is used in a p-type semiconductor. In the oxide compounds of the remaining six elements, i.e., Zn, Ga, In, Sn are the most commonly used in AOS. Indium-based amorphous oxides, including IGZO and IZO, exhibit good electrical properties even with low-temperature processing.[66, 67]

11	12	13	14	15	
29 Cu 63.54	30 Zn 65.37	31 Ga 69.72	32 Ge 72.59	33 As 74.92	4
47 Ag 107.87	48 Cd 112.40	49 In 114.82	50 Sn 118.69	51 Sb 121.75	5
79 Au 196.97	80 Hg 200.59	81 Tl 204.37	82 Pb 207.19	83 Bi 208.98	6

Figure 1.8: *d block metal elements with (n-l)$d^{10}ns^0$(n≥4) configuration.[68]*

1.10 Graphene: A zero band gap semiconductor

Particular material properties should be considered when searching for new materials, which might constitute a choice for post-silicon electronics. The ideal semiconductor should have high mobility, tunable bandgap, capability for large-scale production, highly stable, low contact resistance, and interface matching with dielectrics.[69] Graphene, a two dimensional (2D) material arranged in a hexagonal lattice, is a good trade to meet these necessities. Graphene was invented by Andre Geim and Konstantin Novoselov in 2004 using the mechanical exfoliation method.[70] There are different types of methods to produce graphene, e.g., mechanical exfoliation, epitaxial growth on silicon carbide single crystal, chemical vapor deposition (CVD), self-assembly of soluble graphene, etc.. Still now, CVD is considered one of most efficient technique to produce large-area grapheme with defect state and good uniformity.[71] Unlike silicon, graphene is semi-metal having zero band gap. Contrasting unipolar Si MOSFETs, the charge carriers can be interchanged from electron to hole in a graphene channel just by altering the polarity of a gate voltage. However, in a real application, it is not quite easy because there are some impurities present in graphene during the growth process, and due to this, graphene either works as n-type or p-type in most of the cases.[72, 73] The conduction and valence bands meet each other in graphene, which is like a zero band gap semiconductor. The six points in the two-dimensional Brillouin zone where the bands meet are called Dirac points, as shown in **figure 1.9 a)**. Considering the band diagram in **figure 1.9 b)**, at the K points of the Brillouin zone, the valence band and conduction band meet and, unlike conventional bulk semiconductors, where the band's structure has a parabolic shape; they have linear energy-momentum dispersion close to the Dirac points. In this case, electrons imitate relativistic particles propagating via graphene

lattice and due to this Dirac-like equations will explain particle rather than Schrodinger equations.[74] Due to the lack of a band-gap, graphene transistors can not be switched off so easily and their Ion / Ioff ratios are not sufficient for electronics applications. The inability of switching devices often leads to high static power consumption, which is one of the biggest drawback of graphene transistor-based CMOS with respect to Si CMOS. However, there is a number of options to open a band gap of graphene, which can be achieved by restricting one dimension by forming graphene nanoribbons, biasing bilayer graphene, or adding a certain strain to the monolayer graphene.[75] Among these, biasing of bilayer graphene is one useful method to open its band gap for high-performance field-effect transistor applications.

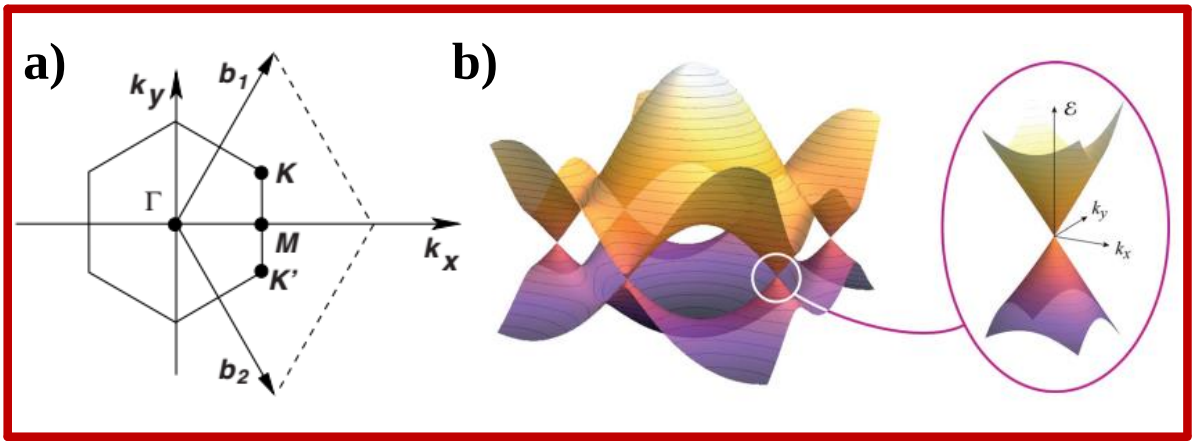

Figure 1.9: a) *First Brillouin zone and* ***b)*** *band structure of graphene with the linear dispersion around the K points.*[76, 77]

1.10.1 Mechanical property and carrier mobility of Graphene

Graphene has some unique features, which makes it a suitable candidate for different applications. Graphene has a young modulus, and tensile strength of ≈ 1 x 10^3 [78] and 130 Gpa[79], which is much higher than steel, and these properties are useful to make durable composites, bio-scaffolds, and hard coatings. The in-plane charge carrier mobility of graphene is as high as 2.5 x 10^5 cm^2 V^{-1} s^{-1}[74], which is much higher than Si and useful for high-speed transistors fabrication, transparent & flexible conductors, and conductive

composites applications. The specific surface area of graphene ≈ 2630 m^2/g[80], which is useful to fabricate light-weight and large area graphene-based electronics and optoelectronics devices.

1.10.2 Monolayer structural study of Graphene

Monolayer graphene is defined as a single two-dimensional hexagonal sheet of carbon atoms. However, graphene can be grown in a bilayer structure of a few layers structure that has up to 10 layers of such two-dimensional sheets. Graphene structures composed of more than 10 such layers are known as dense sheets of graphene and are of less scientific attention. The contrast spectra study is one most accessible way of differentiating few-layer graphene, which is commonly checked by optical microscopy on Si substrate with a 285 nm SiO_2 capping film.[81] However, the transmission electron microscopy (TEM) study gives direct evidence to recognize the graphene structure, as shown in **figure 1.10 a)**. Nevertheless, the TEM picture alone can not be sufficient due to its capability of small area study, which again depends on the destructive analytical technique. Careful analysis of local Raman spectra obtained from various portions of graphene that give a better idea of the graphene's thickness, as shown in **figure 1.10 b)**. There are three predominant peaks, i.e., D, G, and 2D peaks arise during Raman characterization of the graphene layer. D peak around 1350 cm^{-1} is referred to disordered carbon structure, G peak around 1580 cm^{-1} is related to the as graphitic structure or whiskers like carbon, and the 2D peak is referred to as the stacking order of graphene layers.[82] (with ref. discuss the variation of G and 2D peak with different monolayer).

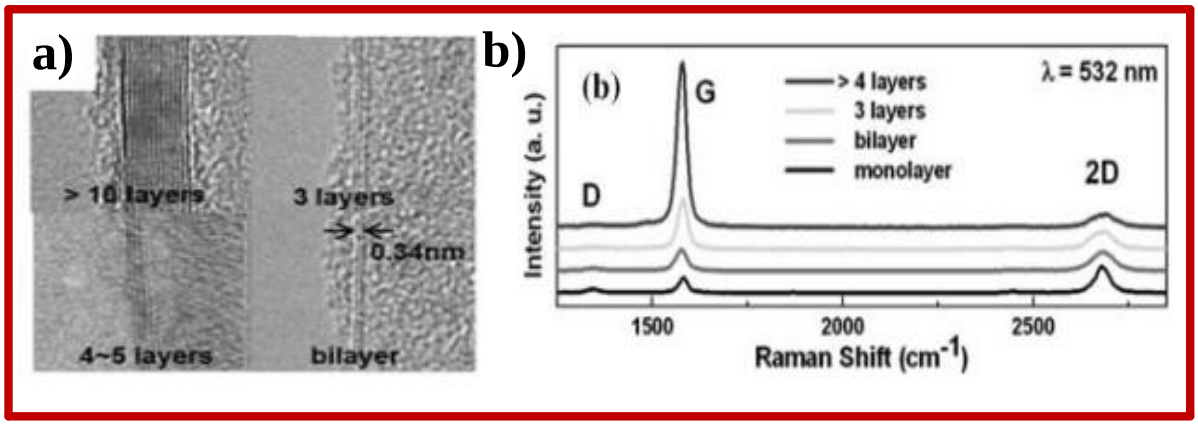

Figure 1.10: a) *TEM images of graphene films with different thicknesses,* ***b)*** *typical Raman spectra obtained from different thickness regions of graphene film (with an increasing number of layers from bottom to top).*[71]

1.11 A brief description of the development of solution-processed low operating voltage oxide TFT

As stated earlier, most vacuum-based techniques involve long processing periods to maintain a high vacuum environment, which needs a high preliminary set-up cost for instruments. Moreover, this vacuum-based deposition is capable of depositing thin film with a limited area based on the set-up. Because of these drawbacks, such methods are not ideal for low-cost deposition on a wide area of a substrate. Therefore, for low cost and large-area electronics applications, conventional vacuum-based deposition techniques can not be an efficient method and need an alternative to this method. Therefore, the development of solution-based printable material synthesis techniques, such as the sol-gel process, is urgently needed for low-cost mass production. The high-κ oxide, as well as AOSs thin films, can be deposited in numerous ways by sol-gel routes and subsequent deposition technique like spin coating, dip coating, spray pyrolysis, drop-casting, inkjet printing, screen printing, chemical bath deposition, doctor blade coating, aerosol jet, and various printing method.[83, 84] Every deposition method has its advantages and disadvantages, as well as ease of use, synthesis of

precursors, performance competence, roll-to-roll (R2R) suitability, etc. which has been summarized in **Table 1.2**.[85-87]

Table 1.2: *Comparison of film deposition techniques using printing and coating* [5]

Technique	**Spin**	**Spray**	**Bar**	**Ink-jet**	**Screen**	**Gravure**
Ink preparation	Simple	Moderate	Simple	Moderate	Demanding	Difficult
Ink waste	Significant	Considerable	Little	None	None	Significant
Speed	–	Fast	Medium	Medium	Fast	Very fast
Noncontact processability	Yes	Yes	No	Yes	Yes	No
R2R compatible	No	Yes	Yes	Yes	Yes	Yes

1.11.1 Sol-gel synthesis method

Spin Coating

Due to the low cost and simplicity of processing, the spin coating was widely used to fabricate oxide dielectrics. To achieve thin and highly uniform film, in this process, drops of precursor solution are allotted on a hydrophilic substrate and, after that, accelerated to high angular velocities, i.e. (hundreds to thousands of rpm). In the last two decades, different types of oxide dielectric have been synthesized by this method.

Innovative work was reported by Keszler et al., who incorporated sulfate/phosphate derivatives of AlPO, HfSOx, and ZrSOx dielectrics into TFTs with sputtered oxide semiconductors.[21] The synthesized dielectrics film is atomically dense, showing reasonable κ values (4.8–12) with high breakdown voltage and low leakage current. A large

number of studies have subsequently been published on the spin-coated binary MOx (M:Li, Al, Zr, Hf, Y, Mg, etc.)[88-96] However binary high κ oxides suffer from a compromise between Eg and κ, which troubles to select material with both high Eg and large κ. Binary oxides, even at low processing temperatures, often appear to crystallize, which produces grain boundaries limits leading to impurities, high leakage current, and interdiffusion.

There have been numerous promising approaches to deal with such problems and accomplish multilayered dielectric integrating large Eg and high κ into the same dielectric. Katz et al. developed a novel dielectric film named sodium beta alumina, which has large Eg (8.8 eV) and very high κ (170).[29] Zinc tin oxide (ZTO) was used as a channel layer, and they got on/off ratio around 10^4 and mobility 28 cm^2 V^{-1} s^{-1}. The authors further fabricated for the first time on an ITO glass substrate based all solution-processed transparent oxide transistors that could work at low operating Voltages.

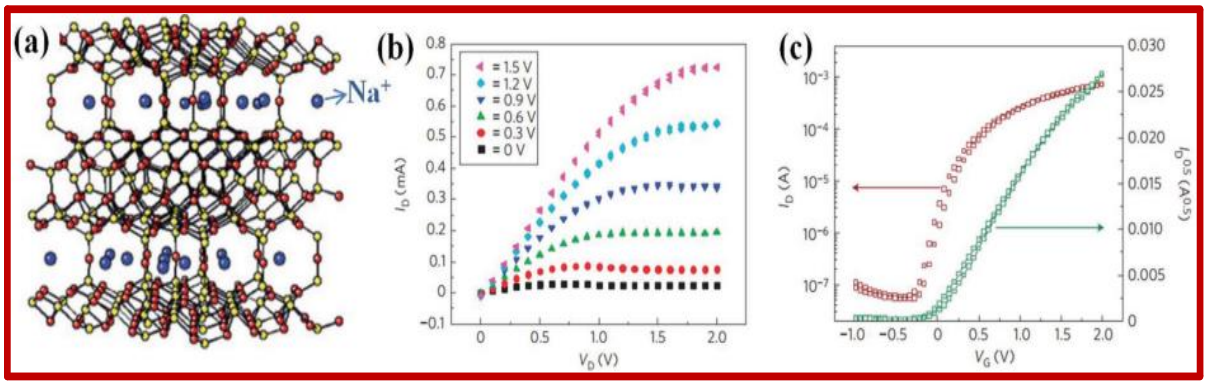

Figure 1.11: *Solution-processed ion-conducting metal oxide thin film transistor* ***a)*** *crystal structure of SBA dielectric* Na^+ *ion is denoted by a blue dot, and red and yellow color represents oxygen and aluminum atoms respectively* ***b)*** *output and* ***c)*** *transfer characteristics of ZTO transistor with sol-gel coated SBA dielectric based TFT.*

Apart from this, spin-coated high κ oxide dielectric is also useful in different types of devices composed of semiconductor colloidal nanocrystals, 2D transition metal dichalcogenides, and single-wall carbon nanotubes. Talphin et al. replaced conventional dielectric SiO_2 with high κ

oxide dielectric ZrOx. They demonstrated CdSe NC based transistor with a very high mobility 450 $cm^2 V^{-1} s^{-1,}$ which is much greater than SiO_2 based TFT device.

Recently Pal et al. developed different types of ion-conducting dielectric for low voltage thin film transistor and phototransistor application. They reported Li_5AlO_4[97], $LiAlO_2$[98], Li_2ZnO_2[99] class of ion-conducting dielectrics, and fabricated TFT has operating voltage <2 V, high Ion/Ioff ratio and low leakage current density.

1.11.2 Spray pyrolysis method

Like spin coating, spray pyrolysis is another simple, low-cost coating method that is also consistent with the large area deposition on different substrates. Usually, films are created by aerosol spray solutions on preheated substrates, where ingredients go through a chemical reaction. The distinctive feature of this method is that irregular structures can be fabricated, e.g., stacks, steps, and trenches. The quantity of raw material used for sprays was revealed to be four times lower than the spin coating needed. However, there needs to be low viscosity of a precursor solution for nebulization, which limits the selection of appropriate solvents. Additionally, spray pyrolyzed film roughness is usually lower than that of spin-coated samples, and the heating of the substrates must be carefully managed.

Anthopoulos et al., who published a sequence of works about high-performance oxide TFTs and circuits using a spray pyrolysis method, achieved the milestone in this field.[100-105] They have prepared polycrystalline ZrO_2 dielectric by this method. The thin film prepared by spray pyrolysis has high κ (=14), high Eg (5.9 eV), low leakage current density J_{leak} < 0.5 µA cm^{-2} at operating voltage of 6 V, and high breakdown voltage ≈ 1.6 MV cm^{-1}. The fabricated TFT with spray pyrolyzed based Li: ZnO and ZrO_2 dielectric shows excellent TFT

characteristics like Ion/Ioff ratio ≈ 10^6, very high mobility 450 cm^2 V^{-1} $s^{-1,}$ and small hysteresis.[101] In subsequent studies, Y_2O_3[106], HfO_2[46], and $LaAlO_3$[107] dielectrics were synthesized using spray pyrolysis, and oxide TFT applications were investigated. Such findings illustrate the broad potential of spray pyrolysis for transparent oxide electronics fabricated over a wide area and at a low cost.

1.11.3 Screen Printing method

Digital printing technology has achieved rapid prototyping for different electronics, which has profoundly modified our ideas on how to produce electronic devices.[108, 109] In this method, the oxide material may be deposited locally, thereby considerably minimizing wasted material and preventing subsequent patterning. The techniques that are used most, such as inkjet, screen, gravure, etc. are now being used for the fabrication of oxide thin films and TFTs. For each printing technology requires different parameters for the ink and provides various thickness and resolutions. The literature was very obvious that the important thing is parameters of printing include accuracy, resolution, precision, uniformity, and ink compatibility with the components of printing, and target substrate wettability.[110] However, in order to avoid irregularities and effects, conditions of drying ink need carefully monitored due to patterned deposition.

Subramanian et al. conducted pioneering work and presented a comprehensive family of printable metal oxide inks, together with SnO_2 semiconductors, Sb doped SnO_2 electrodes, and ZrO_2 dielectric.[111] They established a technology using PMMA layers as fugitive wettability switches to control the surface energy and minimize “coffee ring” effects during inkjet printing. The fabricated ZrO_2 dielectric has a high dielectric constant $\kappa = 23$ and low leakage current density $J_{leak} \approx 10^{-5}$ A cm^{-2} at 1 MV cm^{-1}. The thickness of the film is around

40 μm and the processing temperature of 500 ^{o}C. The fabricated TFT based on the glass substrate by a fully inkjet printing process showed mobility of μ_{FE} = 11 cm^2 V^{-1} s^{-1}, high on/off ratio (Ion/Ioff = 10^6) and low operating voltage (> 5 V).

Recently Li et al. fabricated fully inkjet-printed oxide TFT array by developing a new surface energy pattern method.[111] Employing oxygen plasma treatment and solvent etching, ink blowout, and surface topology of the deposited film were successfully controlled. The annealing temperature of printed ZrO_2 dielectric is 450 ^{o}C, having an amorphous phase with capacitance value 3.3 nF cm^{-2} at 1 kHz frequency and dielectric constant κ = 15.4. The dielectric has leakage current density $J_{leak} \approx 10^{-7}$ A cm^{-2} at 1 MV cm^{-1}. The fabricated device (ITO/InGaO/ZrOx/ITO) by a fully inkjet-printed method showed mobility of μ_{FE} = 7.5 cm^2 V^{-1} s^{-1}, on/off ratio (Ion/Ioff >10^7), and negligible hysteresis. In addition to these notable achievements, several other studies have been investigated using printing techniques to the synthesis of solutions processed TFTs with high oxide dielectrics.

1.12 Scope and objective of present work

Metal-oxide TFT has been widely considered for different applications, including active-matrix light-emitting diodes (AMLEDs), light-emitting transistors, photodetectors, biosensors arrays, etc., due to their outstanding transport properties. These metal oxide TFTs validate reasonably high on/off ratio, high mobility, superb chemical, and thermal constancy, which are the fundamental necessities for practical applications. Though, because of the low dielectric constant (κ) of SiO_2 gate dielectric, TFTs need high operating voltages (≥40V), which is typically used for metal oxide TFT, restrictive its application to portable low power electronics. In addition, the high polarization behavior of dielectric, especially the binary oxide dielectric and their thin-film, have been thoroughly studied as gate dielectric materials

in the thin film transistor that provide low energy consumption. To this extent, Pal et al. first established an innovative approach to developing dielectric material with improved 'κ' value afterward incorporating ionic dopants into oxide lattices. Sodium beta alumina (SBA) is the first ion-conducting dielectric that successfully used as a gate insulator in low voltage TFTs.[29] However, in literature, dielectric behavior in TFT and the effect of lithium-ion in metal oxides are relatively uncommon. We introduce here three new Li^+ containing ion-conducting insulators and successfully used as a gate dielectric in low voltage TFT. These dielectrics showed crystalline nature at lesser processing temperature and exhibited higher performance of TFTs. Hence, the key objective of the current thesis is to synthesize the ion-conducting dielectric using a cost-effective sol-gel process. Moreover, using ion-conducting dielectric efforts have been given to develop balanced ambipolar TFT at a low operating voltage, which is useful for CMOS electronics. In addition, a unique attempt has been taken to develop low operating voltage and large area graphene TFT using ionic gate dielectric. This graphene TFT has been used for low bias chemical gas sensors. Therefore, the thesis is divided into the key objectives comprising these chapters on the basis of the above discussion given in this chapter:

Chapter 2 addresses dielectric and semiconductor synthesis via the cost-effective solution process technique. The thin film of dielectric and semiconductor is fabricated by spin coater and used as a gate dielectric in TFTs. Furthermore, the materials and device characterization procedures are clarified in this chapter.

Chapter 3 describes the synthesis of Li_2ZnO_2 by a solution-processed method and its application as a gate dielectric of a metal-oxide TFT. The high dielectric constant (κ) of Li_2ZnO_2 has been accomplished by employing the better capacitance contributed by the

mobile lithium-ion (Li^+) within the dielectric film. This lower band gap Li_2ZnO_2 is a well-known material for solid-state electrolyte application, has never been considered previously as a gate dielectric of metal-oxide thin-film transistor (TFT). We have synthesized this dielectric by low-cost sol-gel method followed by a low-temperature annealing process 500 ^oC, having hexagonal structure. The TFTs fabricated with Li_5AlO_4 on top of highly doped silicon (p^+-Si) substrate and a solution-processed semiconducting layer of tin oxide (SnO_2) as a channel layer which shows an excellent TFT performance at the operating voltage of 2V. The TFT shows an on/off ratio of 7 x 10^3 and an electron mobility of 23 $cm^2\ V^{-1}\ s^{-1}$. In addition, this device requires a least drain voltage of < 2V to reach the saturation drain current due to higher Li^+ mobility of α-Li_5AlO_4 gate dielectric. This TFT performance on the p^+-Si substrate is also compared with Li_2O gate dielectric, which suggests that Li_2ZnO_2 dielectric is superior to that of the previously reported device with sodium beta-alumina (SBA) gate dielectric. Moreover, this dielectric requires ~300 ^oC lower processing temperatures compared to SBA dielectric.

In chapter 4, we describe the sol-gel synthesis of ion-conducting $LiInO_2$ and $LiGaO_2$ insulator, which are used as a gate dielectric for ultra-low voltage (≤ 1V) of tin oxide (SnO_2) ambipolar thin film transistor (TFT). Metal oxide semiconductors are commonly n-type in nature. However, SnO_2 can show ambipolar nature, in case it's doped in a proper way. In our thesis work, a p-doped SnO_2 channel semiconductor has been fabricated by utilizing dielectric/semiconductor interface doping. To introduce this interfacial-doping, a bottom-gate top-contact TFTs have been fabricated by using two different ion-conducting oxide dielectrics which contain trivalent atoms like indium (In) and gallium (Ga). These ion-conducting dielectrics are $LiInO_2$ and $LiGaO_2$, respectively, containing mobile Li^+ ion.

During SnO_2 thin film fabrication on top of those ionic dielectrics, the trivalent atoms allow p-doping to the dielectric/semiconductor interfacial SnO_2 layer to introduce the 'hole' conduction in the channel of TFT. Our comparative electrical data indicates that TFTs with $LiInO_2$ and $LiGaO_2$ dielectric is ambipolar in nature. Most interestingly, by using $LiInO_2$ dielectric, we are capable to fabricate 1V balanced ambipolar TFT with a high electron and hole mobility values of 7 $cm^2 V^{-1} s^{-1}$and 8 $cm^2 V^{-1} s^{-1}$ respectively with an on/off ratio $>10^2$ for both operations which has been utilized for low-voltage CMOS inverter fabrication.

In chapter 5, a new technique of high-performance large channel length graphene field-effect transistors (GFFTs) fabrication has been described by using the Li_5AlO_4 ion-conducting gate dielectric. In our thesis work, we have fabricated large channel length (up to 5.7 mm) GFETs through a simple, cost-effective method that required thermally evaporated source-drain electrode deposition, which is less cumbersome from the conventional wet-chemistry based photolithography. The semiconducting nature of graphene has been achieved by utilizing the Li^+ ion of Li_5AlO_4 gate dielectric, which shows current saturation at a low operating voltage (~2V). The length scaling of these GFETs has been studied with channel length variation within a range from 0.2 mm to 5.7 mm. It is observed that the GFET of 1.65 mm channel length shows optimum device performance with good current saturation. This particular GFET shows the 'hole' mobility of 312 $cm^2 V^{-1} s^{-1}$ with on/off ratio 3. For comparison, GFET has been fabricated in the same geometry by using conventional SiO_2 dielectric that doesn't show any gate-dependent transport property, which indicates the superior effect of Li^+ of the ionic gate dielectric on current saturation.

Chapter 6 deals with large channel length graphene field-effect transistors (GFETs) for the detection of ammonia gas in the presence of an ambient atmosphere. For an application as

chemical gas sensor, our developed large-area graphene FFT, we have fabricated a GFET with a large channel length of 450 µm. The device characteristics are shown excellent low operation behavior within 2V, which is paving the path for portable TFT based chemical gas sensors. The fabricated device has also been tested for very low concentration ammonia under ambient environment conditions at 25 ºC temperature, which shows the enormous potential for ammonia sensing for real-life applications. The average response time and recovery time of this GFET based sensor is ~40 sec and ~120 sec, respectively. A significant change in the Dirac point variation from 1.4V to 0.7V indicates its high sensitivity in the ammonium atmosphere.

Finally, chapter 7 is dedicated to sum up the major findings of the thesis. At last, the future possibilities of works related to the present thesis have been briefly outlined.