List of Tables

| Table | Caption | Page no. |
|-------|--|-------------|
| 2.1 | Switching States for Voltage Level Synthesis | 29 |
| 2.2 | Constraints of MPSO, PSO and GA | 40 |
| 2.3 | %THD Comparison for Different Algorithms | 40 |
| 2.4 | Conditional Switching States for Capacitor Voltage Balance | 44 |
| 2.5 | Capacitance Values at Different m_a | 54 |
| 2.6 | Parameters Used for Simulation | 54 |
| 2.7 | Components Used for Experiment | 63 |
| 2.8 | Harmonic Magnitudes and % THD of <i>V</i> _{AB} Through Experiment at Different Modulation Indices | 67 |
| 2.9 | Harmonic Magnitudes and %THD of Line Voltage V_{AB} at Different Modulation Indices | 67 |
| 2.10 | Experimental %THD Comparison of Different Algorithms | 67 |
| 3.1 | Parameters of MWO, WO, GA and PSO | 83 |
| 3.2 | Experimental %THD Comparison of Different Algorithms | 91 |
| 4.1 | Parameters of MGWO, GWO, GA and PSO | 104 |
| 4.2 | Comparison between GWO and MGWO | 110 |
| 4.3 | Comparison of % THD Among Proposed MPSO, MWO and | 111 |
| | MGWO | |
| 4.4 | Performance comparison of MGWO, MWO and MPSO | 111 |
| 5.1 | Switching Patterns, Diode behaviour of Capacitor States at Each Voltage Level | 116 |
| 5.2 | PIV across Switches for 17-level DASC-MLI | 121 |
| 5.3 | Largest Discharge Interval for capacitor (C_1) | 124 |
| 5.4 | Comparison of proposed 17-level DASC-MLI with Other Recent SC-MLI Topologies | 131 |
| 5.5 | Devices and Parameters Used for Experimentation | 137 |
| 6.1 | Switching Patterns and States of Capacitors of the Proposed 17- level RVSC-MLI | 147 |
| 6.2 | Maximum Blocking Voltage Across Switches of 17-level RV- SCMLI | 152 |
| 6.3 | Comparison of proposed 17-level RVSC-MLI with Reported 17- level SC-MLI Topologies | 159 |
| 6.4 | Devices and Parameters Used for Experimentation | 165 |