Chapter 6

A 17-Level Reduced Voltage Stress Switched Capacitor Multilevel Inverter

6.1 Introduction

In this chapter, a new 17-level reduced voltage switched-capacitor MLI (RVSC-MLI) is proposed. The peak inverse voltage (PIV) of the switches and diodes are within the input DC source voltage level in RVSC-MLI. The proposed RVSC-MLI can generate 17-level output voltage using a single DC voltage source with lesser number of circuit components. The TSV of the proposed RVSC-MLI is comparatively lower than existing SC-MLIs and diode assisted switched-capacitor MLI (DASC-MLI), which makes it suitable for higher voltage applications with low rated power devices. Higher voltage levels (more than 17-levels) can also be achieved using the extended structure of the proposed RVSC-MLI with only one DC voltage source. The output voltage of the proposed RVSC-MLI is more than the input voltage, which signifies its boosting capability. A voltage gain of two can be achieved using the proposed RVSC-MLI and the voltage gain can be further increased using the extended structure of it. In the proposed RVSC-MLI, the capacitors are periodically charged and discharged without using any voltage balancing mechanism.

6.2 Proposed Reduced Voltage Stress Switched-Capacitor MLI

The circuit configuration of the proposed RVSC-MLI is shown in Fig 6.1. It consists of thirteen unidirectional switches (S_1-S_5), (T_1-T_4), (Q_A-Q_D); four bidirectional switches (S_a-S_d); four diodes (D_A-D_D) and two floating capacitors (C_A and C_B). The PIV across all

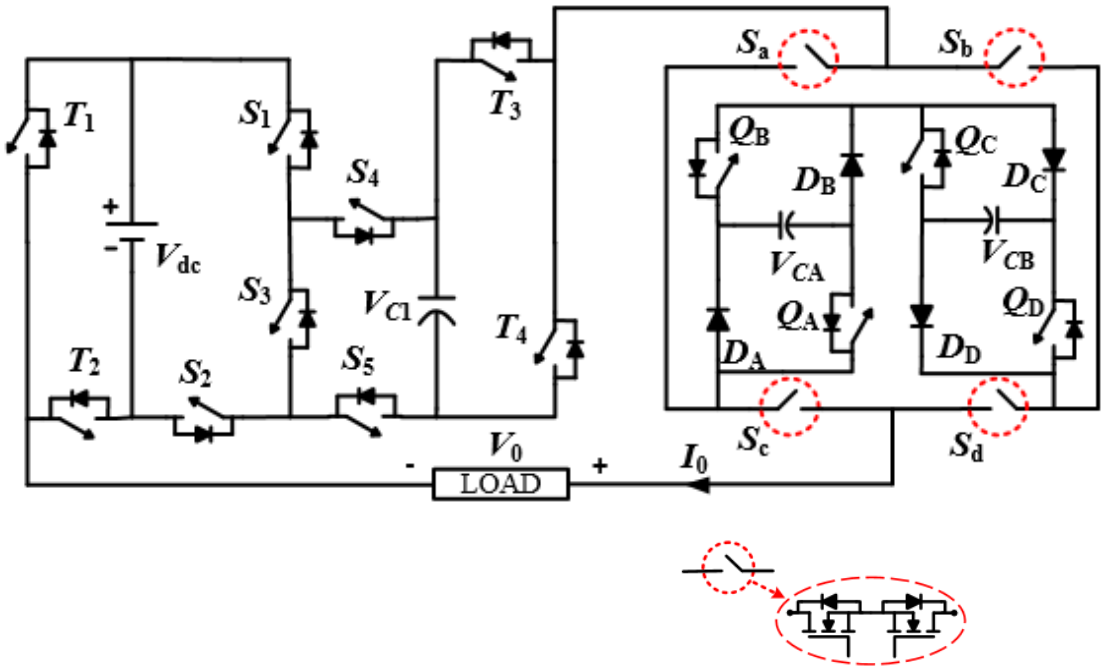


Fig. 6.1 Circuit configuration of the proposed 17-level RVSC-MLI.

switches and diodes are within supply voltage V_{dc} in the proposed RVSC-MLI. Different voltage levels can be generated by series and parallel combinations of voltage source and capacitors in the proposed circuit.

6.3 Generation of Voltage Levels

The switching patterns of different voltage levels for (left and right half) of both half cycles of the proposed 17-level RVSC-MLI are given in Table 6.1. The current path for different left half of positive voltage levels are shown in Fig. 6.2(a)-(i). In these figures, the blue colour indicates the current flowing path in the circuit. It can be observed from Table 6.1 that to maintain the voltages of the floating capacitors C_A and C_B at $V_{dc}/2$ and $V_{dc}/4$ respectively, their charging and discharging time intervals are kept identical. To verify the charge balance of capacitors C_A and C_B, the net charge Q_A and Q_B for a complete cycle are given as ($< >$ represents average current flowing through the capacitors for load impedance Z)

$$Q_A = \left[\langle i^{+L}_{C_A,\frac{V_{dc}}{4}}\rangle - \langle i^{+L}_{C_A,\frac{V_{dc}}{2}}\rangle + \langle i^{+L}_{C_A,\frac{3V_{dc}}{4}}\rangle - \langle i^{+L}_{C_A,\frac{5V_{dc}}{4}}\rangle + \langle i^{+L}_{C_A,\frac{3V_{dc}}{2}}\rangle - \langle i^{+L}_{C_A,\frac{7V_{dc}}{4}}\rangle + \right.$$

$$\langle i^{+R}_{C_A,\frac{3V_{dc}}{2}}\rangle - \langle i^{+R}_{C_A,\frac{V_{dc}}{2}}\rangle - \langle i^{-L}_{C_A,\frac{V_{dc}}{4}}\rangle + \langle i^{-L}_{C_A,\frac{V_{dc}}{2}}\rangle - \langle i^{-L}_{C_A,\frac{3V_{dc}}{4}}\rangle + \langle i^{-L}_{C_A,\frac{5V_{dc}}{4}}\rangle - \langle i^{-L}_{C_A,\frac{3V_{dc}}{2}}\rangle +$$

$$\left.\langle i^{-L}_{C_A,\frac{7V_{dc}}{4}}\rangle - \langle i^{-R}_{C_A,\frac{3V_{dc}}{2}}\rangle + \langle i^{-R}_{C_A,\frac{V_{dc}}{2}}\rangle\right] \cdot T$$

$$= \frac{1}{Z}\{(V_{dc} - V_{C_A} - V_{dc}/4) - V_{C_A} + (V_{dc} - V_{C_A} + V_{dc}/4) - (V_{dc} + V_{C_A} - V_{dc}/4) +$$

$$(2V_{dc} - V_{C_A}) - (V_{dc} + V_{C_A} + V_{dc}/4) + (2V_{dc} - V_{C_A}) - V_{C_A} - (V_{C_A} - V_{dc}/4) +$$

$$(V_{dc} - V_{C_A}) - (V_{C_A} + V_{dc}/4) + (2V_{dc} - V_{C_A} - V_{dc}/4) - (V_{dc} + V_{C_A}) + (2V_{dc} -$$

$$V_{C_A} + V_{dc}/4) - (V_{dc} + V_{C_A}) + (V_{dc} - V_{C_A})\}$$

$$= 8V_{dc} - 16V_{dc} \qquad (6.1)$$

$$Q_B = \left[\langle i^{+L}_{C_B,\frac{V_{dc}}{4}}\rangle - \langle i^{+L}_{C_B,\frac{3V_{dc}}{4}}\rangle + \langle i^{+L}_{C_B,\frac{5V_{dc}}{4}}\rangle - \langle i^{+L}_{C_B,\frac{7V_{dc}}{4}}\rangle + \langle i^{+R}_{C_B,\frac{7V_{dc}}{4}}\rangle - \langle i^{+R}_{C_B,\frac{5V_{dc}}{4}}\rangle \right.$$

$$+ \langle i^{+R}_{C_B,\frac{3V_{dc}}{4}}\rangle - \langle i^{+R}_{C_B,\frac{V_{dc}}{4}}\rangle + \langle i^{-L}_{C_B,\frac{V_{dc}}{4}}\rangle - \langle i^{-L}_{C_B,\frac{3V_{dc}}{4}}\rangle + \langle i^{-L}_{C_B,\frac{5V_{dc}}{4}}\rangle - \langle i^{-L}_{C_B,\frac{7V_{dc}}{4}}\rangle$$

$$\left. + \langle i^{-R}_{C_B,\frac{7V_{dc}}{4}}\rangle - \langle i^{-R}_{C_B,\frac{5V_{dc}}{4}}\rangle + \langle i^{-R}_{C_B,\frac{3V_{dc}}{4}}\rangle - \langle i^{-R}_{C_B,\frac{V_{dc}}{4}}\rangle\right] \cdot T$$

$$= \frac{1}{Z}\{(V_{dc} - V_{C_B} - V_{dc}/2) - (V_{dc} + V_{C_B} - V_{dc}/2) + (V_{dc} - V_{C_B} + V_{dc}/2) - (V_{dc} +$$

$$V_{C_B} + V_{dc}/2) + (2V_{dc} - V_{C_B}) + (V_{dc} - V_{C_B}) - V_{C_B} + (V_{dc}/2 - V_{C_B}) - (V_{C_B} +$$

$$V_{dc}/2) + (V_{dc} - V_{C_B}) + (2V_{dc} - V_{C_B} - V_{dc}/2) - (2V_{dc} + V_{C_B} - V_{dc}/2) + (2V_{dc} -$$

$$V_{C_B}) - (V_{dc} + V_{C_B}) + (V_{dc} - V_{C_B}) - V_{C_B}\}$$

$$= 4V_{dc} - 16V_{C_B} \qquad (6.2)$$

where $i^{+L}_{C_{A(B)},v_0}$, $i^{+R}_{C_{A(B)},v_0}$ are the currents through $C_{A(B)}$ in left and right half of positive

voltage level v_0, $i_{C_{A(B)},v_0}^{-L}$, $i_{C_{A(B)},v_0}^{-R}$ are the currents through $C_{A(B)}$ in left and right half of negative voltage level v_0, and T is the total time period of the output voltage.

At steady state, due to the symmetric nature of the output current and considering $Q_A = 0$ and $Q_B = 0$ in (6.1) and (6.2), it can be observed that the voltage across C_A and C_B are $V_{dc}/2$ and $V_{dc}/4$ respectively. As the capacitors are self-balanced and do not require additional circuit, the overall size, cost and complexity of the RVSC-MLI reduces.

The different voltage levels (left half) of positive half cycle are achieved in the proposed 17-level RVSC-MLI through Table 6.1 and Fig. 6.2 are given as

Level zero: Fig. 6.2(a) shows the circuit configuration of the zero-voltage level. It is achieved using switches T_2, S_2, S_3, S_4, T_3, S_a, Q_A, Q_C, S_d and diodes D_B, D_D.

Level $+V_{dc}/4$: Fig. 6.2(b) shows the circuit configuration of voltage level $+V_{dc}/4$. The voltage source V_{dc} charges the capacitors C_1 through the switches S_1, diodes of S_4, S_5 and S_2. The capacitor C_A charges through the diodes D_A and D_B, whereas C_B charges through diodes D_C and D_D. The switches T_2, T_3, S_a, S_d ensure positive voltage level across the load. The voltage of $+V_{dc}/4$ is obtained as ($+V_{dc}$ - $V_{dc}/2$ - $V_{dc}/4$).

Level $+V_{dc}/2$: Fig. Fig. 6.1(c) shows the circuit configuration of voltage level $+V_{dc}/2$. The capacitor C_A feeds the load to achieve the voltage level and it discharges through the switches Q_A and Q_B. The capacitor C_B is bypassed through the switch Q_C and diode D_D. The capacitor C_1 remains unaffected while the current flows using switches S_2, S_3 and S_4.

Level $+3V_{dc}/4$: Fig. 6.2(d) shows the circuit configuration for generation of voltage level $+3V_{dc}/4$. The voltage source V_{dc} charges the capacitors C_1 and C_A (as explained in level $V_{dc}/4$). The capacitor C_B discharges through the switches Q_C and Q_D. The voltage level $+3V_{dc}/4$ is obtained as (V_{dc} - $V_{dc}/2$ + $V_{dc}/4$).

Table 6.1
Switching Patterns and States of Capacitors of the Proposed 17-level RVSC-MLI

Output voltage levels	Switches	Capacitor states		
		C_1	C_A	C_B
$+2V_{dc}$	T_2, S_1, S_3, S_5, T_3, S_a, Q_A, Q_C, S_d	D	U	U
(+L) $+7V_{dc}/4$	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, Q_B, Q_C, Q_D, S_d	C	D	D
(+R)	T_2, S_1, S_3, S_5, T_3, S_a, Q_A, S_d	D	U	C
$+3V_{dc}/2$	T_2, S_1, S_3, S_5, T_3, S_a, Q_C, S_d	D	C	U
(+L) $+5V_{dc}/4$	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, Q_B, S_d	C	D	C
(+R)	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, Q_C, Q_D, S_d	C	U	D
$+V_{dc}$	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, Q_C, S_d	C	U	U
(+L) $+3V_{dc}/4$	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_C, Q_D, S_d	C	C	D
(+R)	T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, S_d	C	U	C
$+V_{dc}/2$	T_2, S_2, S_3, S_4, T_3, S_a, Q_A, Q_B, Q_C, S_d	U	D	U
(+L) $+V_{dc}/4$	T_2, S_1, S_4, S_2, S_5, T_3, S_a, S_d	C	C	C
(+R)	T_2, S_2, S_3, S_4, T_3, S_a, Q_A, Q_C, Q_D, S_d	U	U	D
0	T_2, S_2, S_3, S_4, T_3, S_a, Q_A, Q_C, S_d	U	U	U

Output voltage levels	Switches	Capacitor states		
		C_1	C_A	C_B
$-2V_{dc}$	S_c, Q_B, Q_D, S_b, T_4, S_4, S_3, S_2, T_1	D	U	U
(-L) $-7V_{dc}/4$	S_c, Q_C, Q_D, S_b, T_4, S_4, S_3, S_2, T_1	D	C	D
(-R)	S_c, Q_A, S_b, T_4, S_4, S_3, S_2, T_1	D	U	C
$-3V_{dc}/2$	S_c, Q_A, Q_B, Q_C, S_b, T_4, S_1, S_4, S_5, S_2, T_1	C	D	U
(-L) $-5V_{dc}/4$	S_c, S_b, T_4, S_4, S_3, S_2, T_1	D	C	C
(-R)	S_c, Q_A, Q_C, Q_D, S_b, T_4, S_5, S_2, S_1, S_4, T_1	C	U	D
$-V_{dc}$	S_c, Q_B, Q_D, S_b, T_4, S_5, S_2, S_1, S_4, T_1	C	U	U
(-L) $-3V_{dc}/4$	S_c, Q_A, Q_B, Q_C, Q_D, S_b, T_4, S_5, S_3, S_1, T_1	U	D	D
(-R)	S_c, Q_A, S_b, T_4, S_5, S_2, S_1, S_4, T_1	C	U	C
$-V_{dc}/2$	S_c, Q_C, S_b, T_4, S_5, S_2, S_1, S_4, T_1	C	C	U
(-L) $-V_{dc}/4$	S_c, Q_A, Q_B, S_b, T_4, S_5, S_3, S_1, T_1	U	D	C
(-R)	S_c, Q_A, Q_C, Q_D, S_b, T_4, S_5, S_3, S_1, T_1	U	U	D
0	S_c, Q_B, Q_D, S_b, T_3, S_4, S_1, T_1	U	U	U

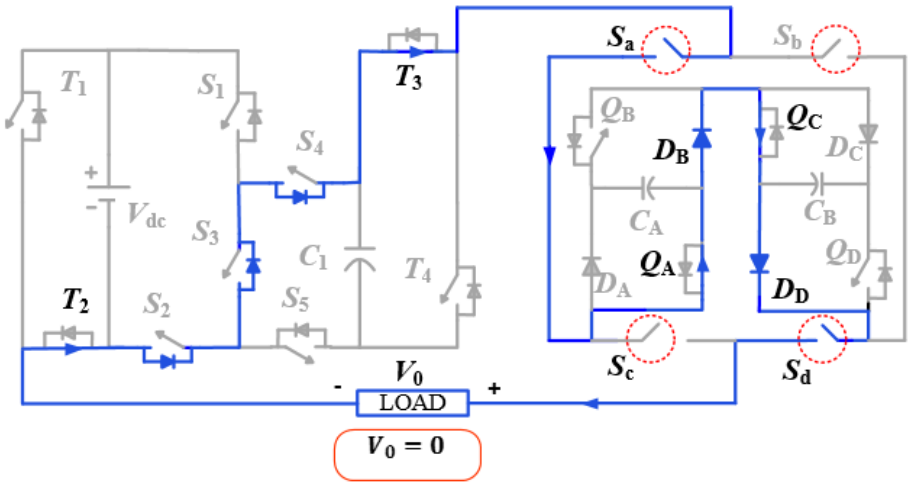
The column ON Switches represents the switches carrying load current. The capacitor states C is for charging, D for discharging, and U for unchanged. +L, +R are left and right half voltage levels of positive half cycle; -L, -R are left and right half voltage levels of negative half cycle.

Level $+V_{dc}$: Fig. 6.2(e) shows the circuit configuration of voltage level $+V_{dc}$. The voltage source feeds the load directly without involving any capacitor to generate the voltage level. C_1 is charged in this interval (as explained in level $V_{dc}/4$). The capacitors C_A and C_B remain unaffected and are bypassed through switches Q_A, Q_C and diodes D_B, D_D.

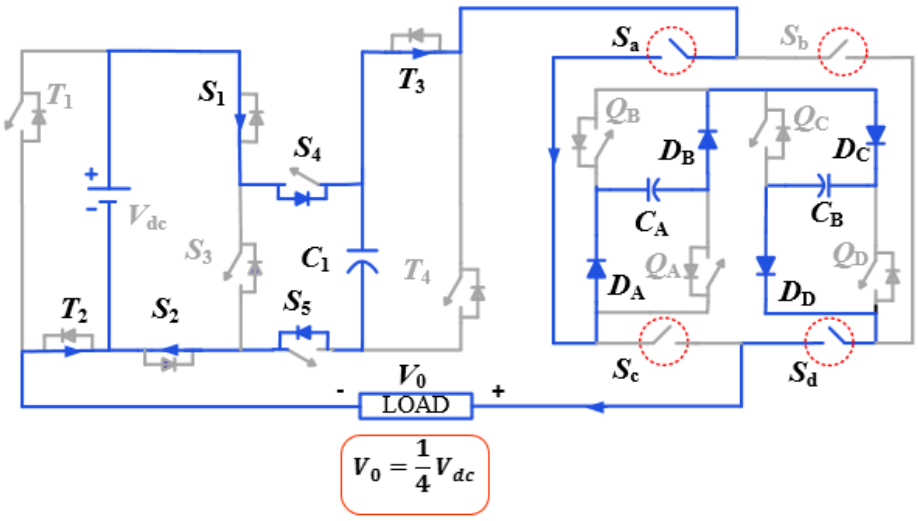
Level $+5V_{dc}/4$: Fig. 6.2(f) shows the circuit configuration for generation of voltage level $+5V_{dc}/4$. The switches T_2, S_1, S_4, S_2, S_5, T_3, S_a, Q_A, Q_B and S_d are turned on in this interval. The capacitors C_1 and C_B get charged in this interval. The capacitor C_A discharges through the switches Q_A and Q_B.

Level +3V_{dc}/2: Fig. 6.2(g) shows the circuit configuration of voltage level +3V_{dc}/2. The switches T_2, S_1, S_3, S_5, T_3, S_a, Q_C and S_d are turned on in this interval. The capacitors C_A get charged through the charging loop. The capacitor C_1 discharges in this interval through switches S_1, S_3 and S_5. The capacitor C_B remain unaffected and are bypassed through switches Q_A, Q_C and diodes D_B, D_D.

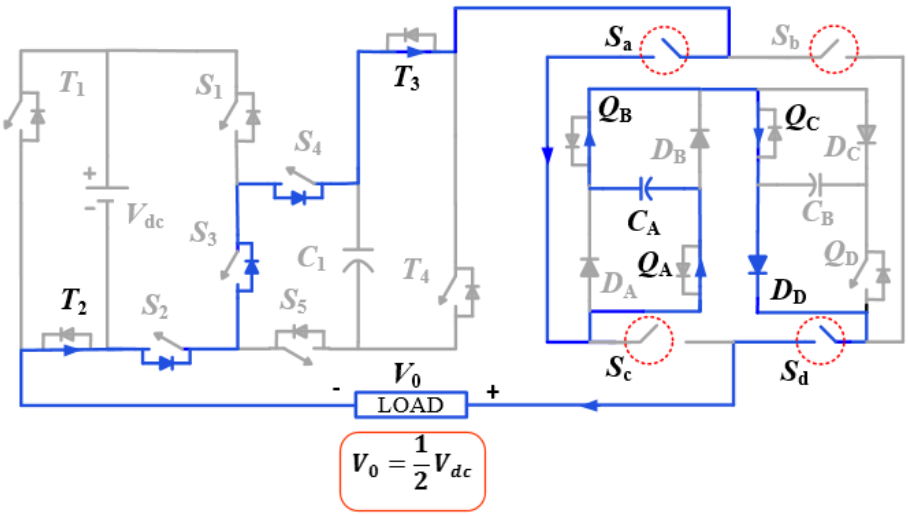
Level +7V_{dc}/4: Fig. 6.2(h) shows the circuit configuration for generation of voltage level +7V_{dc}/4. The voltage source V_{dc} charges the capacitors C_1 (as explained in level V_{dc}/4). The capacitor C_A and C_B discharges through the switches Q_A, Q_B, Q_C and Q_D. The voltage level +7V_{dc}/4 is obtained as (V_{dc} +V_{dc}/2 + V_{dc}/4).



(a)

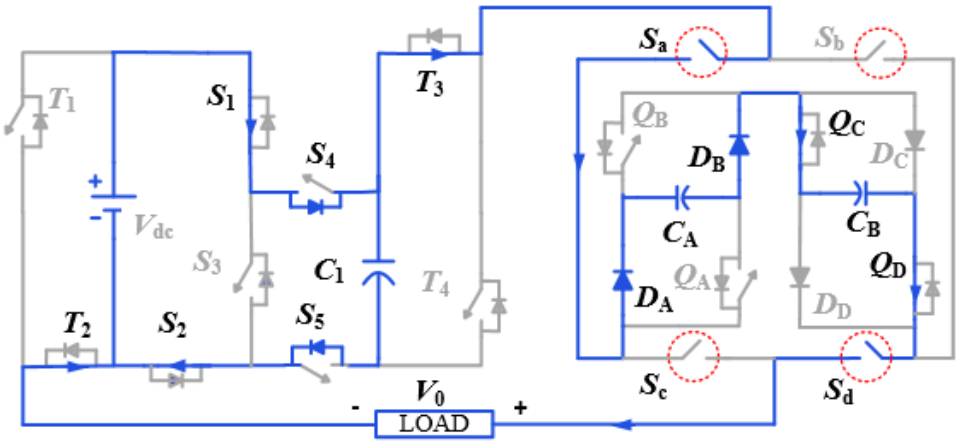


(b)



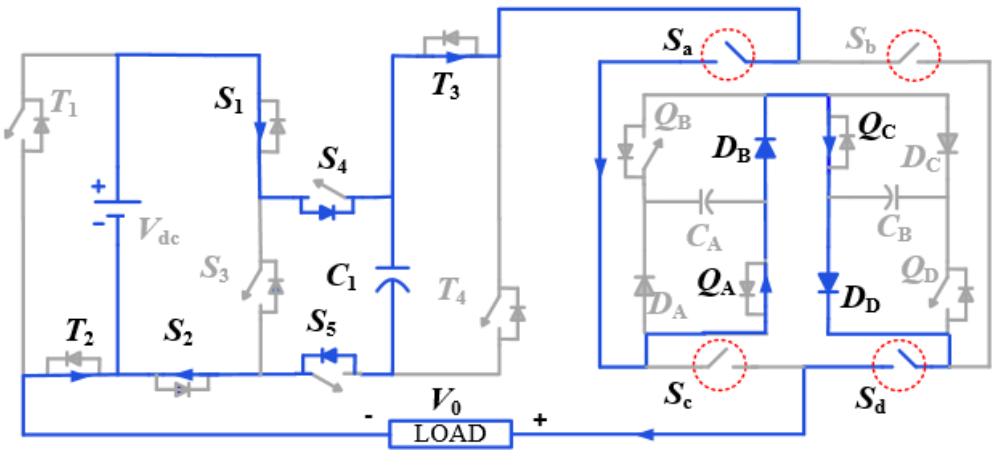
$$V_0 = \frac{1}{2}V_{dc}$$

(c)



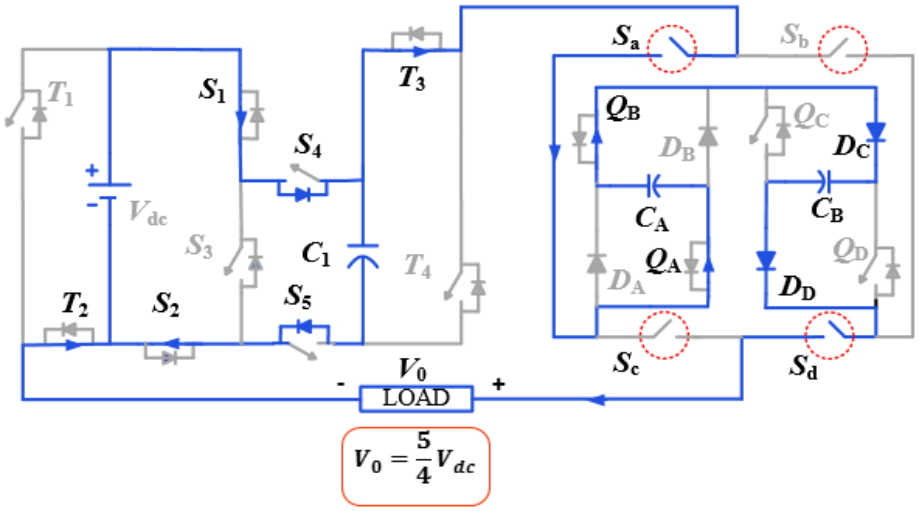
$$V_0 = \frac{3}{4}V_{dc}$$

(d)

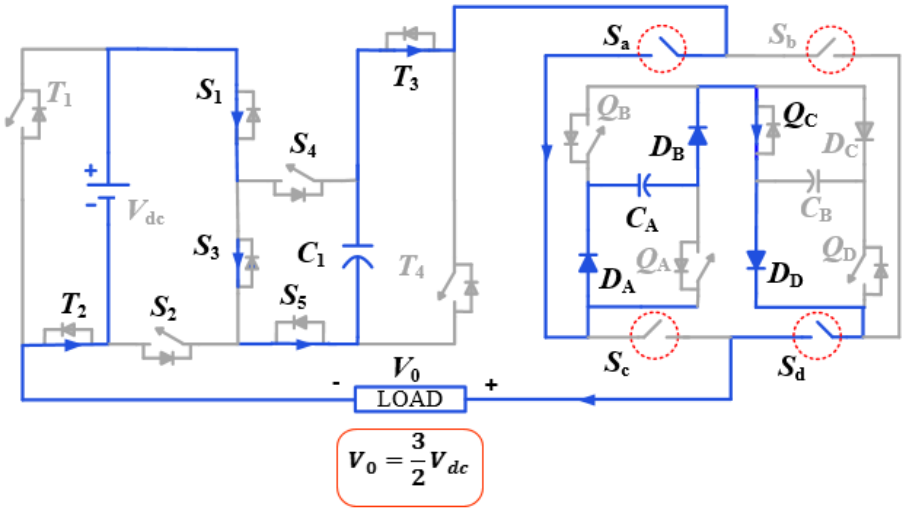


$$V_0 = V_{dc}$$

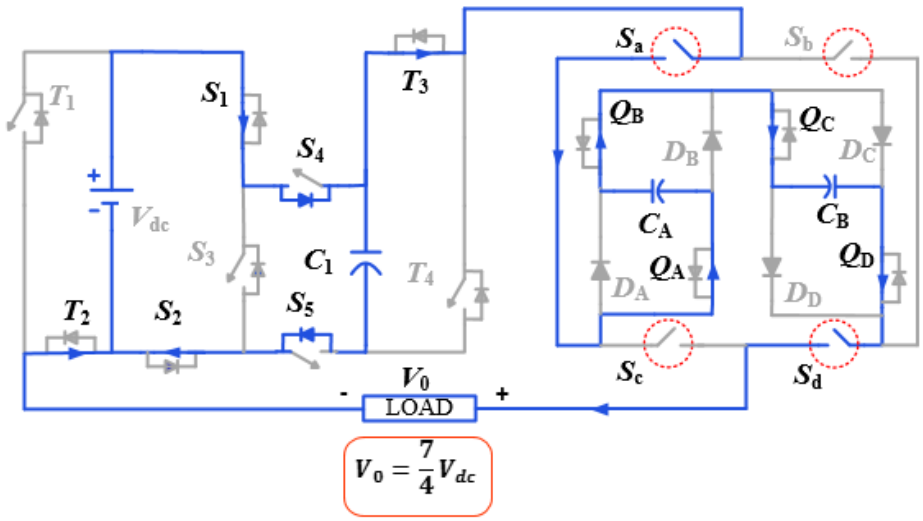
(e)


T_1
S_1
T_3
S_a
S_b
Q_B
D_B
Q_C
D_C
S_4
V_{dc}
C_A
C_B
S_3
C_1
T_4
Q_A
Q_D
D_A
D_D
T_2
S_2
S_5
S_c
S_d
V_0
LOAD
$V_0 = \frac{5}{4} V_{dc}$

(f)


T_1
S_1
T_3
S_a
S_b
Q_B
D_B
Q_C
D_C
S_4
V_{dc}
C_A
C_B
S_3
C_1
T_4
Q_A
Q_D
D_A
D_D
T_2
S_2
S_5
S_c
S_d
V_0
LOAD
$V_0 = \frac{3}{2} V_{dc}$

(g)


T_1
S_1
T_3
S_a
S_b
Q_B
D_B
Q_C
D_C
S_4
V_{dc}
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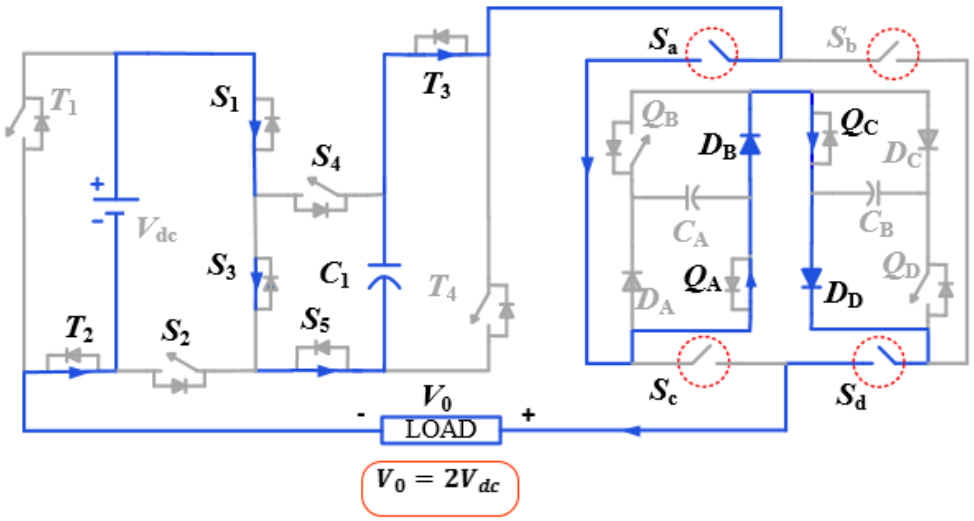
C_B
S_3
C_1
T_4
Q_A
Q_D
D_A
D_D
T_2
S_2
S_5
S_c
S_d
V_0
LOAD
$V_0 = \frac{7}{4} V_{dc}$

(h)



(i)

Fig. 6.2 Current flow for posituve voltage levels of the proposed 17-level RVSC-MLI. (a) Current flow at voltage level zero. (b) Current flow at voltage level $V_{DC}/4$. (c) Current flow at voltage level $V_{DC}/2$. (d) Current flow at voltage level $3V_{DC}/4$. (e) Current flow at voltage level V_{DC}. (f) Current flow at voltage level $5V_{DC}/4$. (g) Current flow at voltage level $3V_{DC}/2$. (h) Current flow at voltage level $7V_{DC}/4$. (i) Current flow at voltage level $2V_{DC}$.

Level $+2V_{dc}$: Fig. 6.2(i) shows the circuit configuration of voltage level $+2V_{dc}$. The voltage source and the capacitor C_1 feeds the load directly without involving any capacitor to generate the voltage level. C_1 is discharged in this interval thorough switches S_1, S_3 and S_5. The capacitors C_A and C_B remains unchanged in this interval. The voltage level $+2V_{dc}$ is obtained as (V_{dc} +V_{dc}).

6.4 Generalized Structure of the Proposed 17-level RVSC-MLI

For achieving higher voltage levels, the proposed RVSC-MLI structure can be extended by cascading the (switches $S_{1,i}$-$S_{5,i}$ and capacitors $C_{1,i}$), where i is the number of units are connected in cascade as shown in Fig. 6.3. The generalized structure of the proposed RVSC-MLI does not require any additional voltage source to achieve higher voltage levels.

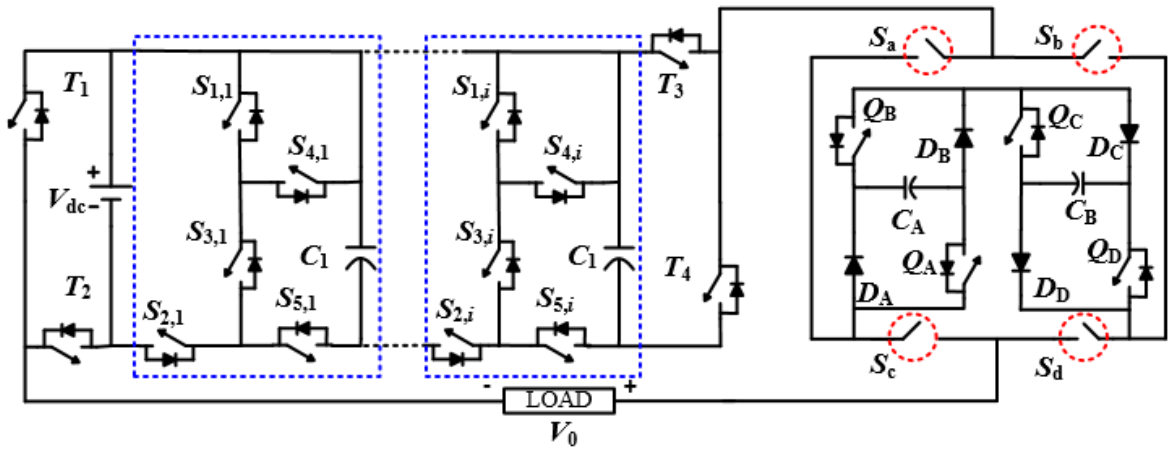


Fig. 6.3 Extended structure of the proposed 17-level RVSC-MLI.

Table 6.2
Maximum Blocking Voltage Across Switches of 17-level RV-SCMLI

Switches	Maximum voltage stress($\times V_{dc}$)	Switches	Maximum voltage stress($\times V_{dc}$)
S_1	1	T_4	1
S_2	1	S_a	$\frac{3}{4}$
S_3	1	S_b	$\frac{3}{4}$
S_4	1	S_c	$\frac{3}{4}$
S_5	1	S_d	$\frac{3}{4}$
T_1	1	Q_A	$\frac{1}{2}$
T_2	1	Q_B	$\frac{1}{2}$
T_3	1	Q_C, Q_D	$\frac{1}{4}$, $\frac{1}{4}$

The maximum blocking voltages of all switches are given in Table 6.2. The PIV across all switches are within input DC source voltage V_{dc}. From Table 6.2, the TSV of the 17-level RVSC-MLI is calculated by adding the individual PIV of all switches and is obtained as

$$\begin{cases} \text{TSV} = 16.5V_{dc} \\ \text{PIV} = 1V_{dc} \end{cases} \tag{6.3}$$

The PIV of switches and diodes in the generalized structure of the proposed RVSC-MLI are within V_{dc}. The number of active and passive elements for generating $8n-7$ voltage levels in the proposed generalized RVSC-MLI (where n is the number of capacitors) can be expressed as

$$\begin{cases} N_{switch} = 5n+6 \\ N_{diode} = 4 \\ N_{source} = 1 \end{cases} \tag{6.4}$$

where N_{switch}, N_{diode} and N_{source} are the number of switches, diodes and DC sources respectively.

6.5 Switching Scheme

Selective harmonic elimination technique using modified grey wolf optimization is used to generate the switching angles of the proposed RVSC-MLI. The switching angles and output voltage levels of the proposed 17-level RVSC-MLI is shown in Fig. 6.4, where the amplitude of each step voltage and switching angle are taken as $\pm V_{dc}/4$ and θ_i (i=1-8) respectively. Fourier expansion of the quasi-square waveform of the output voltage for the proposed 17-level RVSC-MLI is given as

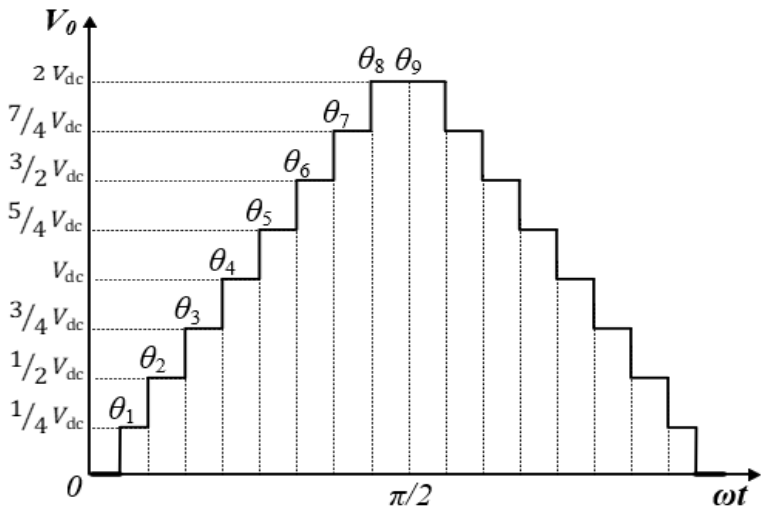


Fig. 6.4 Switching angles and output voltage levels of the proposed 17-level RVSC-MLI.

$$V_0 = \frac{V_{dc}}{2\pi} \sum_{k=1,3,\cdots}^{\infty} \sum_{i=1}^{8} \frac{\cos(k\theta_i)}{k} \sin k\omega t \tag{6.5}$$

where ω is the angular frequency of the staircase output voltage waveform. The amplitude modulation index (M_{of}) of the fundamental output voltage waveform is expressed as:

$$M_{of} = \frac{1}{8} \sum_{i=1}^{8} \cos(\theta_i) \tag{6.6}$$

The switching angles for 17-level RVSC-MLI θ_i (i = 1-8) are obtained using

$$\begin{cases} \cos\theta_1 + \cos\theta_2 + \cos\theta_3 + \cos\theta_4 + \cos\theta_5 + \cos\theta_6 + \cos\theta_7 + \cos\theta_8 = 8M_{of} \\ \cos(m\theta_1) + \cos(m\theta_2) + \cos(m\theta_3) + \cos(m\theta_4) + \cos(m\theta_5) \\ + \cos(m\theta_6) + \cos(m\theta_7) + \cos(m\theta_8) = 0 \end{cases} \tag{6.7}$$

where m is the number of harmonics. The harmonics such as 5th, 7th, 11th, 13th, 17th, 19th and 23rd are considered for obtaining the switching angles.

6.6 Capacitance Calculation

To calculate the values of the capacitances, the longest discharging cycles of the capacitors are considered. It can be observed from Table 6.1 that the capacitor C_1 has the longest discharging cycle in the interval θ_8 to $\pi - \theta_6$. The capacitor C_A has the longest discharging period from $\pi - \theta_6$ to $\pi + \theta_8$, which consists of a few small charging intervals also. The discharging intervals are $\pi - \theta_7$ to $\pi - \theta_6$, $\pi + \theta_2$ to $\pi + \theta_3$, $\pi + \theta_5$ to $\pi + \theta_6$ and $\pi + \theta_7$ to $\pi + \theta_8$, whereas the charging intervals are $\pi - \theta_3$ to $\pi - \theta_2$, $\pi + \theta_1$ to $\pi + \theta_2$, $\pi + \theta_3$ to $\pi + \theta_4$ and $\pi + \theta_6$ to $\pi + \theta_7$. The capacitor C_B has the longest discharging period from θ_7 to θ_8. The maximum discharging values Q_{C1}, Q_A and Q_B of the capacitors C_1, C_A and C_B are given as

$$Q_{C_1} = \frac{1}{\omega}\left[\int_{\theta_8}^{\pi-\theta_8} i_o d\theta + \int_{\pi-\theta_8}^{\pi-\theta_7} i_o d\theta + \int_{\pi-\theta_7}^{\pi-\theta_6} i_o d\theta\right] \tag{6.8}$$

$$Q_{C_A} = \frac{1}{\omega}\left[\int_{\pi-\theta_7}^{\pi-\theta_6} i_o d\theta - \int_{\pi-\theta_3}^{\pi-\theta_2} i_o d\theta - \int_{\pi+\theta_1}^{\pi+\theta_2} i_o d\theta + \int_{\pi+\theta_2}^{\pi+\theta_3} i_o d\theta\right.$$

$$\left. - \int_{\pi+\theta_3}^{\pi+\theta_4} i_o d\theta + \int_{\pi+\theta_5}^{\pi+\theta_6} i_o d\theta - \int_{\pi+\theta_6}^{\pi+\theta_7} i_o d\theta + \int_{\pi+\theta_7}^{\pi+\theta_8} i_o d\theta\right] \tag{6.9}$$

$$Q_{C_B} = \frac{1}{\omega}\left[\int_{\theta_7}^{\theta_8} i_o d\theta\right] \tag{6.10}$$

where $i_0=\frac{v_0}{R_L}$, v_0 is output voltage at the respective intervals (given in Table 6.1) and R_L is load resistance. The maximum allowable voltage ripples across the capacitor C_i is kV_{Ci} (i=1, A, B), where k is the ripple factor. The optimal value of the capacitance (C_i) is given as

$$C_i \geq \frac{Q_{Ci}}{kV_{Ci}} \text{ for } i = 1, \text{A, B} \tag{6.11}$$

Substituting the values of i_0 into (6.8), (6.9) and (6.10) and from (6.11), the values of capacitors (C_1, C_A and C_B) are obtained as

$$C_{1\min} = \frac{1}{8\pi f_S R_L k}\left(8\pi - 6\theta_6 - \theta_7 - 9\theta_8\right) \tag{6.12}$$

$$C_{A\min} = \frac{1}{4\pi f_S R_L k}\left(\theta_1 - \theta_2 + 3\theta_3 - 3\theta_4 - 5\theta_5 + 5\theta_6 - 7\theta_7 + 7\theta_8\right) \tag{6.13}$$

$$C_{B\min} = \frac{1}{2\pi f_S R_L k}\left(-7\theta_7 + 7\theta_8\right) \tag{6.14}$$

6.7 Switching Loss Calculation

The switching loss occurs due to charging and discharging of parasitic capacitances of switches. Switching loss occurs during the turn on and turn off of switches in a cycle [51]. The switching loss during turn on $P_{\mathrm{sw},i(\mathrm{on})}$ and turn off $P_{\mathrm{sw},i(\mathrm{off})}$ are given as

$$\begin{aligned} P_{\mathrm{sw},i\,(\mathrm{on})} &= f_{\mathrm{sw}} \int_0^{t_{on}} V_{\mathrm{sw},i}(\mathrm{t}).i(t)dt \\ &= f_{sw} \int_0^{t_{on}} \left(\frac{V_{sw,i}}{t_{on}} \cdot t \right) \left(-\frac{I_i}{t_{on}} (t - t_{on}) \right) dt \\ &= \frac{1}{6} f_{sw,i} V_{\mathrm{sw},i} I_i t_{on} \end{aligned} \tag{6.15}$$

$$\begin{aligned} P_{\mathrm{sw},i\,(\mathrm{off})} &= f_{\mathrm{sw}} \int_0^{t_{off}} V_{\mathrm{sw},i}(\mathrm{t}).i(t)dt \\ &= f_{sw} \int_0^{t_{off}} \left(\frac{V_{\mathrm{sw},i}}{t_{off}} \cdot t \right) \left(-\frac{I_i^{'}}{t_{off}} (t - t_{off}) \right) dt \\ &= \frac{1}{6} f_{sw} V_{\mathrm{sw},i}\, I_i^{'} t_{off} \end{aligned} \tag{6.16}$$

where $V_{\mathrm{sw,i}}$ is the off-state voltage of the i^{th} switch, I_{i} is the current of the i^{th} switch when the switch is turned on, I_{i}' is the current of the i^{th} switch before the turn off of the switch, t_{on} is the duration when the switch is turned on, t_{off} is the duration when the switch is turned off and f_{sw} is the switching frequency. To calculate total switching loss, the number of N_{on} and the number of N_{off} switching states per one cycle is multiplied by (6.15) and (6.16). The total switching loss is calculated as

$$P_{\mathrm{S}} = \sum_{i=1}^{17} \left(\sum_{j=1}^{N_{on(i)}} P_{\mathrm{sw,on(ij)}} + \sum_{j=1}^{N_{off\,(i)}} P_{\mathrm{sw,off(ij)}} \right) \tag{6.17}$$

Using (6.17), the total switching loss of the proposed 17-level RVSC-MLI is obtained as

$$P_{\mathrm{S}} = \frac{14.65 {V_{dc}}^2}{R_L} f_s t_{on} + \frac{13.76 {V_{dc}}^2}{R_L} f_s t_{off} \tag{6.18}$$

6.8 Conduction Loss Analysis

Conducting loss is caused by the parasitic parameters such as on-state resistances of switches, voltage drops of diodes, and the currents in the circuits. The diodes (including the body diodes of switches) are assumed to have the same voltage drop V_D and resistance r_d. All the switches are assumed to have the same on-state resistance r_s. The conduction loss of the proposed 17-level RVSC-MLI is given as

$$P_{con} = \frac{2}{\pi}\sum_{i=1}^{8}\left\{\frac{V_0 - V_{Deq}}{r_{eq} + R_L}\right\} \times r_{eq}.\left(\theta_{i+1} - \theta_i\right) \tag{6.19}$$

where V_0, V_{Deq}, r_{eq} and R_L are the output voltage, the equivalent voltage drops of diodes, the equivalent parasitic resistance and the load resistance respectively.

6.9 Ripple Loss Analysis

The ripple loss occurs at the time of charging of capacitors at different switching instances. The voltage ripple of capacitors is obtained as

$$\Delta V_{Ci} = \frac{1}{C_i}\int_{t}^{t'} i_{c_i}(t).dt \tag{6.20}$$

where i_{c_i} is the capacitor current and $t - t'$ is the charging interval. The ripple voltages of capacitors (C_1, C_A and C_B) are given as:

$$\Delta V_{C1} = \frac{1}{8\pi f_S R_L C_1}\left(8\pi - 6\theta_6 - \theta_7 - 9\theta_8\right) \tag{6.21}$$

$$\Delta V_{CA} = \frac{1}{4\pi f_S R_L C_2}\left(\theta_1 - \theta_2 + 3\theta_3 - 3\theta_4 - 5\theta_5 + 5\theta_6 - 7\theta_7 + 7\theta_8\right) \tag{6.22}$$

$$\Delta V_{CB} = \frac{1}{2\pi f_S R_L C_B}\left(-7\theta_7 + 7\theta_8\right) \tag{6.23}$$

The ripple loss in one cycle operation of the output voltage is given as

$$P_{\mathrm{R}} = \frac{1}{2T} \sum_{i=1,\mathrm{A},\mathrm{B}} C_i \Delta V_i^2 \tag{6.24}$$

where C_{i} and ΔV_i are the i^{th} capacitor and ripple voltage of it.

The efficiency of the proposed 17-level RVSC-MLI can be written as

$$\eta = \frac{P_0}{P_0 + P_C + P_S + P_R} \tag{6.25}$$

where P_0, P_{C}, P_{S} and P_{R} are the output power, conduction, switching and ripple losses.

6.10 Comparison with Other Reported SC-MLI Topologies

In this section, the proposed RVSC-MLI is compared with other reported SC-MLIs in terms of active and passive components, TSV, PIV and cost as given in Table 6.3. The proposed SC-MLI requires one DC voltage source, PIV and TSV is reduced as compared to the reported SC-MLIs. In [59] and [60] number of sources increases linearly with the output voltage level. In [38], [40], [47] and [56] to generate 17-level output voltage, seven capacitors are required and TSV and PIV are also relatively higher as compared to proposed RVSC-MLI. The topology presented in [40] and [47] requires thirty-nine and twenty-five switches to generate a 17-level output voltage with higher TSV and PIV as compared to proposed topology. The TSV and PIV of the topologies [12-18] and DASC-MLI are much higher than the proposed RVSC-MLI. The generalized graphical representation of PIV and TSV versus output voltage levels for different topologies are shown in Fig. 6.5(a) and (b).

A cost function (CF) has been used to compare the proposed RVSC-MLI with the reported SC-MLIs and is given as [54]

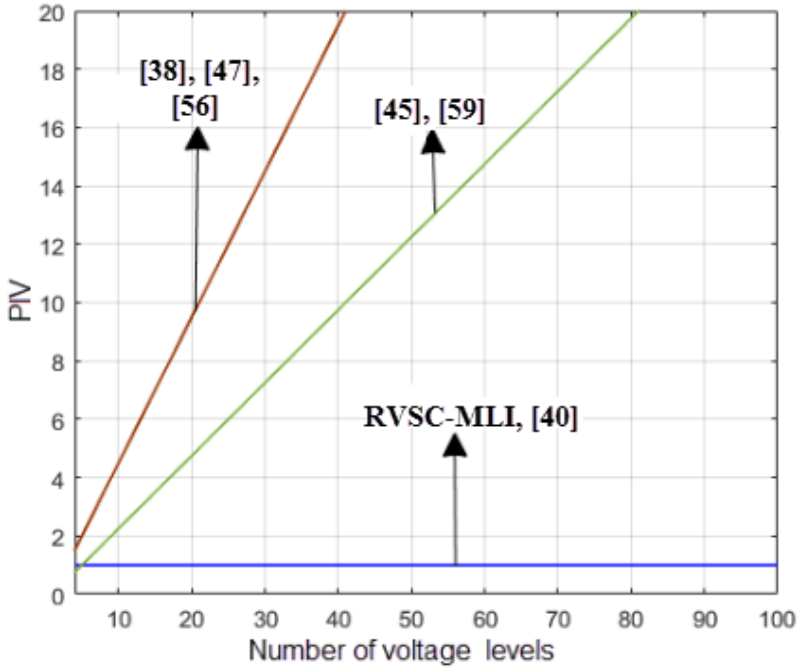
$$\mathrm{CF} = \left(N_{\mathrm{switch}} + N_{\mathrm{cap}} + N_{\mathrm{diode}} + \lambda TSV_{\mathrm{pu}} + \delta PIV_{\mathrm{pu}} \right) N_{\mathrm{source}} \tag{6.26}$$

Table 6.3
Comparison of proposed 17-level RVSC-MLI with Reported 17-level SC-MLI Topologies

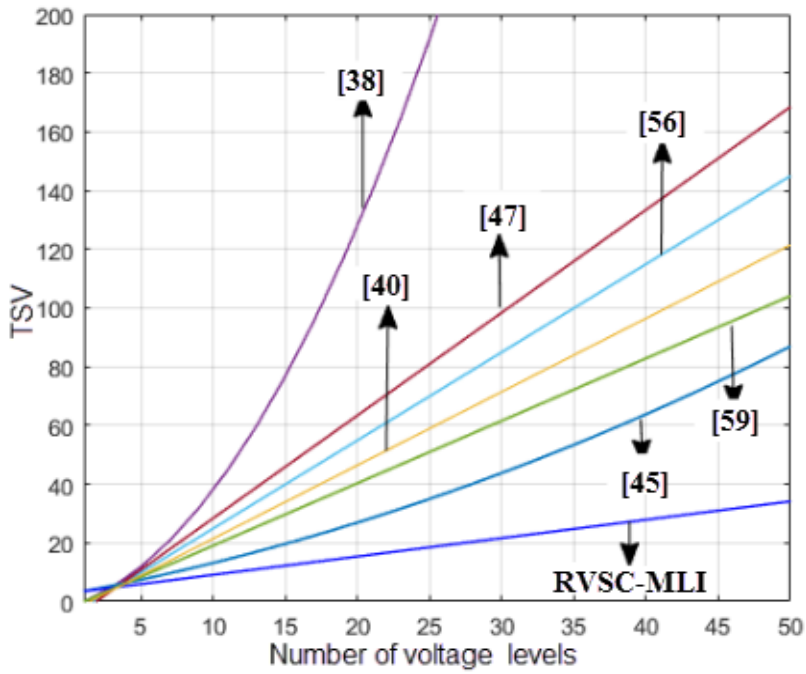
Parameters	[60]	[47]	[40]	[59]	[56]	[38]	[45]	DASC-MLI	RVSC-MLI
N_{Source}	8	1	1	4	1	1	1	1	1
N_{Switch}	18	25	39	14	18	12	17	11	21
N_{Cap}	0	7	7	4	7	7	4	4	3
N_{Diode}	0	0	0	20	7	14	4	5	4
TSV($\times V_{dc}$)	32	53	39	34	46	96	29	25.5	16.5
PIV($\times V_{dc}$)	8	8	1	4	8	8	4	4	1
CF (λ=0.5, δ=0.5)	304	62.5	66	228	59	85	41.5	34.75	36.75
CF (λ=1.5, δ=0.5)	560	115.5	105	364	105	181	70.5	60.25	53.25
CF (λ=0.5, δ=1.5)	368	70.5	67	244	67	93	45.5	38.75	37.75
CF (λ=1.5, δ=1.5)	624	123.5	106	380	113	189	74.5	64.25	54.25
Boosting Feature and Extendibility	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes

where N_{switch}, N_{cap}, N_{diode} and N_{source} are the number of switches, capacitors, diodes, DC source and λ, δ are the importance factors of TSV_{pu} and PIV_{pu}. The active/passive components such as the number DC voltage sources, number of switches, capacitors and diodes are considered in the cost calculation. To explain the effects of TSV and PIV in the proposed CF, weight coefficients λ and δ are multiplied in per unit scales. The values of λ and δ mentioned in Table 3 are: λ=0.5, δ=0.5; λ=1.5, δ=0.5; λ=0.5, δ=1.5 and λ=1.5, δ=1.5. It is important to note that if λ and δ are less than one, the required number of passive components are given more importance in the cost calculation. However, if λ and δ are more than one, TSV and PIV are given more importance in the cost calculation. Referring Table 6.3, when λ=0.5 and δ=0.5, the required number of passive components are given more importance; for λ=1.5 and δ=0.5, TSV is given more importance; for λ=0.5 and δ=1.5, PIV is given more importance; for λ=1.5 and δ=1.5, both TSV and PIV are given importance in the cost calculation. Thus, the cost calculated using four different

values of λ and δ shows the merits of the proposed RVSC-MLI for all cases, whether passive components or TSV and/or PIV are given more importance.



(a)



(b)

Fig. 6.5 Comparison of the proposed 17-level RVSC-MLI with reported SC-MLIs. (a) PIV versus number of voltage levels. (b) TSV with number of voltage levels.

6.11 Simulation Studies

The performance of the proposed RVSC-MLI is simulated in MATLAB/Simulink. The DC source voltage V_{DC} is taken as 100 V. Fundamental switching strategy (50 Hz) is used and the value of modulation index is taken as 0.75. Considering 10% voltage ripple, the values of capacitors C_1, C_A and C_B obtained using (6.12)-(6.14) are approximately 1470 µF, 660 µF and 800 µF respectively. The output voltage V_0 and current I_0 waveforms of the proposed 17-level RVSC-MLI for a resistive load (R = 40 Ω) are shown in Fig. 6.6(a). The measured rms values of voltage and current are 135.5 V and 3.42 A respectively.

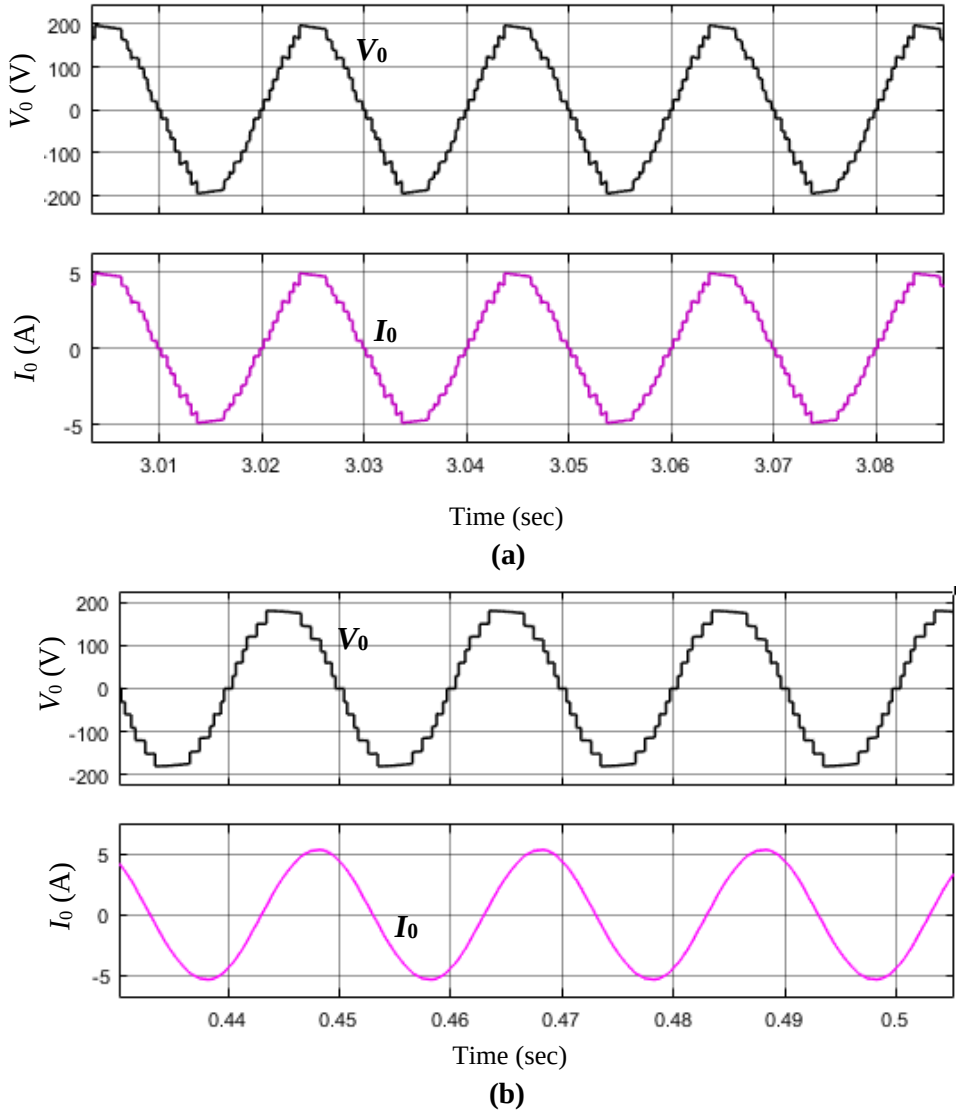


Fig. 6.6 Simulation results of the proposed 17-level RVSC-MLI. (a) Output voltage (V_o) and current (I_o) for R load (R= 40 Ω). (b) Output voltage (V_o) and current (I_o) for R-L load (R= 40 Ω, L= 60 mH).

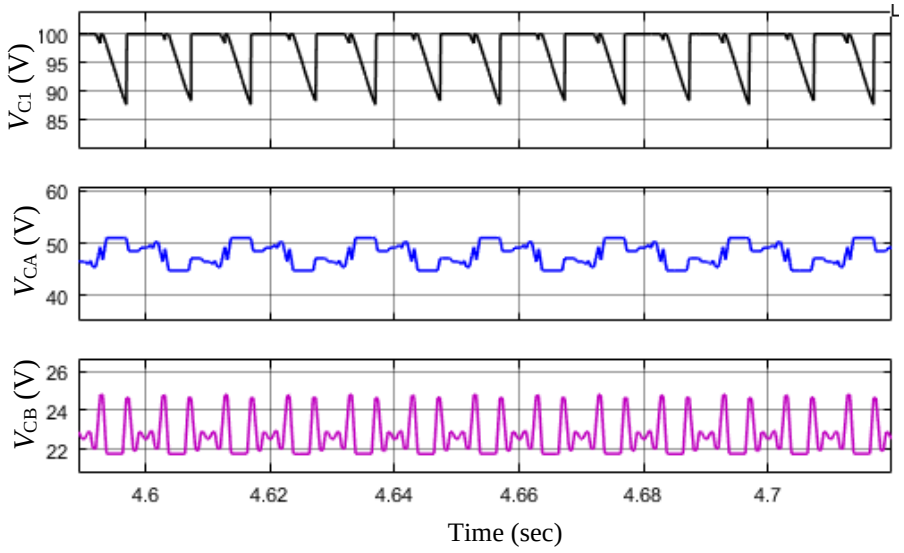
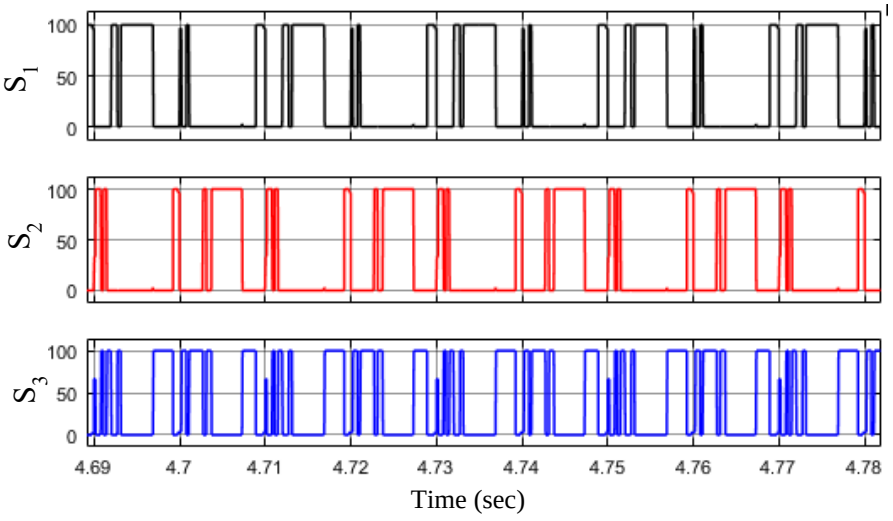


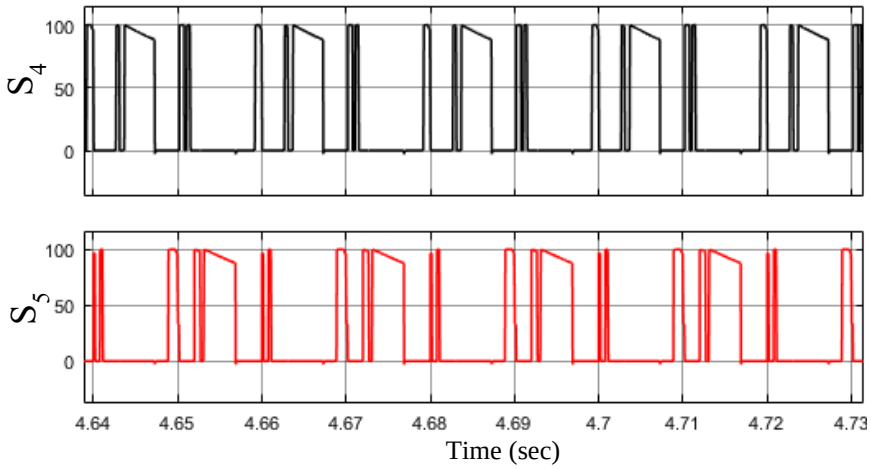
Fig. 6.7 Simulation results of capacitor voltages of RV-SCMLI. (V_{C1}, V_{CA} and V_{CB}).

The output voltage V_0 and current I_0 waveforms for *R-L* (40 Ω and 60 mH) condition loading condition is shown in Fig. 6.6(b). The three capacitor voltages are shown in Fig. 6.7. It can be observed from Fig. 6.7 that capacitor voltages V_{C1}, V_{CA} and V_{CB} are self-balanced at voltages V_{C1} = 100 V, V_{CA} = 50 V and V_{CB} = 25 V respectively. The voltage stresses across switches of (S_1, S_2, S_3, S_4 and S_5) of the proposed RVSC-MLI are shown in Fig. 6.8(a) and (b) respectively. The voltage stresses across switches (S_1, S_2, S_3 S_4 and S_5) are measured as 100 V respectively. The voltage stresses across switches (S_a, S_b, S_c and S_d) are shown in Fig. 6.8(c). It can be observed from Fig.6.8(c) that the voltage measured across switches (S_a, S_b, S_c and S_d) are 75 V respectively.

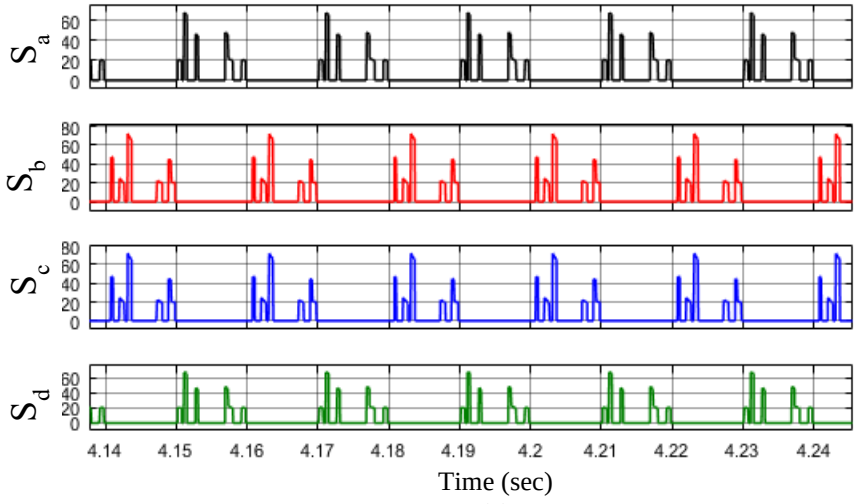


(a)

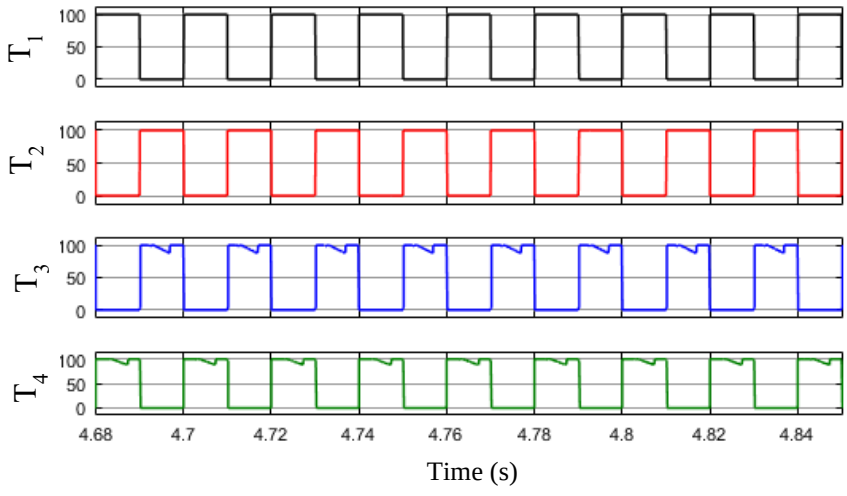
The voltage stresses across switches T_1, T_2, T_3 and T_4 are shown in Fig. 6.8(d) and are measured as 100 V respectively. Similarly, the voltage stresses across switches (Q_A, Q_B, Q_C and Q_D) are shown in Fig. 6.8(e) and measured as 50 V, 50 V, 25 V and 25 V respectively.



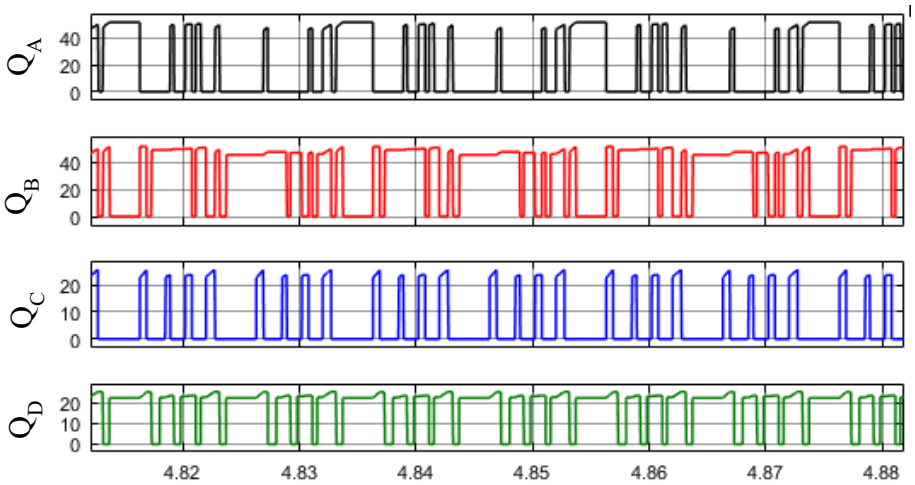
(b)



(c)



(d)



(e)

Fig. 6.8 Simulation results of voltage stress of the proposed RVSC-MLI. (a) Voltage stresses across switches (S_1, S_2 and S_3). (b) Voltage stresses across switches (S_4 and S_5). (c) Voltage stresses across switches (S_a, S_b, S_c and S_d). (d) Voltage stresses across switches (T_1, T_2, T_3 and T_4). (e) Voltage stresses across switches (Q_A, Q_B, Q_C and Q_D).

The dynamic performance of the proposed RVSC-MLI is verified through simulation in this work. The load resistance is step changed from 80 Ω to 40 Ω to observe the dynamic behaviour of the RV-SCMLI. The load current is changed from 1.8 A to 3.53 A due to step change in resistance and is shown in Fig. 6.9. From Fig. 6.9, it can be noticed that the load change does not any effect on output voltage waveform. Hence, it confirms the inherent voltage balance of capacitors in the proposed RVSC-MLI.

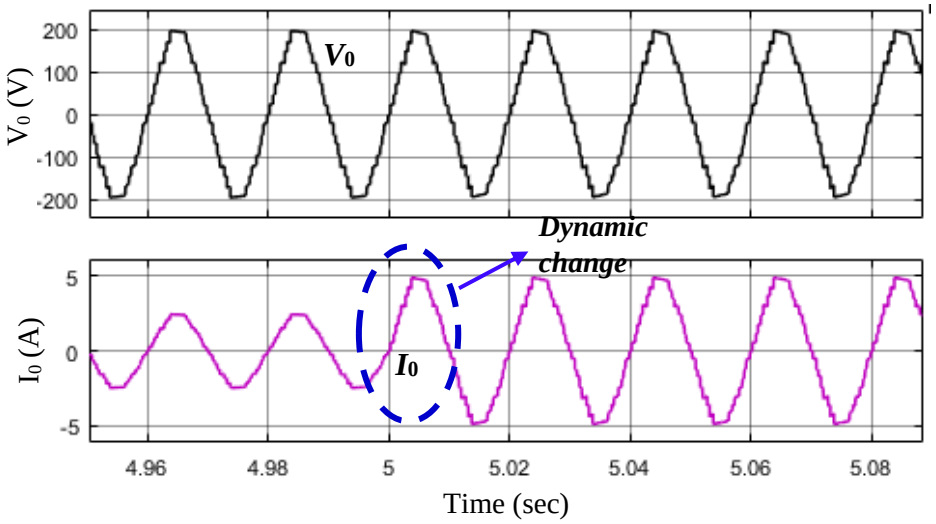


Fig. 6.9 Dynamic performance of the proposed RVSC-MLI for step-down change in load resistance.

6.12 Experimental Validation

The performance of the proposed RVSC-MLI is validated through a 550 W experimental prototype, as shown in Fig. 6.10. The parameters used in experiment are listed in Table 6.4.

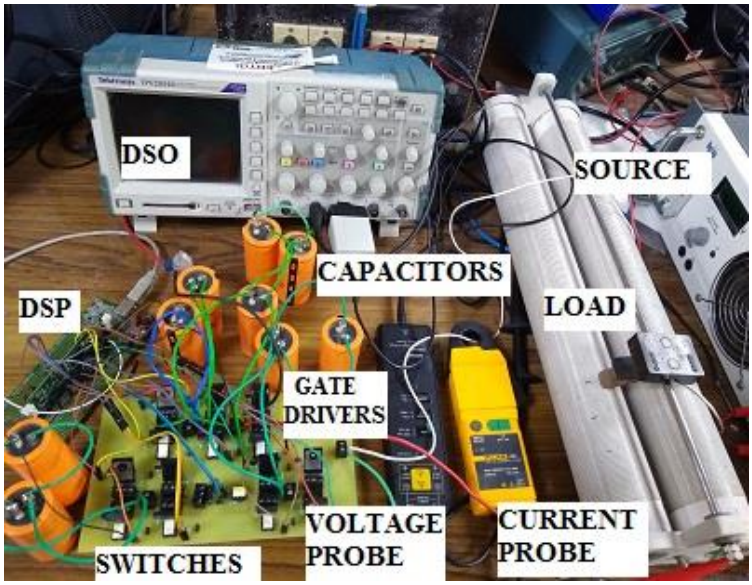


Fig. 6.10 Photograph of experimental prototype (17-level RV-SCMLI).

Table 6.4
Devices and Parameters Used for Experimentation

Microcontroller	TI-TMS320F28335
IGBT	HGTG12N60A4D
Gate Drivers	FOD-3184
Electrolytic Capacitors	1470µF (C_1), 660 µF (C_A) and 800 (C_B)

6.12.1 Steady State Performance

The steady state performance of the proposed RV-SCMLI is investigated in this section. The input DC source voltage V_{dc} is as taken 100 V. Fundamental switching strategy (50 Hz) is used and the value of M_{of} is taken as 0.75 in this study. The input voltage V_{dc}, input current $I_{in,}$ voltage V_0 and output current I_0 waveforms of the proposed 17-level RVSC-MLI for a resistive load ($R = 40\ \Omega$) are shown in Fig. 6.11(a) and the rms values of V_0 and I_0 are 134.8 V and 3.37 A respectively. The measured frequency of V_0 and I_0 is 50 Hz.

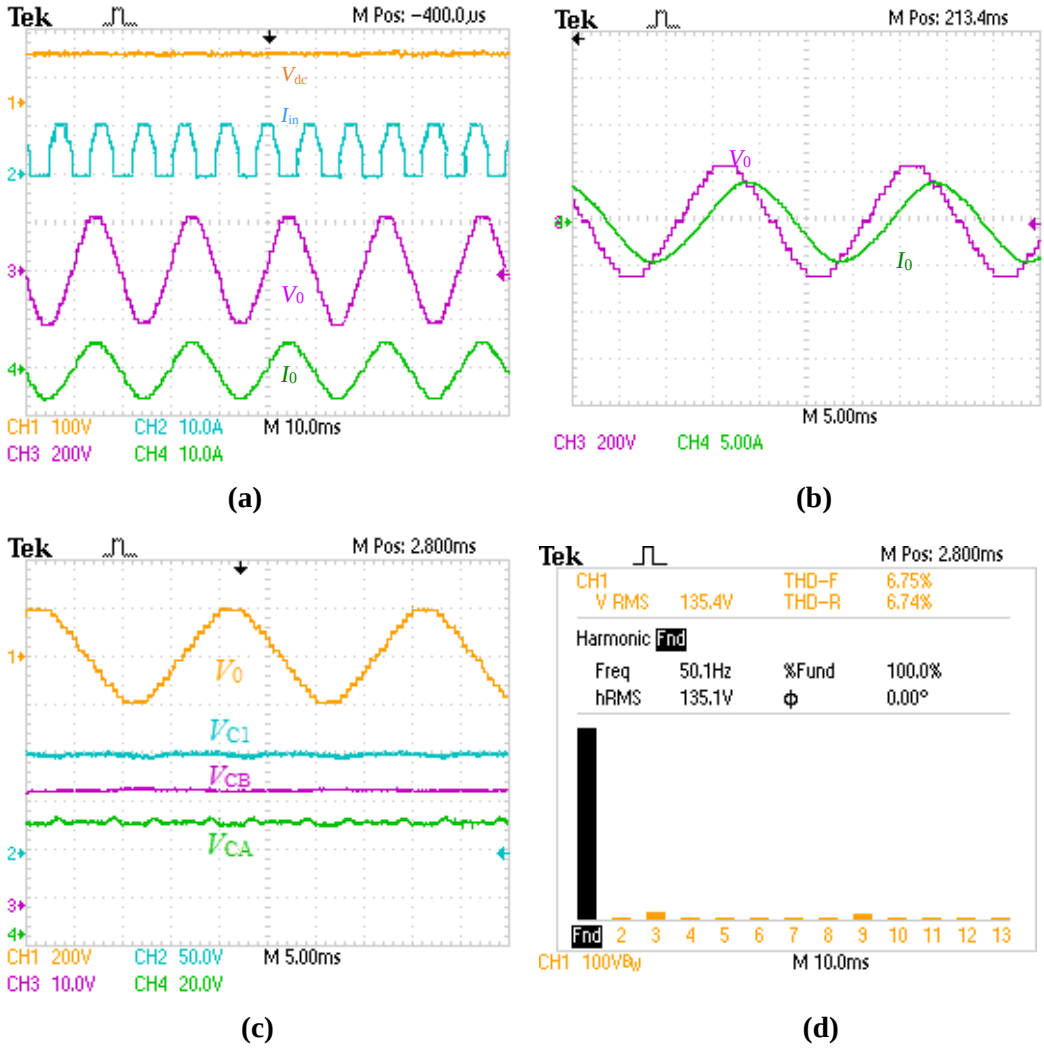


Fig. 6.11 Experimental results of the proposed RVSC-MLI. (a) Input voltage (V_{dc}), Input current (I_{in}), Output voltage (V_o) and current (I_o) for *R* load. (b) Output voltage (V_o) and current (I_o) for *R-L* load. (c) Capacitor voltages (V_{C1}, V_{CA}, V_{CB}). (d) Harmonic spectrum of V_o.

For *R-L* load (R = 40 Ω, L = 60 mH), output voltage V_0 and current I_0 are shown in Fig. 6.11(b). It can be observed from Fig. 6.11(c) that capacitor voltages (V_{C1}, V_{CA} and V_{CB}) are balanced at 100 V, 50 V and 25 V respectively. The ripples voltage ΔV_{C1}, ΔV_{CA} and ΔV_{CB} of capacitors are 9 V, 4.5 V and 2.5 V respectively. The harmonic spectrum of the output voltage V_0 is shown in Fig. 6.11(d) and THD is measured as 6.75%. The voltage stresses across switches of (S_1, S_2, S_3, S_4 and S_5) are shown in Fig. 6.12(a) and (b) and measured as 100 V respectively. Similarly, the voltage stresses across switches (T_1, T_2, S_c and S_d) and (T_3, T_4, S_a and S_b) are shown in Fig. 6.12(c) and (d) respectively.

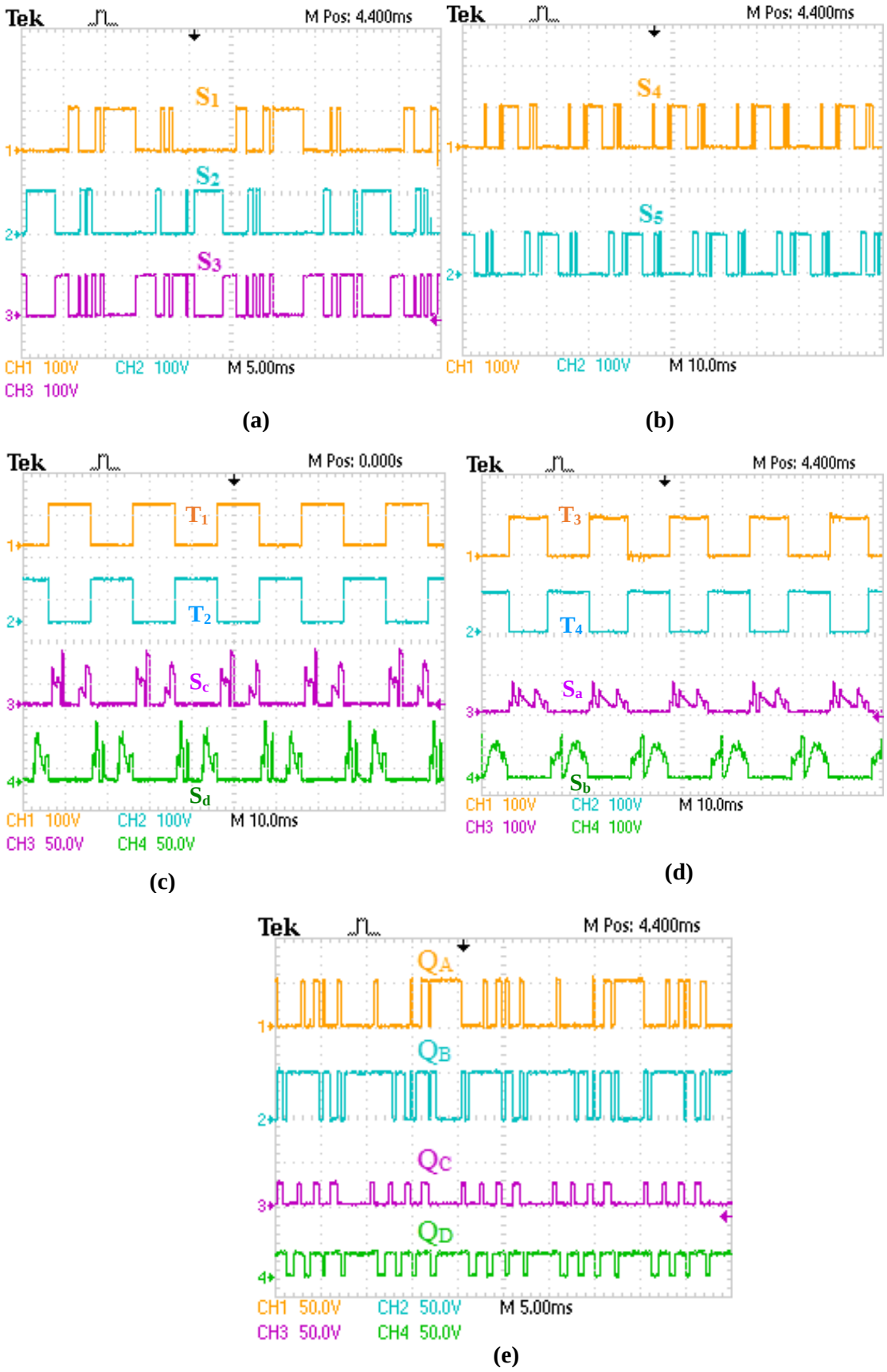
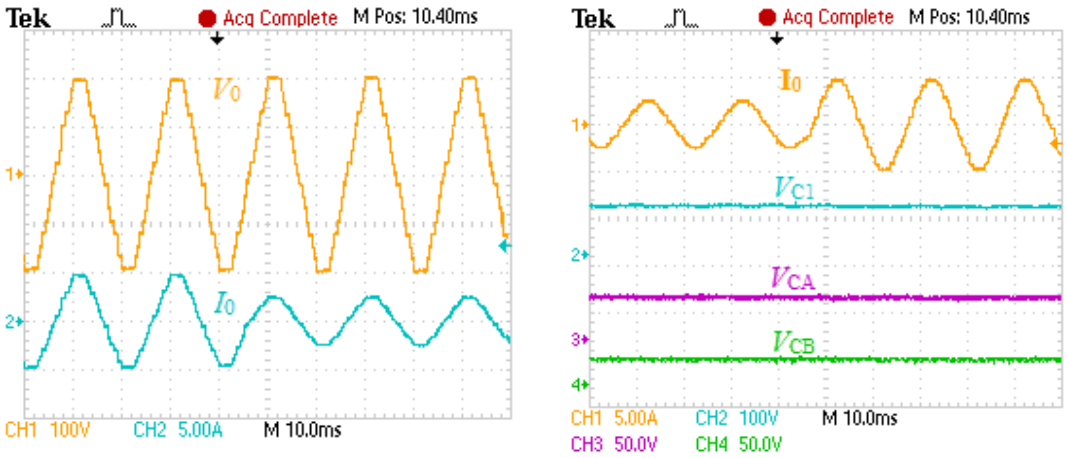


Fig. 6.12 Experimental results of voltage stresses of the proposed RVSC-MLI. (a) Voltage stresses across switches (S_1, S_2, S_3). (b) Voltage stresses across switches (S_4, S_5). (c) Voltage stresses across switches (T_1, T_2, S_c, S_d). (d) Voltage stresses across switches (T_3, T_4, S_a, S_b). (e) Voltage stresses across switches (Q_A, Q_B, Q_C, Q_D).

It can be observed that the voltage stress across the switches T_1, T_2, S_c and S_d are 100 V, 100 V, 75 V and 75 V respectively and the voltage stresses across switches T_3, T_4, S_a and S_b are 100 V, 100 V, 75 V and 75 V respectively. The voltage stresses across switches (Q_A, Q_B, Q_C and Q_D) are shown in 6.12(e) and are measured as Q_A, Q_B, Q_C and Q_D are 50 V, 50 V, 25 V and 25 V respectively.

The voltage stresses across diodes of the proposed SC-MLI are also within input DC voltage V_{dc}. From the experimental results, it is verified that the PIV of all switches of the proposed RVSC-MLI are within input DC voltage V_{dc}. The voltage stresses across diodes of the proposed RVSC-MLI are also within V_{dc}.

The switching loss, conduction loss and ripple loss are calculated using (6.18), (6.19) and (6.24) and are given as 8.51 W, 20.78 W and 9.67 W respectively. From Fig. 6.11(a), the measured input power P_{in} = 500 W, output power P_{out} = 456 W and loss P_{loss} = 44 W, which gives efficiency η = 91.2%.



(a) **(b)**

Fig. 6.13 Dynamic performance of the proposed RVSC-MLI. (a) Step-down change in load current. (b) Step-up change in load current.

6.12.2 Dynamic Performance

The dynamic performance of the proposed RV-SCMLI is investigated in this section. The load resistance is changed to observe the dynamic response of the proposed RVSC-MLI.

The dynamic response for step-down change in load current 5 A (peak) to 2.5 A (peak) and step-up change in load current 2.5 A (peak) to 5 A (peak) are shown in Fig. 6.13(a) and (b) respectively. From Fig. 6.13(a) it can be observed that the load change does not have any considerably effect on the output voltage waveform and Fig. Fig. 6.13(b) confirms the self-voltage balance of capacitors in the proposed RVSC-MLI.

6.13 Conclusion

An extendable 17-level RVSC-MLI with reduced voltage stress and lesser number of active and passive components using a single DC voltage source is presented in this chapter. It has been observed that the PIV across all the switches and diodes are within the input DC voltage in proposed RVSC-MLI. Higher voltage levels than 17 can also be achieved through the extended structure of the proposed RVSC-MLI. The proposed RVSC-MLI requires lower rated power switches as compared to existing SC-MLIs due to reduction in PIV. Moreover, a voltage gain of two is achieved through the proposed 17-level RVSC-MLI which can be further increased through the extended structure of it. Comparative analysis with the reported SC-MLIs validates its merits in terms of PIV, TSV and active/passive components. Capacitor voltage balance has been achieved in the proposed RVSC-MLI without using any additional circuit. The performance of the proposed RVSC-MLI has been validated through experimental prototype.