Chapter 5

A 17-Level Diode Assisted Switched Capacitor Multilevel Inverter

5.1 Introduction

In this chapter, a new 17-level diode assisted switched-capacitor MLI (DASC-MLI) is proposed. The proposed DASC-MLI generates output voltage using single DC voltage source and lower number of active and passive components, and has reduced total standing voltage (TSV) and peak inverse voltage (PIV) as compared to conventional SC-MLIs. The DASC-MLI possesses reverse current capability and can also be extended to obtain higher voltage levels through its extended structure. The capacitors are self-balanced in the proposed DASC-MLI without any additional voltage balancing mechanism. Output voltages higher than input voltage can be achieved through DASC-MLI, thus signifying its voltage boosting ability. The overall cost and volume of the proposed DASC-MLI, reduces considerably as compared to other reported SC-MLIs.

5.2 Proposed 17-level Diode Assisted Switched-Capacitor MLI

The basic module of diode assisted switched-capacitor MLI (DASC-MLI) is shown in Fig. 5.1. It uses series-parallel combinations of voltage source and capacitor to maintain the capacitor voltages at the desired levels. It can be observed from Fig. 5.1(a) that the capacitors are charged through parallelization by voltage source, when the switch S_w is turned ON. In this mode, both the diodes D_{Da} and D_{Db} are reverse biased. As can be seen in Fig. 5.1(b), the capacitor is discharged to obtain higher voltage levels by turning OFF the switch S_w, thus forcing the current to flow through forward biased diodes D_{Da} and D_{Db}. This module forms the basis of the proposed DASC-MLI and is connected to DASC-

MLI by four connection points α, β, γ and δ as highlighted in Fig. 5.1. The complete structure of proposed DASC-MLI and the connection with one of the modules is shown in Fig. 5.2. It consists of a single DC source, four capacitors C_1-C_4, five diodes D_1-D_5 and eleven switches S_1-S_{11}. The capacitor voltages of C_1, C_2 and C_3 are balanced at input voltage V_{DC} respectively, whereas the capacitor voltage of C_4 is balanced at $V_{DC}/2$. The mathematical derivation for voltage balancing of capacitor C_4 is explained below. Assuming that the output voltage and current waveforms possess half wave symmetry, the average current flowing through the capacitor (C_4) with R as the load resistance is given as

$$I_{C,\frac{7V_{dc}}{2}}^{+} = \frac{4V_{dc} - V_{C_4}}{R_L} \qquad I_{C,\frac{5V_{dc}}{2}}^{+} = \frac{3V_{dc} - V_{C_4}}{R_L} \qquad I_{C,\frac{3V_{dc}}{2}}^{+} = \frac{2V_{dc} - V_{C_4}}{R_L}$$

$$I_{C,\frac{V_{dc}}{2}}^{+} = \frac{V_{dc} - V_{C_4}}{R_L} \qquad I_{C,\frac{V_{dc}}{2}}^{-} = \frac{-V_{C_4}}{R_L} \qquad I_{C,\frac{3V_{dc}}{2}}^{-} = \frac{-V_{dc} - V_{C_4}}{R_L}$$

$$I_{C,\frac{5V_{dc}}{2}}^{-} = \frac{-2V_{dc} - V_{C_4}}{R_L} \qquad I_{C,\frac{7V_{dc}}{2}}^{-} = \frac{-3V_{dc} - V_{C_4}}{R_L} \tag{5.1}$$

where I_C^+ and I_C^- are currents through C_4 in positive and negative half cycle of output voltage V_0. The expression for net charge (Q) delivered/absorbed for a period T can be expressed as

$$\mathrm{Q} = I_{C,\frac{7V_{dc}}{2}}^{+} \cdot \left(\frac{\theta_8 - \theta_7}{\pi}\right).T + I_{C,\frac{5V_{dc}}{2}}^{+} \cdot \left(\frac{\theta_6 - \theta_5}{\pi}\right).T + I_{C,\frac{3V_{dc}}{2}}^{+} \cdot \left(\frac{\theta_4 - \theta_3}{\pi}\right).T +$$

$$I_{C,\frac{V_{dc}}{2}}^{+} \cdot \left(\frac{\theta_2 - \theta_1}{\pi}\right).T + I_{C,\frac{V_{dc}}{2}}^{-} \cdot \left(\frac{\theta_2 - \theta_1}{\pi}\right).T + I_{C,\frac{3V_{dc}}{2}}^{-} \cdot \left(\frac{\theta_4 - \theta_3}{\pi}\right).T +$$

$$I_{C,\frac{5V_{dc}}{2}}^{-} \cdot \left(\frac{\theta_6 - \theta_5}{\pi}\right).T + I_{C,\frac{7V_{dc}}{2}}^{-} \cdot \left(\frac{\theta_8 - \theta_7}{\pi}\right).T \tag{5.2}$$

$$Q = \left(\frac{V_{DC} - 2V_{C_4}}{R_L}\right) \cdot \left(\frac{\theta_8 - \theta_7 + \theta_6 - \theta_5 + \theta_4 - \theta_3 + \theta_2 - \theta_1}{\pi}\right) . T = 0$$

$$V_{DC} = \frac{V_{C_4}}{2} \tag{5.3}$$

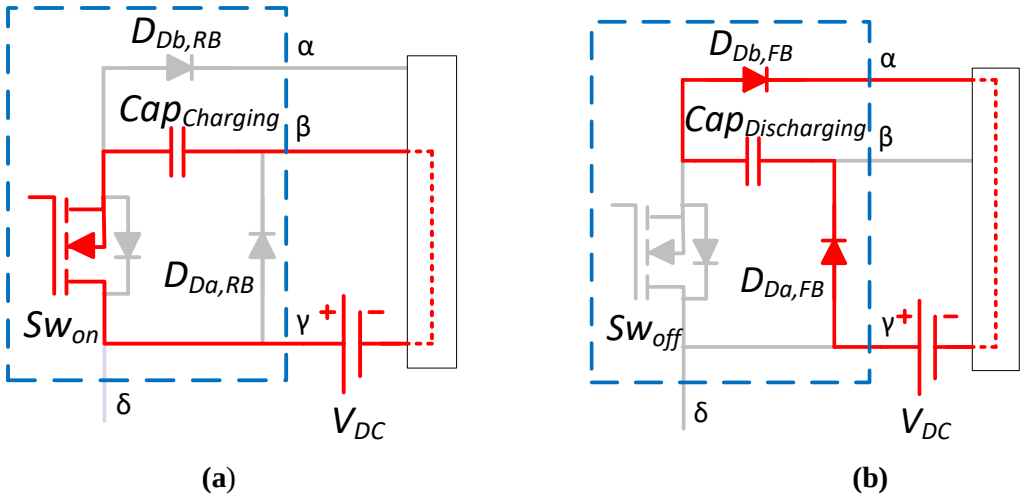


Fig. 5.1 Modes of DASC module (a) Charging (b) Discharging.

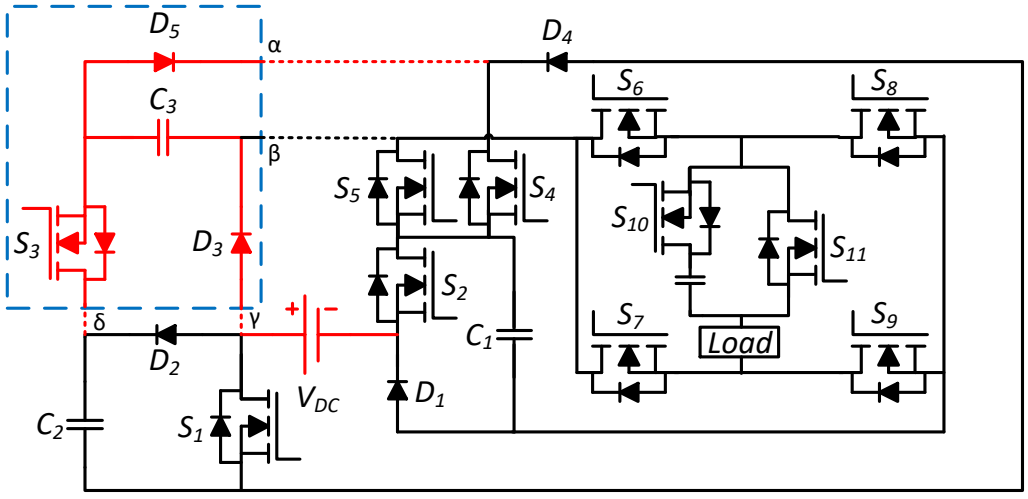


Fig. 5.2 Proposed 17-level DASC-MLI.

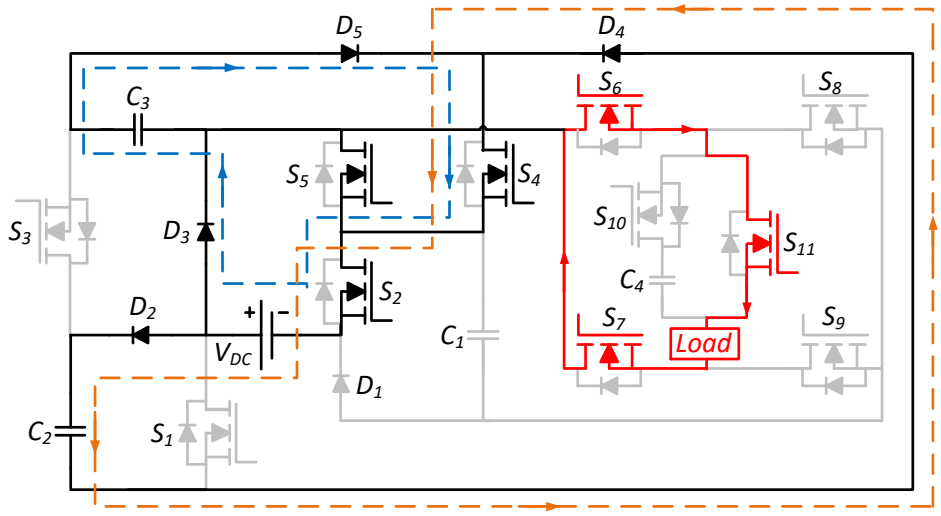
The switching patterns, diode behaviour and states of capacitors at each voltage level of the proposed DASC-MLI are shown in Table 5.1. The current paths of the proposed 17-level DASC-MLI for all positive levels are shown in Fig. 5.3(a)-(i). The dotted lines show

Table 5.1
Switching patterns, Diode behaviour and Capacitor states at each voltage level

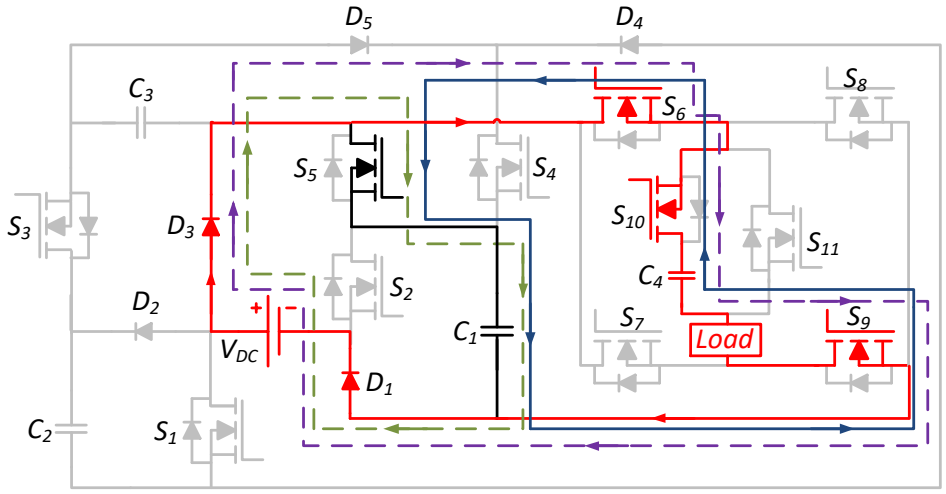
Output Voltage	$S_1 - S_{11}$	$D_1 - D_5$	$C_1 - C_4$
$+4V_{DC}$	1 1 1 0 0 1 0 0 1 0 1	0 0 0 0 0	DDDU
$+7V_{DC}/2$	1 1 1 0 0 1 0 0 1 1 0	0 0 0 0 0	DDDC
$+3V_{DC}$	1 0 1 0 0 1 0 0 1 0 1	1 0 0 0 0	UDDU
$+5V_{DC}/2$	1 0 1 0 0 1 0 0 1 1 0	1 0 0 0 0	UDDC
$+2V_{DC}$	0 1 0 1 0 1 0 0 1 0 1	0 1 1 1 1	DCCU
$+3V_{DC}/2$	0 1 0 1 0 1 0 0 1 1 0	0 1 1 1 1	DCCC
$+V_{DC}$	0 0 0 0 1 1 0 0 1 0 1	1 0 1 0 0	CUUU
$+V_{DC}/2$	0 0 0 0 1 1 0 0 1 1 0	1 0 1 0 0	CUUC
0	0 1 0 1 0 1 1 0 0 0 1	0 1 1 1 1	UCCU
$-V_{DC}/2$	0 0 0 1 1 1 1 0 0 1 0	0 1 1 1 1	UCCD
$-V_{DC}$	0 0 0 0 1 0 1 1 0 0 1	1 0 1 0 0	CUUU
$-3V_{DC}/2$	0 0 0 0 1 0 1 1 0 1 0	1 0 1 0 0	CUUD
$-2V_{DC}$	0 1 0 1 0 0 1 1 0 0 1	0 1 1 1 1	DCCU
$-5V_{DC}/2$	0 1 0 1 0 0 1 1 0 1 0	0 1 1 1 1	DCCD
$-3V_{DC}$	1 0 1 0 0 0 1 1 0 0 1	1 0 0 0 0	UDDU
$-7V_{DC}/2$	1 0 1 0 0 0 1 1 0 1 0	1 0 0 0 0	UDDD
$-4V_{DC}$	1 1 1 0 0 0 1 1 0 0 1	0 0 0 0 0	DDDU

In the column of switches, 1 and 0 represent turn ON and turn OFF. In the column of diode, 1 and 0 represent forward conduction and reverse blocking. The capacitor states are C for charging, D for discharging, and U for unchanged.

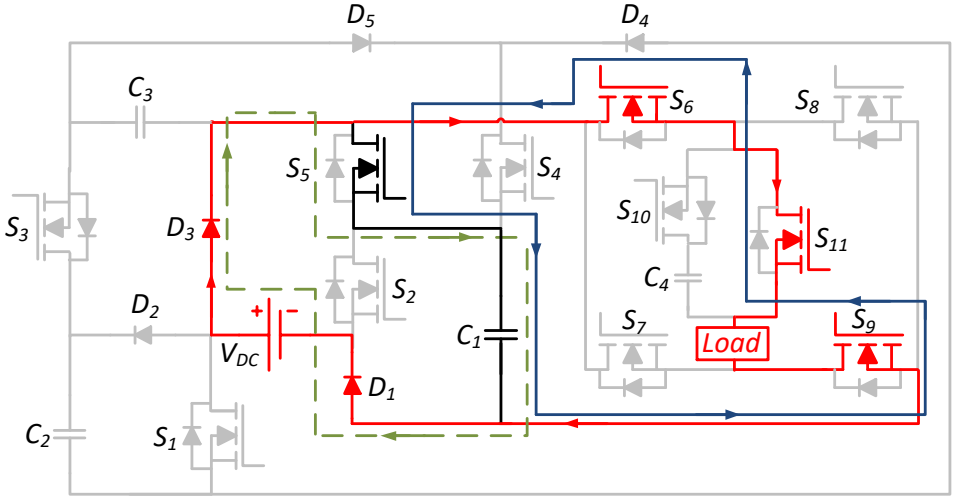
the charging path of the capacitors, the red (solid) lines show the current path through the load, and the blue (solid) lines show the reverse current path of the proposed DASC-MLI. All circuit configurations for voltage levels in one complete positive half cycle of output voltage are as follows:


D5
D4
C3
S6
S8
S5
S4
S10
S11
S3
D3
C4
S2
D2
+
-
C1
S7
Load
S9
VDC
D1
C2
S1

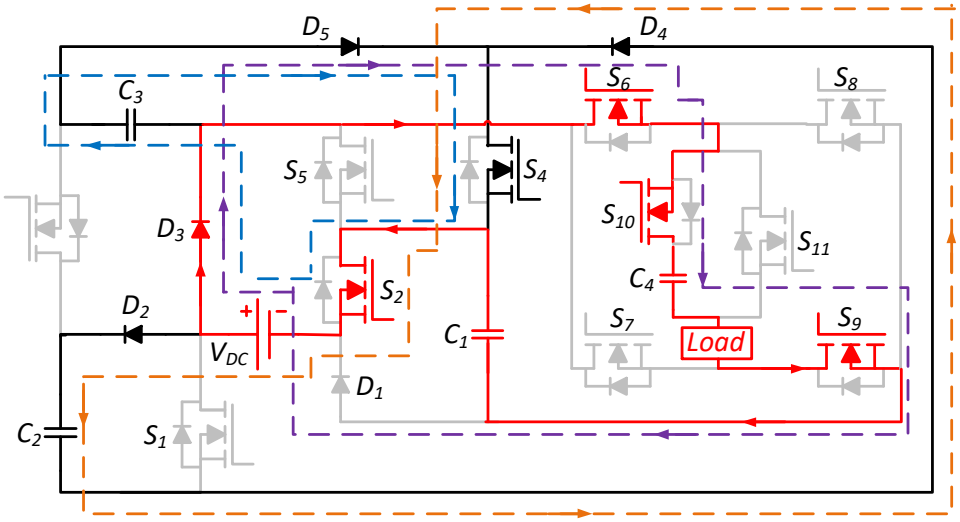
(a)


D5
D4
C3
S8
S6
S5
S4
S10
S11
S3
D3
C4
S2
D2
+
-
C1
S7
Load
S9
VDC
D1
C2
S1

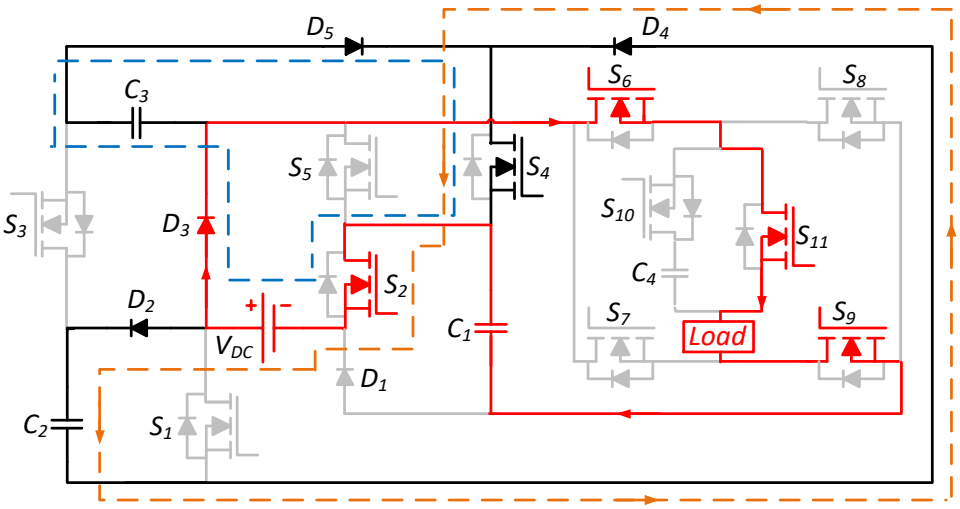
(b)


D5
D4
C3
S6
S8
S5
S4
S10
S11
S3
D3
C4
S2
D2
+
-
C1
S7
Load
S9
VDC
D1
C2
S1

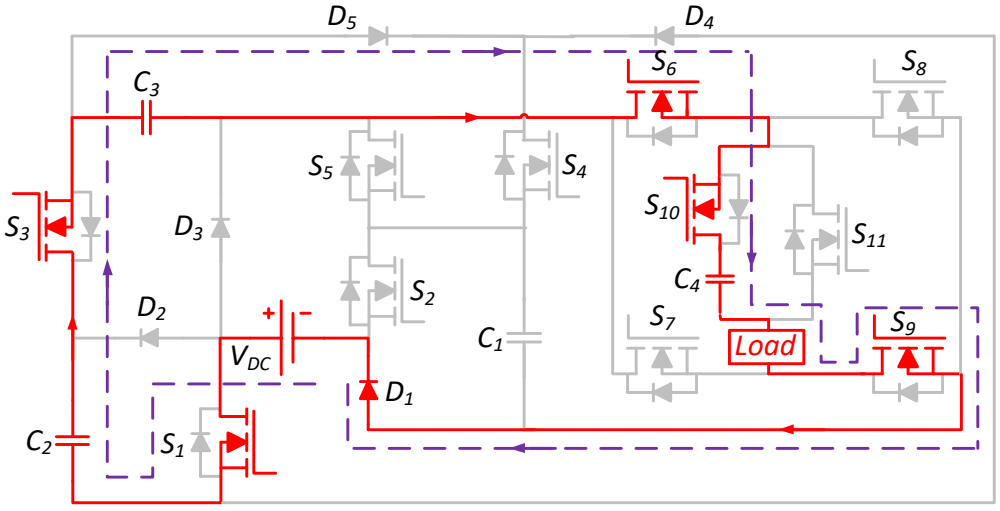
(c)


D5
D4
C3
S6
S8
S5
S4
S10
S11
D3
S2
C4
D2
VDC
C1
S7
Load
S9
D1
C2
S1

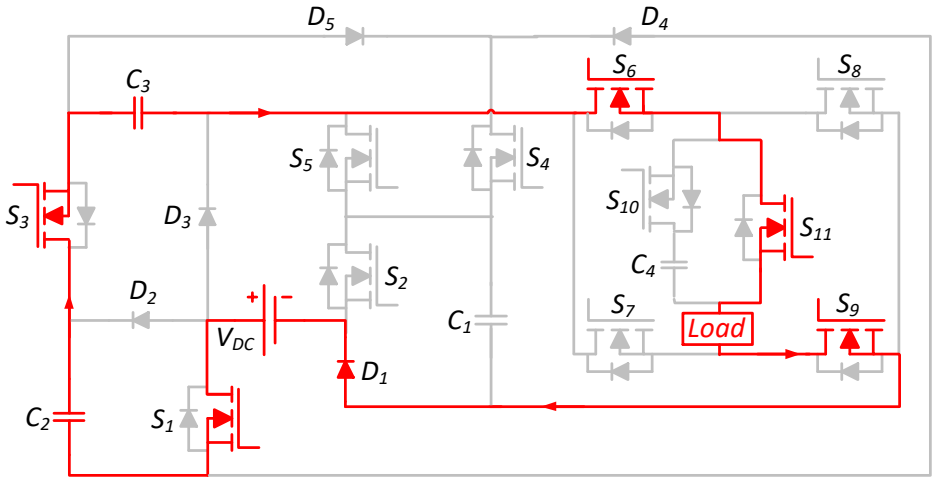
(d)


D5
D4
C3
S6
S8
S5
S4
S3
S10
S11
D3
S2
C4
D2
VDC
C1
S7
Load
S9
D1
C2
S1

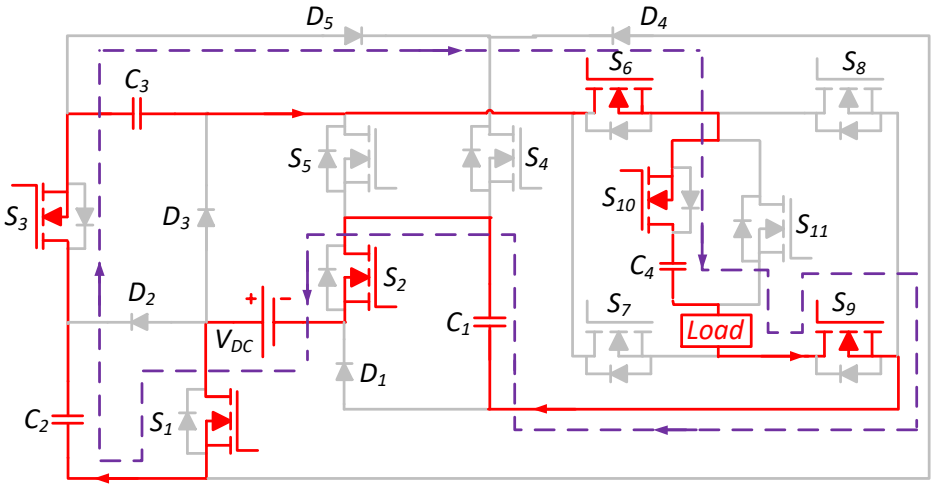
(e)


D5
D4
C3
S6
S8
S5
S4
S3
S10
S11
D3
S2
C4
D2
VDC
C1
S7
Load
S9
D1
C2
S1

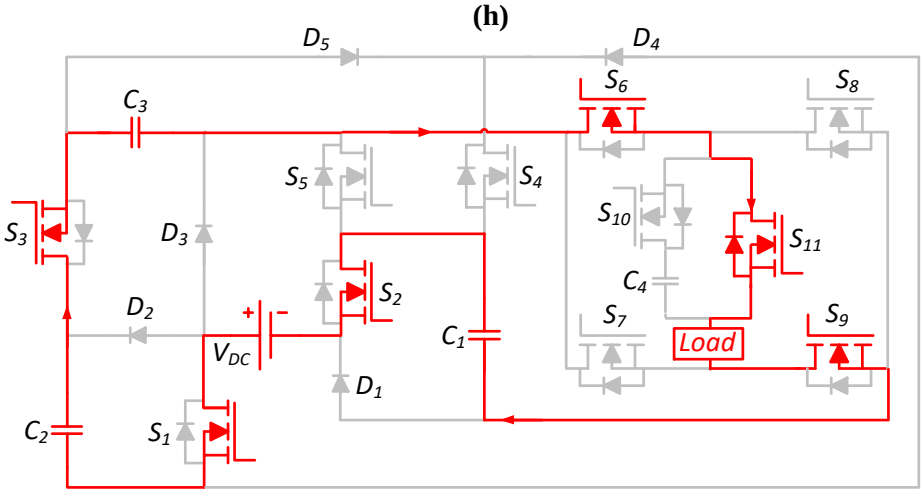
(f)



(g)



(h)



(i)

Fig. 5.3 Current flow for posituve voltage levels of the proposed 17-level DASC-MLI. (a) Current flow at voltage level zero. (b) Current flow at voltage level $V_{DC}/2$. (c) Current flow at voltage level V_{DC}. (d) Current flow at voltage level $3V_{DC}/2$. (e) Current flow at voltage level $2V_{DC}$. (f) Current flow at voltage level $5V_{DC}/2$. (g) Current flow at voltage level $3V_{DC}$. (h) Current flow at voltage level $V_{DC}/2$. (i) Current flow at voltage level $4V_{DC}$.

Level zero: Fig. 5.3(a) presents the current path for zero output voltage level. The capacitors C_2 and C_3 charge through D_2, D_4, S_4, S_2 and D_3, D_5, S_4, S_2 respectively in this interval.

Level $V_{DC}/2$: Fig. 5.3(b) shows the circuit configuration for generation of voltage level $V_{DC}/2$. The capacitors C_1 and C_4 charge through paths D_3, S_5, D_1 and D_3, S_6, S_{10}, S_9, D_1 respectively in this level. The reverse current passes through the switches S_{10}, S_6, S_5 and S_9.

Level V_{DC}: The circuit configuration for obtaining voltage V_{DC} across load is shown in Fig. 5.3(c). The capacitor C_1 charges in this interval through D_3, S_5 and D_1. The reverse current passes through the switches S_{11}, S_6, S_5 and S_9.

Level $3V_{DC}/2$: Fig. 5.3(d) shows the circuit configuration for voltage level $3V_{DC}/2$. All three capacitors C_2, C_3 and C_4 charge in this interval through charging paths D_2, D_4, S_4, S_2; D_3, D_5, S_4, S_2 and D_3, S_6, S_{10}, S_9, D_1 respectively. Capacitor C_1 discharges through D_3, S_6, S_{10}, S_9 and S_2 during this interval.

Level $2V_{DC}$: Fig. 5.3(e) shows the circuit configuration of voltage $2V_{DC}$. The capacitors C_2 and C_3 charge in this interval through D_2, D_4, S_4, S_2 and D_3, D_5, S_4, S_2. The capacitor C_1 discharges through D_3, S_6, S_{11}, S_9 and S_2.

Level $5V_{DC}/2$: Fig. 5.3(f) shows the circuit configuration for generation of voltage level $5V_{DC}/2$. The capacitors C_2 and C_3 are connected in series with the voltage source and discharge through S_1, S_3, S_6, S_{10}, S_9 and D_1. The capacitor C_4 is charged in this interval through the same path.

Level $3V_{DC}$: Fig. 5.3(g) shows the circuit configuration for output voltage $3V_{DC}$. The capacitors C_2 and C_3 are connected in series with the voltage source and discharge in this interval through path S_1, S_3, S_6, S_{11}, S_9 and D_1 to generate required output voltage.

Level $7V_{DC}/2$: Fig. 5.3(h) shows the circuit configuration of voltage level $7V_{DC}/2$. The capacitors C_1, C_2, and C_3 are connected in series with the voltage source and they discharge through S_1, S_3, S_6, S_{10}, S_9 and D_1 to generate $7V_{DC}/2$ output voltage. The capacitors C_4 charges in this interval through the same path.

Level $4V_{DC}$: Fig. 5.3(i) shows the circuit configuration for output voltage $4V_{DC}$. The capacitors C_1, C_2 and C_3 are connected in series with voltage source and they discharge through switches S_1, S_3, S_6, S_{11}, S_9 and S_2 to generate the required output voltage.

Similarly, output voltage levels for negative half cycle can be obtained through switching patterns given in Table 5.1.

PIV is a major factor in the selection of components for any MLI. In the proposed DASC-MLI, the switches S_6, S_7, S_8, S_9 suffer maximum stress, whereas the switches S_{10} and S_{11} suffer constant PIV of $V_{DC}/2$ irrespective of the number of levels. The PIV across the switches and diodes in the proposed for 17-level DASC-MLI is given in the Table 5.2.

Table 5.2
PIV across Switches for 17-level DASC-MLI

Device	PIV (×V_{DC})	Device	PIV (×V_{DC})
S_1, S_2	1	S_6, S_7, S_8, S_9	4
S_3	3/2	S_{10}, S_{11}	0.5
S_4	2	D_1, D_3, D_4, D_5	1
S_5	3	D_2	2

5.3 Extended Structure of Proposed 17-Level DASC-MLI

The extended structure of the proposed DASC-MLI can be obtained by adding a DASC unit consisting of one switch, one capacitor, and two diodes. Each such extended unit (m) adds 4 extra levels to the output voltage. The generalized (17+4m) level extended structure of the proposed DASC-MLI is shown in Fig. 5.4. One diode of each module is

connected through γ, while the other diode is connected through α. The switch and capacitors are connected through δ and β respectively as shown in Fig. 5.1. All the capacitor voltages in the proposed extended DASC-MLI are inherently self-balanced. For achieving higher voltage levels, the proposed DASC-MLI does not require any additional voltage source. Hence, the cost of the proposed DASC-MLI is considerably reduced for achieving higher voltage levels.

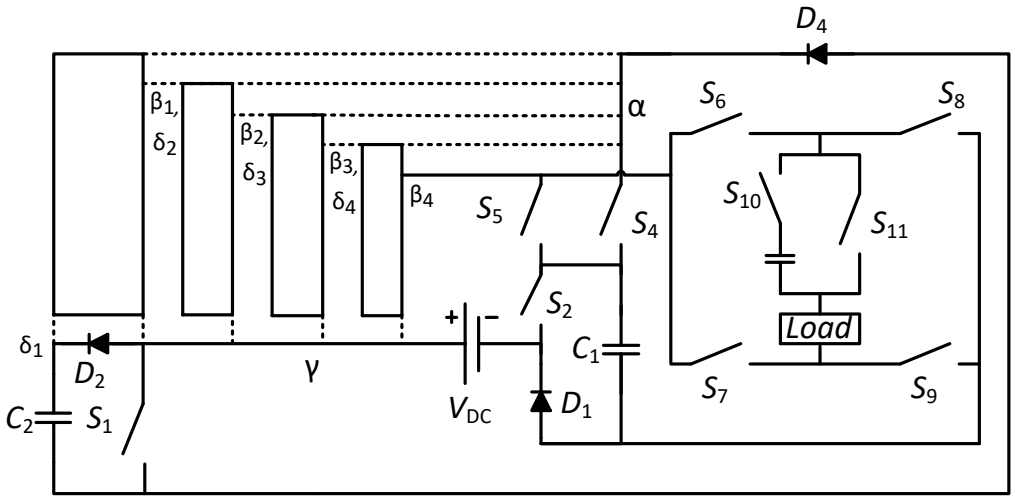


Fig. 5.4 Extension of proposed DASC-MLI.

5.3.1 Generalized Configuration of the Proposed DASC-MLI

The required number of active and passive components for generating $4n+1$ levels in the proposed generalized DASC-MLI (where n is the number of capacitors) can be calculated as:

$$\begin{cases} N_{\text{Switch}} = n+7 \\ N_{\text{Diode}} = 2n-3 \\ N_{\text{Source}} = 1 \end{cases} \tag{5.4}$$

where N_{Switch}, N_{Diode} and N_{Source} are the number of switches, diodes, and DC sources respectively. The TSV of the proposed DASC-MLI is calculated by adding the individual PIV of all switches. The TSV and TSV_{pu} of the generalized DASC-MLI are given as

$$\text{TSV} = \left(\frac{n^2 + 5n + 15}{2} \right) \cdot V_{\text{DC}} \tag{5.5}$$

$$\text{TSV}_{\text{pu}} = \left(\frac{n^2 + 5n + 15}{2n} \right) \cdot V_{\text{DC}} \tag{5.6}$$

5.4 Switching Scheme

Selective harmonic elimination technique using modified grew wolf optimization is used to generate the switching angles for the proposed DASC-MLI. The switching angles and output voltage levels of the proposed 17-level DASC-MLI are shown in Fig. 5.5. For proper operation of SC-MLI, the switching angles should satisfy the condition given as

$$0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 < \theta_6 < \theta_7 < \theta_8 < \theta_9 = \frac{\pi}{2} \tag{5.7}$$

The Fourier expansion of the quasi-square waveform of the output voltage for the proposed 17-level DASC-MLI is given as

$$V_0 = \frac{V_{\text{DC}}}{2\pi} \sum_{p=1,3,\cdots}^{\infty} \sum_{i=1}^{8} \frac{\cos(p\theta_i)}{p} \sin p\omega t \tag{5.8}$$

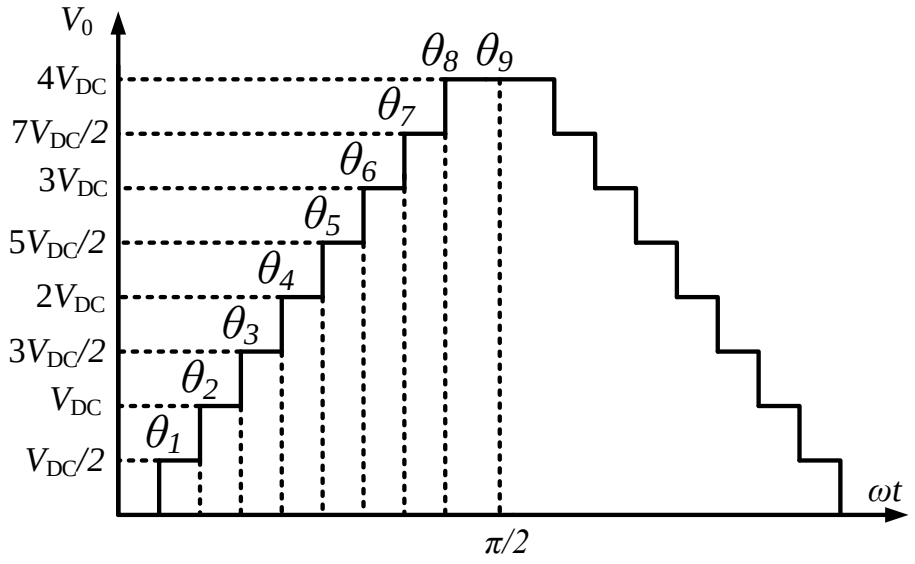


Fig. 5.5 Switching angles and output voltage levels of proposed 17-level DASC-MLI.

where ω is the angular frequency of the staircase output voltage waveform. The amplitude modulation index (M_{of}) of the fundamental output voltage waveform is expressed as:

$$M_{of} = \frac{1}{8}\sum_{i=1}^{8}\cos(\theta_i) \tag{5.9}$$

The switching angles for 17-level DASC-MLI θ_i (i = 1-8) are obtained using

$$\cos\theta_1 + \cos\theta_2 + \cos\theta_3 + \cos\theta_4 + \cos\theta_5 + \cos\theta_6 + \cos\theta_7 + \cos\theta_8 = 8M_{of}$$

$$\begin{aligned}&\cos(z\theta_1) + \cos(z\theta_2) + \cos(z\theta_3) + \cos(z\theta_4) + \cos(z\theta_5)\\ &+ \cos(z\theta_6) + \cos(z\theta_7) + \cos(z\theta_8) = 0\end{aligned} \tag{5.10}$$

where z is the number of harmonics. The harmonics such as 5th, 7th, 11th, 13th, 17th, 19th and 23rd are considered for obtaining the switching angles.

5.5 Capacitance Calculation

To calculate values of the capacitances, the charge-discharge cycle of each capacitor is considered [45]. For demonstration, the largest discharge period is calculated for C_1. The largest discharge interval and the corresponding currents through resistive load R_L for these intervals is calculated to define total charge and is shown in Table 5.3.

Table 5.3
Largest Discharge Interval for capacitor (C_1)

Interval	Current (i_0)
$\theta_3 \le \theta \le \theta_4$	$5V_{DC}/2R_L$
$\theta_4 \le \theta \le \theta_5$	$3V_{DC}/R_L$
$\theta_7 \le \theta \le \theta_8$	$7V_{DC}/2R_L$
$\theta_8 \le \theta \le \pi - \theta_8$	$4V_{DC}/R_L$

The maximum discharging value Q_{C_1} of the capacitor C_1 is calculated based on discharge cycles and is given as:

$$Q_{C_1} = \frac{1}{\omega}\left[\int_{\theta_3}^{\theta_4} i_o d\theta + \int_{\theta_4}^{\theta_5} i_o d\theta + \int_{\theta_7}^{\theta_8} i_o d\theta + \int_{\theta_8}^{\pi-\theta_8} i_o d\theta\right] \tag{5.11}$$

Similarly, maximum discharging values Q_{C_2}, Q_{C_3}, Q_{C_4} of the capacitors C_2, C_3, C_4 can be obtained. The maximum allowable voltage ripples across the capacitor C_i is kV_{C_i} (i=1, 2, 3 and 4), where k is the ripple factor. Using the derived values of Q_{C_1}, Q_{C_2}, Q_{C_3} and Q_{C_4} the values of capacitors C_1, C_2, C_3 and C_4 are obtained as:

$$C_1 \geq \frac{\left(4\pi - 3\theta_3 - \theta_4 + 4\theta_5 - 7\theta_7 - \theta_8\right)}{2\pi f_S k R_L} \tag{5.12}$$

$$C_2, C_3 \geq \frac{\left(4\pi - 5\theta_5 - \theta_6 - \theta_7 - \theta_8\right)}{2\pi f_S k R_L} \tag{5.13}$$

$$C_4 \geq \frac{\left(\theta_2 - \theta_1 - 3\theta_3 + 3\theta_4 - 5\theta_5 + 5\theta_6 - 7\theta_7 + 7\theta_8\right)}{2\pi f_S k R_L} \tag{5.14}$$

For the resistive-inductive loading condition, the function of load current, $I_L(t)$ can be derived as

$$I_L(t) = I_{max} \sin(\omega t - \phi) \tag{5.15}$$

here I_{max} is the maximum value of load current, and ϕ is the output phase difference. The net charge can then be obtained. Substituting the charge to obtain capacitance yields

$$C_1 \geq \frac{2I_{max}\begin{pmatrix}\cos(\theta_3 - \Phi) + \cos(\theta_7 - \Phi) \\ -\cos(\theta_5 - \Phi) - \sin(\Phi)\end{pmatrix}}{2\pi f_S k V_{DC}} \tag{5.16}$$

$$C_2, C_3 \geq \frac{2I_{max}\left(\cos(\theta_5 - \Phi) - \sin(\Phi)\right)}{2\pi f_S k V_{DC}} \tag{5.17}$$

$$C_4 \geq \frac{I_{max}\begin{pmatrix}\cos(\theta_4 - \Phi) - \cos(\theta_3 - \Phi) + \cos(\theta_2 - \Phi) \\ -\cos(\theta_1 - \Phi) + \cos(\theta_6 - \Phi) - \cos(\theta_5 - \Phi) \\ +\cos(1.5\pi) - \cos(\theta_7 - \Phi)\end{pmatrix}}{2\pi f_S k V_{DC}} \tag{5.18}$$

Assuming voltage ripple k = 0.05 and 0.1, the optimal capacitor values can be determined. From (5.16)-(5.18), it can be observed that the optimum values of capacitors inversely vary with the ripple factor, and output frequency. To demonstrate the effect of load resistance on the optimum capacitance values, the variations of C_1, C_2, C_3 and C_4 with different ranges of output load, R_L are shown in Fig. 5.6(a). The optimal values of capacitors are calculated for different values of phase angle and are shown in Fig. 5.6(b).

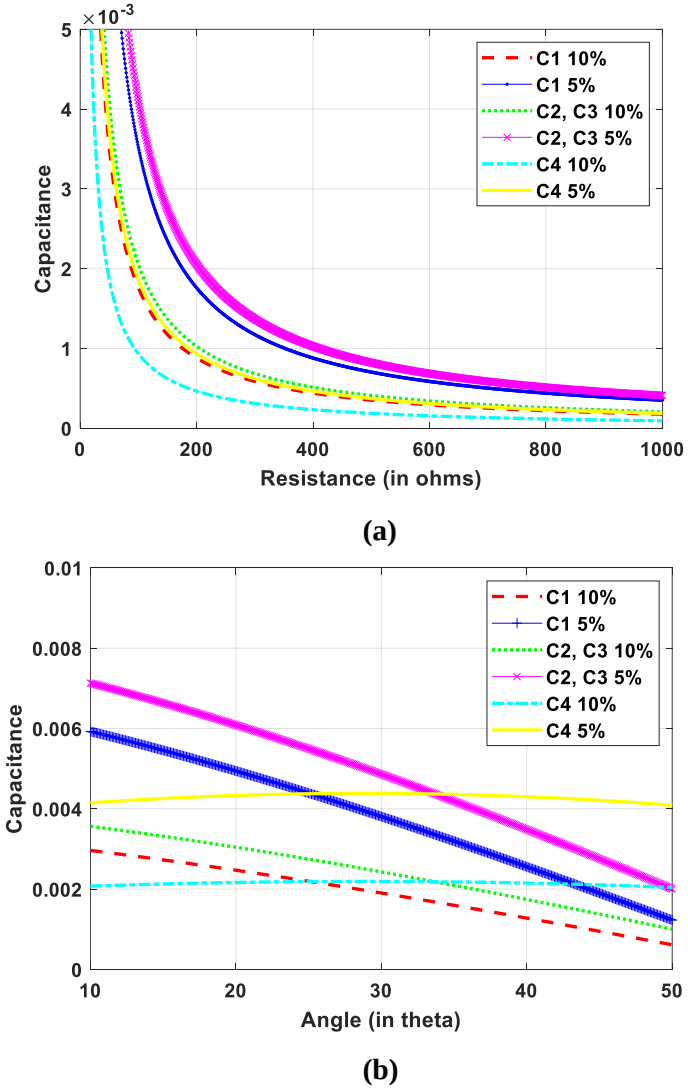


Fig. 5.6 Values of capacitance of all capacitors. (a) under different load resistance. (b) under different phase angles.

5.6 Conduction Loss of the Proposed DASC-MLI

The conduction losses, P_C in the proposed DASC-MLI can be attributed to two factors: steady state conduction losses and the charging state conduction losses. The steady state

conduction loss (CL), $P_{CL,SS}$ can be calculated by summing loss across each circuit element (diode, Switch, etc.) and $F_{j,}$ (j=1,.., J) incurred at each voltage level $U_{q,}$ (q=1,.., Q).

$$P_{CL,SS} = \sum_{q=1}^{Q}\sum_{j=1}^{J} P_{CL,SS,F_j,U_q} \tag{5.19}$$

here J and Q are the total number of elements and voltage levels respectively. The conduction loss, P_{CL,SS,F_j,U_q} at each level U_q for each element F_j can further be generalized as the sum of losses experienced due to on-state voltage drop at j^{th} component and their on-state resistances. This loss can be presented as

$$P_{CL,SS,F_j,U_q} = \begin{pmatrix} V_{on,F_j,U_q}.i_{load,avg,SS,F_j,U_q} \\ +R_{on,F_j,U_q}.i^2_{load,rms,SS,F_j,U_q} \end{pmatrix} \tag{5.20}$$

The charging state (CS) conduction losses (CL), $P_{CL,\,CS}$ occur due to charging currents superimposing the steady state current while charging capacitors. This charging current, $i_{CL,CS,F_j,U_q}(t)$ and its associated losses can be drastically reduced using a very small inductor (L_S) and a very small resistor (R_S) in series with the input source. The inclusion of this impedance at source side transforms the circuit into a series RLC circuit. Assuming series RLC circuit, the instantaneous current flowing through any element F_j, at any level U_q can be easily calculated as

$$i_{CL,CS,F_j,U_q}(t) = e^{\frac{-t.R_{eq,\,U_q}}{L_S}}.\left(I_{q-1}\cos(\lambda t) - \frac{I_{q-1}R_{eq,L_q}}{2.\lambda.L_S}\sin(\lambda t) - \frac{\Delta V}{\lambda.L_S}\sin(\lambda t) \right) \tag{5.21}$$

where

$$\lambda = \sqrt{\frac{1}{L_S.C_{\text{eq,U}_q}} - \left(\frac{R_{\text{eq,U}_q}}{2.L_S}\right)^2} \tag{5.22}$$

where $C_{\text{eq.}}$ and $R_{\text{eq.}}$ are the equivalent capacitance and resistance respectively in the charging loop including source resistance R_S. The ΔV is the difference between the capacitor voltage at beginning of level Uq. For each element F_j at level U_q, this current would generate conduction losses of magnitude:

$$P_{\text{CL,CS,F}_j,\text{ U}_q} = \left(\int_{t_{U_q,begin}}^{t_{U_q,end}} R_{\text{on, F}_j,\text{U}_q}.i^2_{\text{CL,CS, F}_j,\text{ U}_q}.dt + \int_{t_{U_q,begin}}^{t_{U_q,end}} V_{\text{on, F}_j,\text{U}_q}.i_{\text{CL,CS, F}_j,\text{ U}_q}.dt \right) \tag{5.23}$$

where, $t_{U_{q,begin}}$ and $t_{U_{q,end}}$ are the beginning and ending time of output voltage level Uq. The total CS-CL losses can be calculated like SS-CL by adding losses across each element:

$$P_{\text{CL,CS}} = \sum_{q=1}^{Q}\sum_{j=1}^{J} P_{CL,CS,F_j,U_q} \tag{5.24}$$

Since, it is mathematically difficult to accurately predict voltage at each instant of time due to several components involved, for ease in calculation of losses, ΔV is approximated to its maximum value of $0.1V_{\text{DC}}$.

5.7 Switching Loss Calculation

The switching loss occurs due to charging and discharging of parasitic capacitances of switches during the turn on and turn off of switches in a cycle [51]. The switching loss during turn on $P_{\text{sw, }i\text{(on)}}$ and turn off $P_{\text{sw, }i\text{(off)}}$ are given as

$$P_{\text{sw},\,i\,(\text{on})} = \frac{1}{6} f_{sw,i} V_{\text{sw},i} I_i t_{on} \tag{5.25}$$

$$P_{\text{sw},\,i\,(\text{off})} = \frac{1}{6} f_{sw,i} V_{\text{sw},i}\, I_i^{'} t_{off} \tag{5.26}$$

where $V_{\text{sw},\,i}$ is the off-state voltage of the i^{th} switch, I_{i} is the current of the i^{th} switch when the switch is turned on, I_{i}' is the current of the i^{th} switch before the turn off of the switch, t_{on} is the duration when the switch is turned on, t_{off} is the duration when the switch is turned off, and f_{sw} is the switching frequency. To calculate total switching loss, the number of N_{on} and the number of N_{off} switching states per one cycle is multiplied by (5.25) and (5.26). The total switching loss is calculated for each level and added as follows:

$$P_S = \sum_{i=1}^{17} \left(\sum_{j=1}^{N_{on}(i)} P_{\text{sw,on(ij)}} + \sum_{j=1}^{N_{off}(i)} P_{\text{sw,off(ij)}} \right) \tag{5.27}$$

Using (5.27), the total switching loss of the proposed 17-level DASC-MLI is obtained as:

$$P_{\text{S}} = \frac{54 V_{DC}^2}{R_L} f_S t_{on} + \frac{53.5 V_{DC}^2}{R_L} f_S t_{off} \tag{5.28}$$

5.8 Ripple Loss Analysis

The ripple loss occurs at the time of charging of capacitors at different switching instances. The voltage ripple of capacitors is obtained as

$$\Delta V_{Ci} = \frac{1}{C_i} \int_{t}^{t'} i_{c_i}(\text{t}).dt \tag{5.29}$$

where i_{c_i} is the capacitor current and $t - t'$ is the charging interval. The ripple voltages of capacitors C_1, C_2, C_3 and C_4 are given as

$$\Delta V_{C1} = \frac{V_{dc}}{2\pi f_S R_L C_1}\left(4\pi - 3\theta_3 - \theta_4 + 4\theta_5 - 7\theta_7 - \theta_8\right) \tag{5.30}$$

$$\Delta V_{C2}, \Delta V_{C3} = \frac{V_{dc}}{2\pi f_S R_L C_2}\left(4\pi - 5\theta_5 - \theta_6 - \theta_7 - \theta_8\right) \tag{5.31}$$

$$\Delta V_{C4} = \frac{V_{dc}}{2\pi f_S R_L C_4}\left(\theta_2 - \theta_1 - 3\theta_3 + 3\theta_4 - 5\theta_5 + 5\theta_6 - 7\theta_7 + 7\theta_8\right) \tag{5.32}$$

The ripple loss in one cycle operation of the output voltage is given as

$$P_{\mathrm{R}} = \frac{1}{2T}\sum_{i=1,2,3,4} C_i \Delta V_i^2 \tag{5.33}$$

where C_{i} and ΔV_i are the i^{th} capacitor and ripple voltage of it.

The efficiency of the proposed DASC-MLI can be written as:

$$\eta = \frac{P_0}{P_0 + P_C + P_S + P_R} \tag{5.34}$$

where P_0, P_{C}, P_{S} and P_{R} are the output power, conduction, switching and ripple losses respectively.

5.9 Comparison with Other Reported topologies

In this section, the proposed DASC-MLI is compared with other reported SC-MLIs in terms of used capacitors, switches, diodes, TSV, PIV, boosting factor and cost function (CF). It can be observed from Fig. 5.7(a) that the proposed DASC-MLI requires lesser number of capacitors to utilize the same levels as compared to other selected MLIs. The DASC-MLI uses lower number of switches compared to other recently proposed topologies like symmetric topology in [44] and switched-capacitor topology in [42] as

shown in Fig. 5.7(b). Topologies presented in [43] possess large TSV for higher levels, whereas topology [40] requires much more diodes to achieve same voltage levels. The topology given in [41] and [45] requires a greater number of switches as compared to proposed DASC-MLI. The TSV and number of capacitors required in [46] are also very high. Table 5.4 also gives the comparison of different reported SC-MLIs and the proposed DASC-MLI in for 17-level SC-MLI. The generalized graphical representations of TSV and number of diodes versus voltage levels for different SC-MLI topologies are shown in Fig. 5.7(c) and (d) respectively. A CF has been further used to demonstrate potentiality of proposed DASC-MLI compared to other reported SC-MLIs and is given as [54]

$$\mathrm{CF} = N_{\mathrm{switch}} + N_{\mathrm{cap}} + N_{\mathrm{diode}} + TSV_{\mathrm{pu}} \tag{5.35}$$

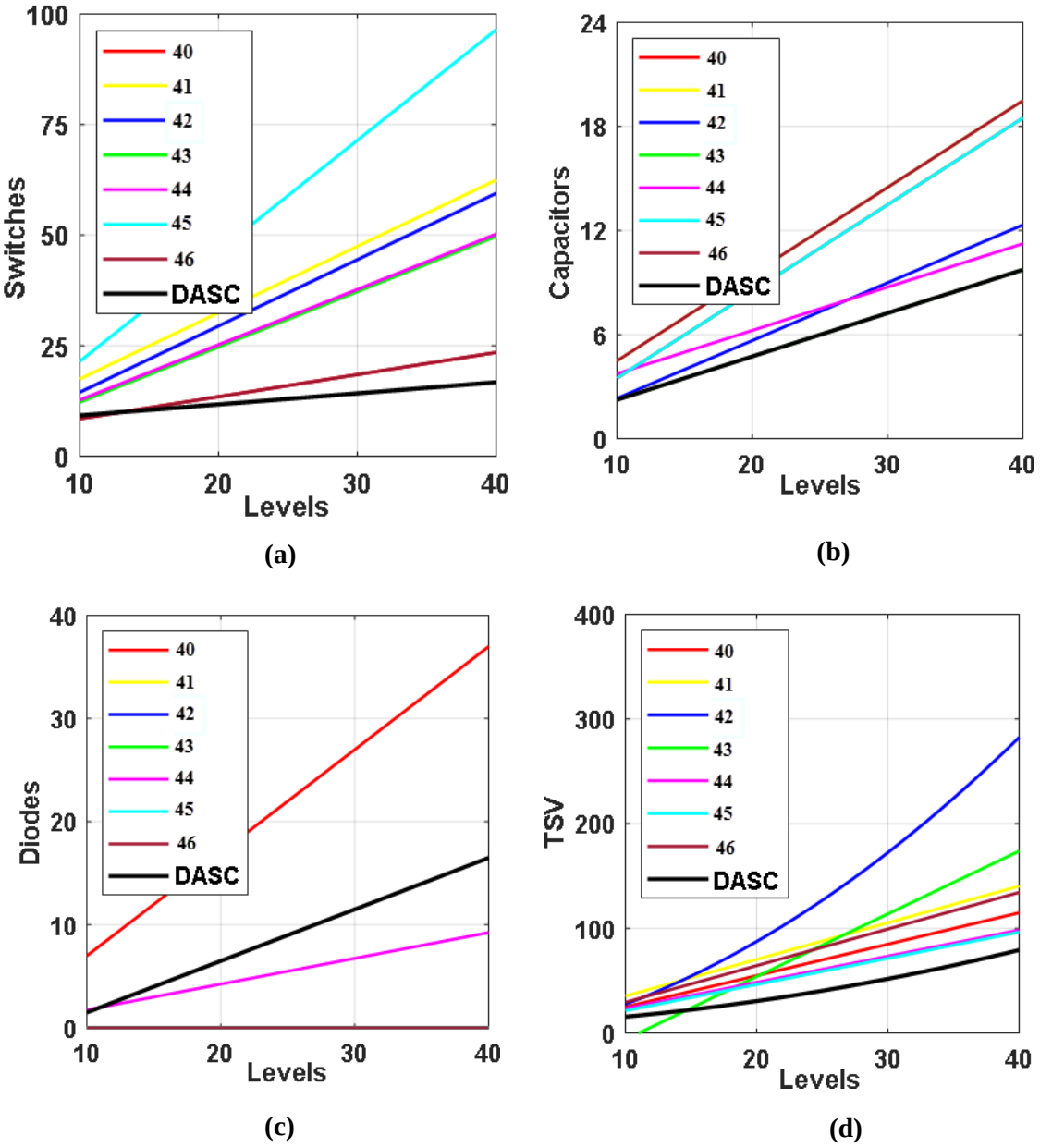
where N_{switch}, N_{cap} and N_{diode} are the number of switches, capacitors and diodes, respectively.

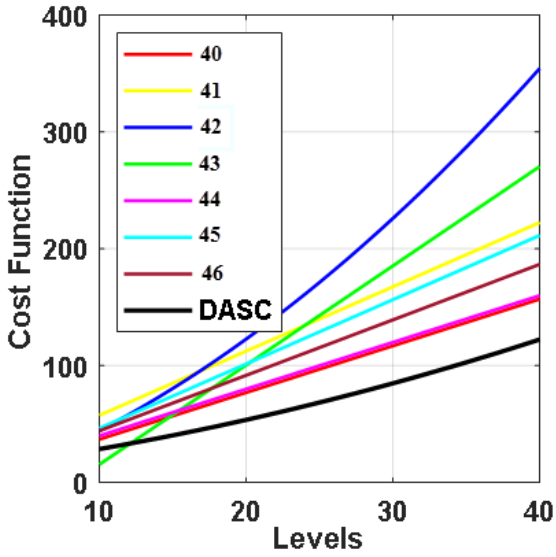
Table 5.4
Comparison of proposed 17-level DASC-MLI with Other Recent SC-MLI Topologies

Param.	**[45]**	**[42]**	**[40]**	**[41]**	**[46]**	**[43]**	**[44]**	**DASC-MLI**
N_{Switch}	39	25	12	25	12	23.5*	23.5*	11
N_{Cap}	7	7	7	7	8	4.5*	5.5*	4
N_{Diode}	0	0	14	0	0	0	3.5*	5
TSV_{sw}	39	72	96	53	54	48	41	25.5
TSV_{diode}	0	0	28	0	0	0	3.5	6
TSV_{total}	39	72	126	53	54	48	44.5	31.5
PIV	1	8	8	8	4	8	2	4
Boost factor	8	8	8	8	8	14	4	4
Extend-ability	Y	Y	Y	Y	Y	Y	Y	Y

* **as per the generalization provided in paper**

The generalized graphical representations of CF versus voltage levels for different SC-MLI topologies are shown in Fig. 5.7(e). It can be observed that the cost of the proposed DASC-MLI is reduced as compared to other reported SC-MLIs. When operated at same boosting factor, the proposed DASC-MLI requires lower number of switches at same number of voltage levels. If the proposed DASC-MLI has greater TSV at same boosting ratio, then the number of levels generated is almost twice those generated by other SC-MLI topologies, thus verifying the lower TSV and component count at higher voltage levels of the proposed DASC-MLI.





(e)

Fig. 5.7 Comparison of the proposed DASC-MLI with recent topologies. (a) Number of required sources versus levels. (b) Number of required switches versus levels. (c) TSV versus number of levels. (d) Diode versus number of levels CF. (e) Cost function versus number of levels of different topologies.

5.10 Simulation Studies

The performance of the proposed DASC-MLI is validated through a 550 W MATLAB/Simulink model. Modulation index is taken as 0.75 in this study. The output voltage V_0 and current I_0 waveforms of the proposed 17-level DASC-MLI for a resistive load (R = 40 Ω) are shown in Fig. 5.8(a). The measured rms values of voltage and current are 155.4 V and 3.42 A respectively at 50 Hz frequency. For R-L load (R = 40 Ω, L = 100 mH), output voltage V_0 and current I_0 are shown in Fig. 5.8(b) and measured as 155.4 V and 3.38 A respectively. The capacitor voltages are shown in Fig. 5.9. It can be observed that capacitor voltages V_{C1}, V_{C2}, V_{C3} and V_{C4} are balanced at 60 V, 60 V, 60 V and 30 V respectively. The voltage stresses across four switches (S_1, S_2, S_3 and S_4) of the proposed DASC-MLI are shown in Fig. 5.10(a) and are measured as 60 V, 60 V, 90 V and 120 V respectively. The voltage stresses across switches (S_5, S_{10} and S_{11}) are shown in Fig. 5.10(b) and are also measured as 180 V, 30 V and 30 V respectively. Similar, the voltage stresses across each switch (S_6, S_7, S_8 and S_9) of the H-bridge are 240 V respectively, as shown in Fig. 5.10(c).

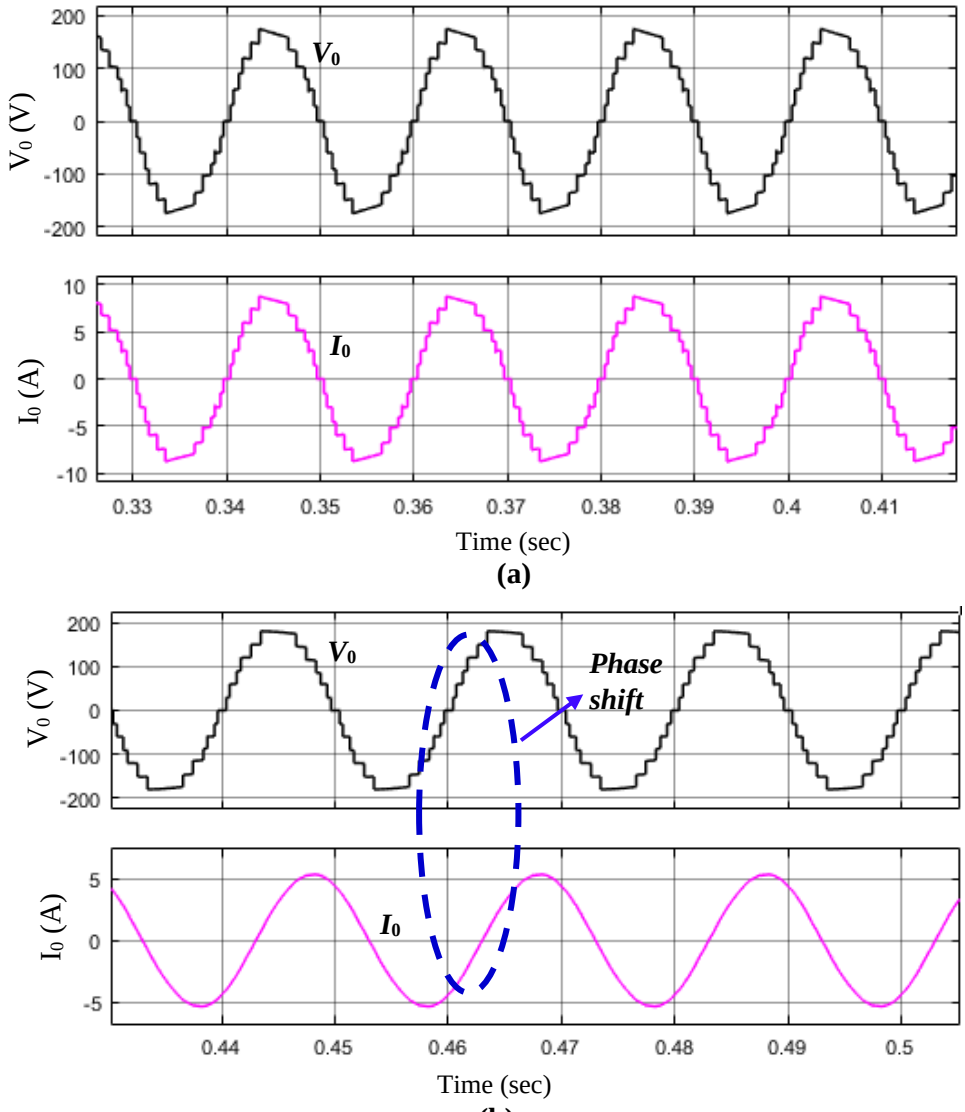


Fig. 5.8 Simulation results of the proposed DASC-MLI. (a) Output voltage (V_o) and current (I_o) for *R* load (R= 40 Ω). (b) Output voltage (V_o) and current (I_o) for *R-L* load (R= 40 Ω, L= 100 mH.

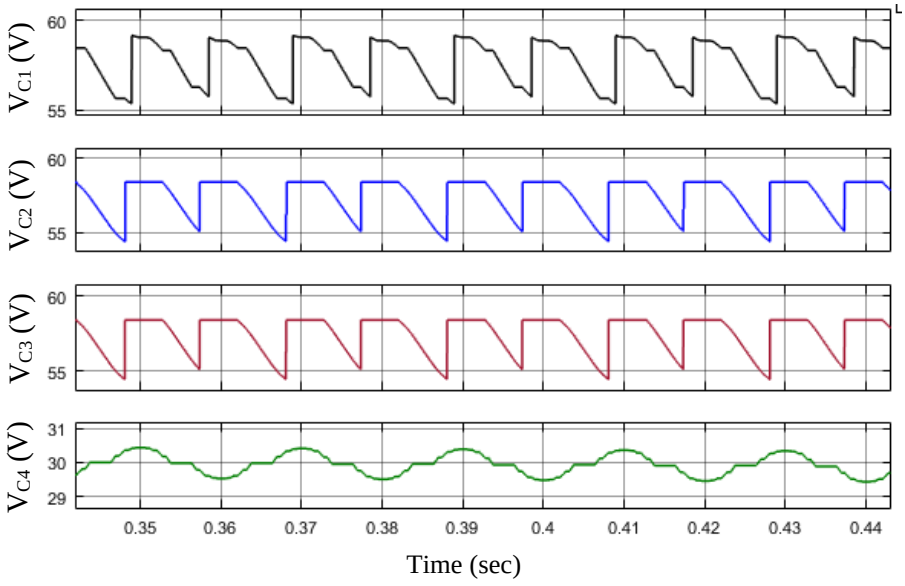


Fig. 5.9 Simulation results of capacitor voltages. (V_{C1}, V_{C2}, V_{C3}, V_{C4}).

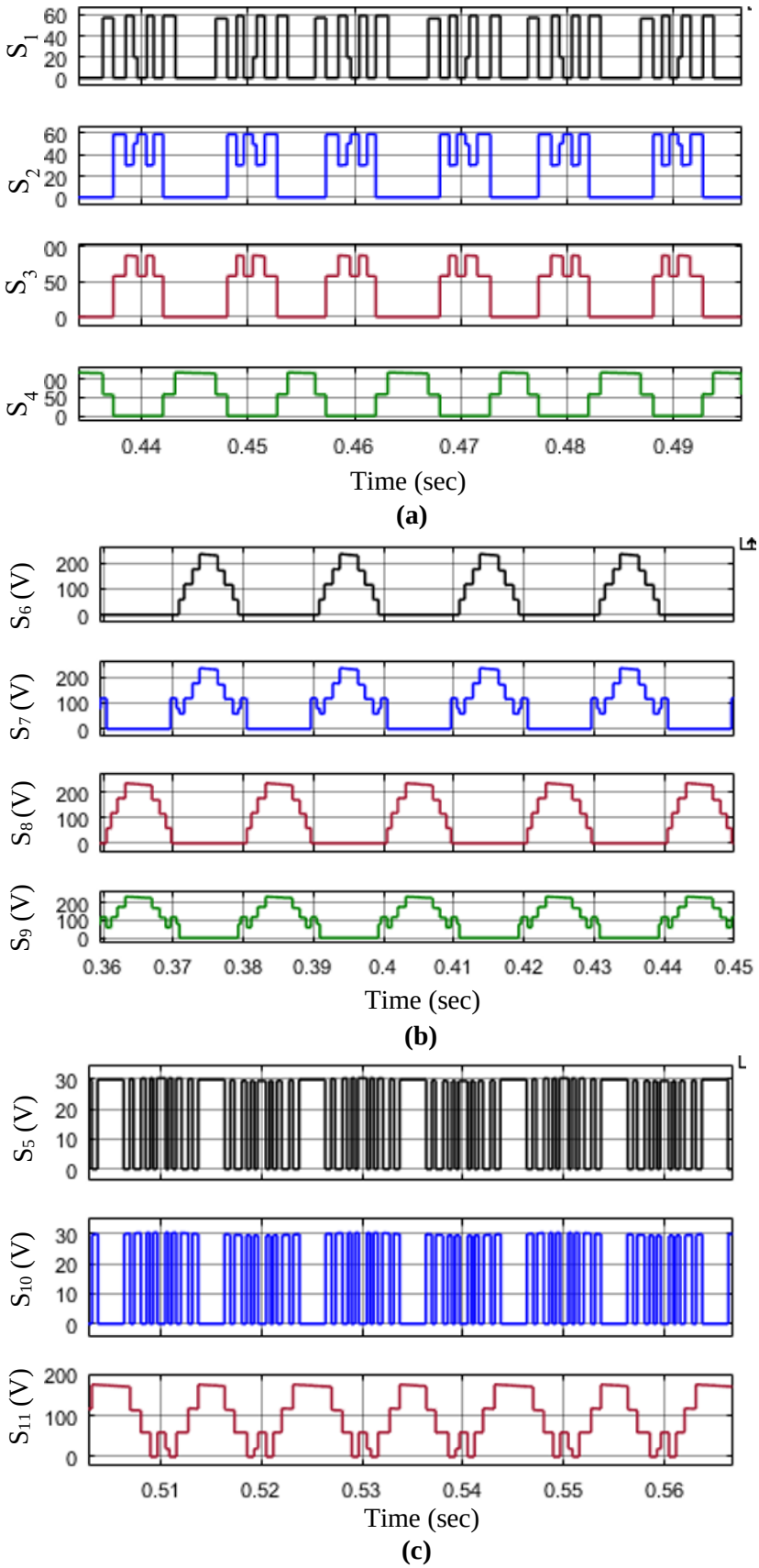


Fig. 5.10 Voltage stress of the proposed DASC-MLI. (a) Voltage stresses across switches (S_1, S_2, S_3, S_4). (b) Voltage stresses across switches (S_5, S_{10}, S_{11}). (c) Voltage stresses across switches (S_6, S_7, S_8, S_9).

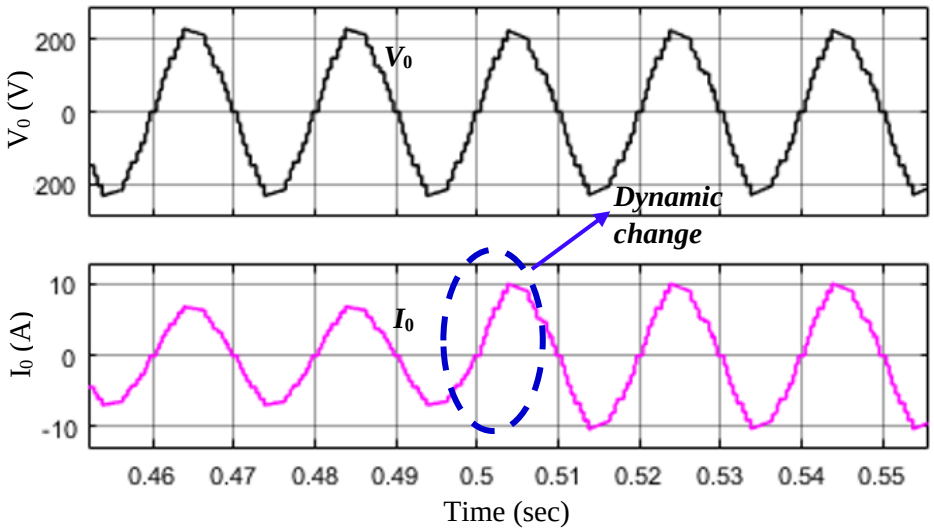


Fig. 5.11 Dynamic performance of the proposed SC-MLI for step-down change in load resistance.

The load resistance is step changed from 70 Ω to 35 Ω to observe the dynamic behaviour of the DASC-MLI. The load current is changed from 3.5 A to 7 A due to step change in resistance and is shown in Fig. 5.11. It can be observed that the load change does not have any effect on the output voltage waveform. Hence, it confirms the self-voltage balance of capacitors in the proposed DASC-MLI.

5.11 Experimental Validation of DASC-MLI

The performance of the proposed DASC-MLI is validated through a 570 W experimental prototype as shown in Fig. 5.12. The parameters used in experiment are listed in Table 5.5.

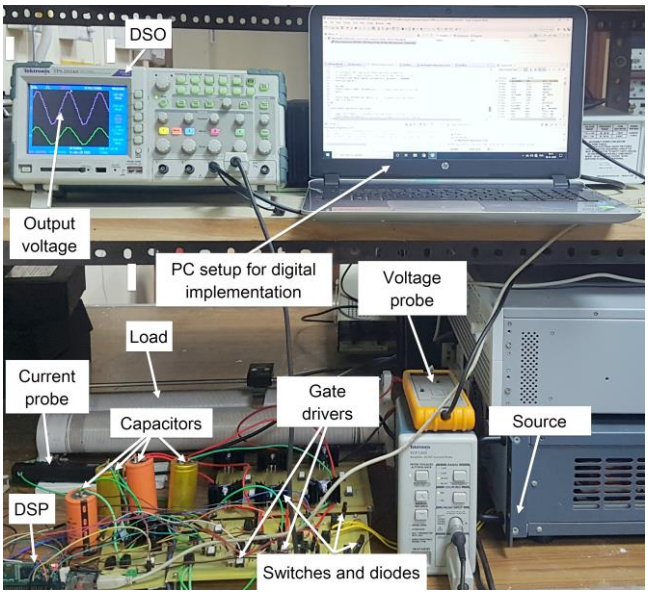


Fig. 5.12 Photograph of experimental prototype of 17-level DASC-MLI.

Table 5.5
Devices and Parameters Used for Experimentation

Microcontroller	TI-TMS320F28335
IGBT	HGTG12N60A4D
Gate Driver	FOD3184
Diode	STP516150
Electrolytic Capacitors	2200µF (C_1, C_2) and 1800 µF (C_3, C_4)

5.11.1 Steady State Performance

The steady state performance of DASC-MLI is investigated in this section. The DC source voltage V_{dc} is taken as 60 V and the experimentation has been carried out using TI-TMS320F28335 DSP processor.

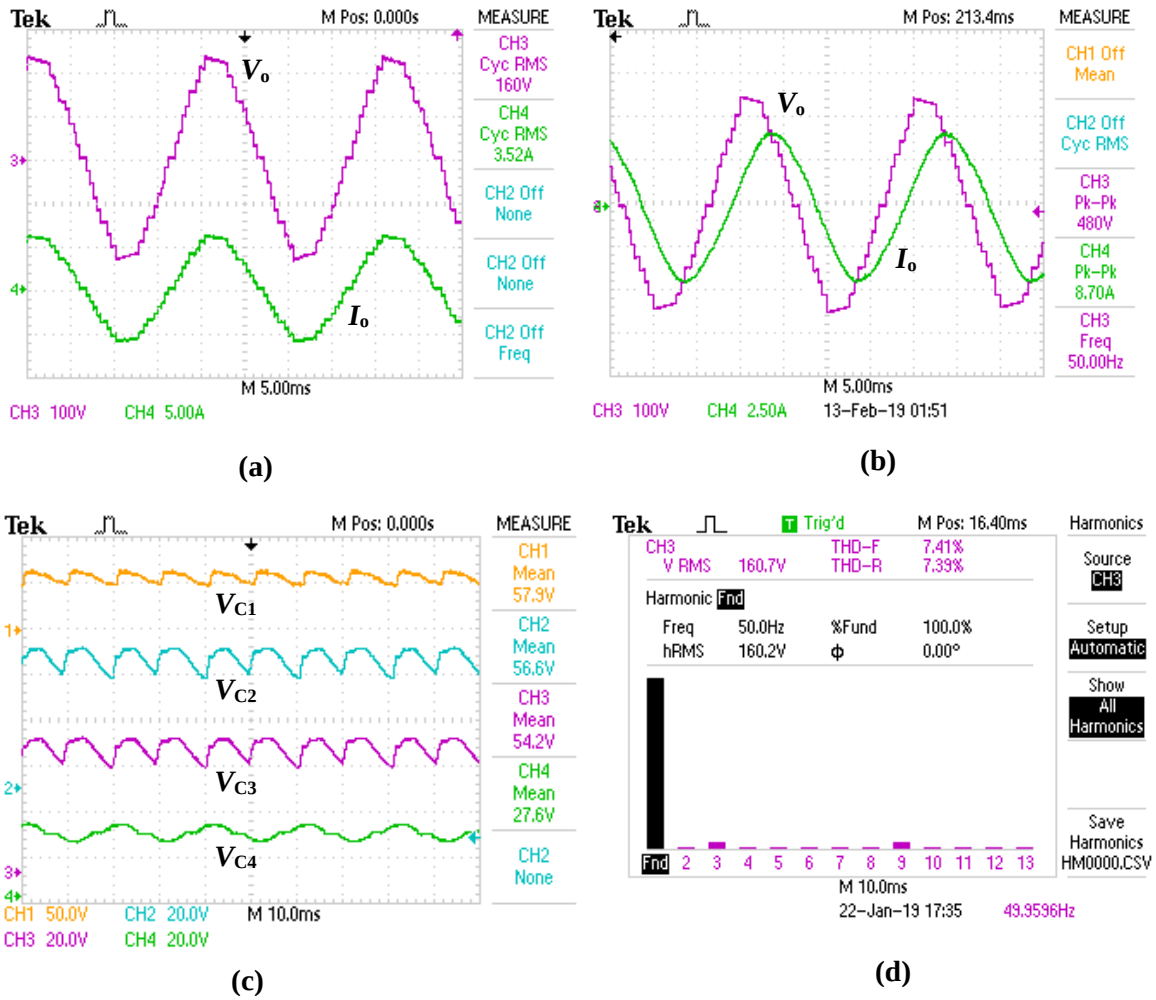


Fig. 5.13 Experimental results of the proposed DASC-MLI. (a) Output voltage (V_o) and current (I_o) for R load (R= 40 Ω). (b) Output voltage (V_o) and current (I_o) for R-L load (R= 40 Ω, L= 100 mH). (c) Capacitor voltages (V_{C1}, V_{C2}, V_{C3}, V_{C4}). (d) Harmonic spectrum of V_o.

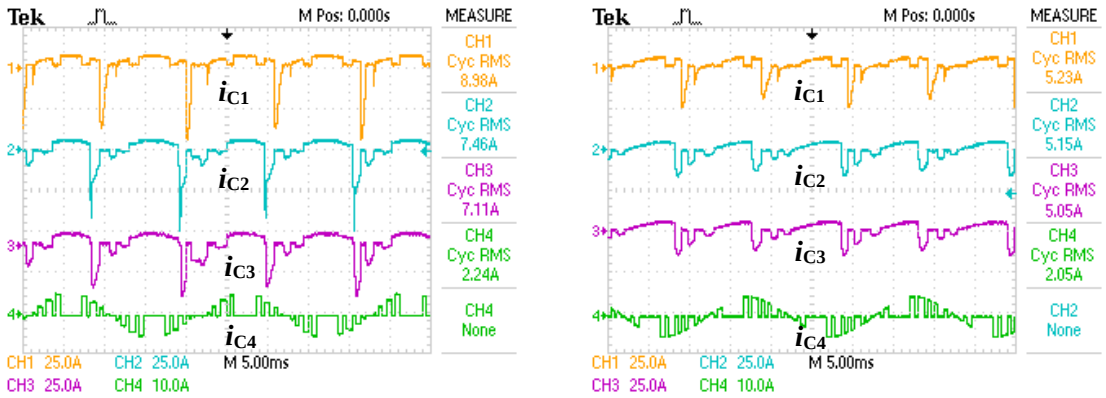


Fig. 5.14 Experimentally results of capacitor currents of DASC-MLI. (a) Capacitor currents i_{C1}, i_{C2}, i_{C3}, and i_{C4} for $R = 40\ \Omega$. (b) Capacitor currents i_{C1}, i_{C2}, i_{C3} and i_{C4} for $R = 40\ \Omega$, $L = 100$ mH.

Fundamental switching strategy (50 Hz) is used and the value of M_{of} is taken as 0.75. The output voltage V_0 and current I_0 waveforms for a resistive load ($R = 40\ \Omega$) are shown in Fig. 5.13(a). The measured rms values of voltage and current are 154.7 V and 3.38 A at 50 Hz frequency respectively. For *R-L* load ($R = 40\ \Omega$, $L = 100$ mH), output voltage V_0 and current I_0 are shown in Fig. 5.13(b) and measured as 154.1 V and 3.17 A respectively. The capacitor voltages are shown in Fig. 5.13(c). It can be observed that capacitor voltages V_{C1}, V_{C2}, V_{C3} and V_{C4} are balance at 56.5 V, 56 V, 54.2 V and 27 V respectively. The ripples voltage ΔV_{C1}, ΔV_{C2}, ΔV_{C3} and ΔV_{C4} of capacitors are 4 V, 4.4 V, 5.9 V and 2.3 V respectively. The harmonic spectrum of the output voltage V_0 is shown in Fig. 5.13(d) and output voltage THD is measured as 7.41%. To verify the proper charge balance in capacitors, the respective capacitor currents for *R* and *R-L* load are shown in Fig. 5.14(a)-(b). The measured rms values of current in case of *R* load ($R = 40\ \Omega$) for capacitors C_1, C_2, C_3 and C_4 are 4.27 A, 4.10 A, 4.25 A and 2.64 A respectively as shown in Fig. 5.14(a). Similarly, for *R-L* load ($R = 40\ \Omega$ and $L = 100$ mH), the measured rms value of capacitors are 4.35 A, 3.31 A, 3.58 A and 2.63 A respectively as shown in Fig. 5.14(b). The voltage stresses across four switches (S_1, S_2, S_3 and S_4) of the proposed DASC-MLI are shown in Fig. 5.15(a) and are measured as 60 V, 60 V, 92 V and 120 V

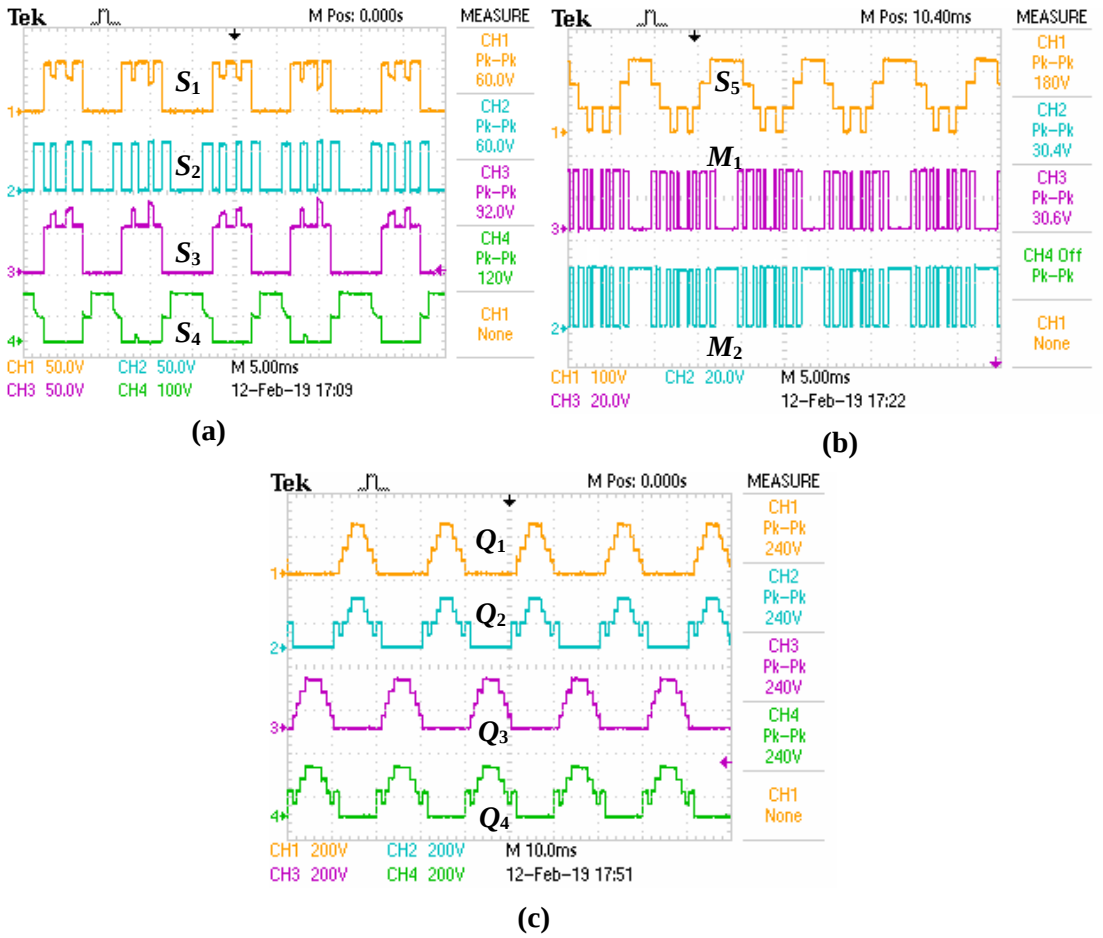


Fig. 5.15 Experimental results of voltage stress of DASC-MLI. (a) Voltage stresses across switches (S_1, S_2, S_3, S_4). (b) Voltage stresses across switches (S_5, M_1, M_2). (c) Voltage stresses across switches (Q_1, Q_2, Q_3, Q_4).

respectively. The voltage stresses across switches (S_5, M_1 and M_2) are shown in Fig. 5.15(b) and are measured as 180 V, 30.4 V and 30.6 V respectively. Similarly, the voltage stresses across switches (Q_1, Q_2, Q_3 and Q_4) of the H-bridge are 240 V, as shown in Fig. 5.15(c). Peak charging current is common in DASC-MLIs and to alleviate the current spikes, and reduce the device stresses, several strategies are discussed in literatures [47], [48] and [52]. Reducing spikes by increasing switching frequency is given in [47]. Literature [48] discusses the alleviation of spikes by increasing capacitance value. Using resistors [52] or inductors at source also reduces the spikes. In the proposed work, a small inductor and a small resistor at the source is used to reduce the current spikes. The switch and device current stress analysis is carried out for load resistance R= 40 Ω, input resistor R= 0.15 Ω and input inductor L=35 µH.

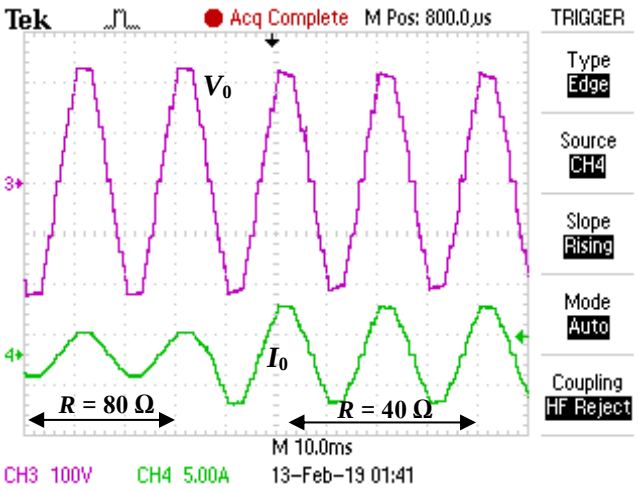


Fig. 5.16 Experimental verification of dynamic performance of DASC-MLI for step-up change in load resistance.

5.11.2 Dynamic Performance

The dynamic performance of the proposed RV-SCMLI is investigated in this section. The load resistance is step changed from 80 Ω to 40 Ω to observe the dynamic performance of the DASC-MLI. The load current is changed from 1.8 A to 3.6 A due to step change in resistance and is shown in Fig. 5.16. From Fig. 5.16, it can also be observed that the load change has no effect on the output voltage waveform, which confirms the self-voltage balancing of capacitors in DASC-MLI.

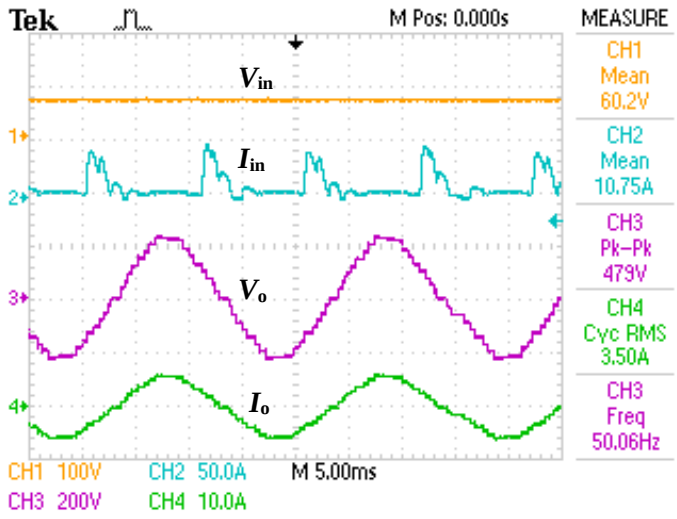


Fig. 5. 17 Input voltage, current and output voltage, current for *R* load (*R* = 40Ω) of DASC-MLI.

5.11.3 Calculation of Efficiency

The conduction loss, switching loss and ripple loss are calculated using (5.24), (5.28) and (5.33) and are 16.75 W, 5.37 W and 6.23 W respectively. The experimental efficiency of the proposed DASC-MLI is also calculated. To determine the efficiency (η) of the proposed DASC-MLI; input voltage V_{in}, input current I_{in}, output voltage V_o and output current I_o are measured experimentally for R load from Fig. 5.17. For R load (R= 40 Ω), the measured input power, output power and loss are P_{in} = 580.15 W, P_{out} =543.47 W and P_{loss} = 37.49 W, respectively. The experimentally calculated efficiency (η) for 580 W DASC-MLI is 93.54%.

5.12 Conclusion

A new 17-level DASC-MLI using reduced number of active and passive components is proposed in this chapter. TSV of the proposed DASC-MLI is low, thus facilitating utilization of lower-rated semiconductor devices for higher power applications. The DASC-MLI possesses reverse current carrying capability and higher output voltage levels using only one DC voltage source. Output voltage levels, higher than 17-level can also be achieved using the extended structure of proposed DASC-MLI. The potentiality of proposed DASC-MLI is verified through a cost function. Capacitor voltages are inherently balanced utilizing a combination of switches and diodes, thus completely eliminating the necessity of any external balancing circuit or algorithm in DASC-MLI. The number of capacitors and switches required in DASC-MLI are lower than reported SC-MLIs and thus its cost is lesser than reported SC-MLIs. The performance of the proposed DASC-MLI has been validated through a 580 W experimental prototype in this chapter. In order to further reduce the PIV, a new self-voltage balanced 17-level reduced voltage switched-capacitor MLI (RVSC-MLI) is proposed in the next chapter.