Chapter 2

Harmonic Minimization in HC-MLI Using Modified Particle Swarm Optimization

2.1 Introduction

In this chapter, a modified particle swarm optimization (MPSO) for fast convergence and harmonic minimization in three-phase, 11-level hybrid cascaded multilevel inverter (HC-MLI) has been proposed [99]. Selective harmonic elimination pulse width modulation (SHE-PWM) technique implemented through MPSO has been used in the proposed work for synthesizing an 11-level output voltage using two DC sources, a pre-charged capacitor and twelve switches. The switching angles of the three-phase, 11-level HC-MLI has been computed for eliminating specified lower order odd harmonics such as 5^{th}, 7^{th}, 11^{th} and 13^{th} from the output voltage of the HC-MLI. In the proposed MPSO optimized HC-MLI, capacitor voltage balance is also ensured even at higher modulation indices by utilizing the redundant switching states available at different switching instances of the HC-MLI. The redundant switching states affects the charging and discharging sequences of the capacitors depending on the direction of the load current in the HC-MLI. Based on analytical studies, a constraint for capacitor voltage balancing has been derived. Subsequently, using this constraint in MPSO and applying a voltage averaging technique to three-phase, 11-level HC-MLI, capacitor voltage balancing has been ensured, even at higher modulation indices. The results obtained through MPSO are compared with the results obtained through genetic

algorithm (GA) and particle swarm optimization (PSO) in terms of convergence rate and harmonic content.

2.2 Hybrid Cascaded MLI

A three-phase, 11-level HC-MLI is shown in Fig. 2.1. In the Fig. 2.1; H_1, H_2 are primary and H_3 is the supplementary H-bridge cells. The H-bridges are connected in cascade and the output voltage waveform is the sum of the outputs of all the individual H-bridges. The DC voltage source V_{dc} is used in primary H-bridges (H_1 and H_2). The DC source used in the supplementary bridge (H_3) is a pre-charged capacitor, whose voltage (V_{CAP}) is kept at $V_{dc}/2$. The output voltages of H_1, H_2 and H_3 are denoted as V_1, V_2 and V_3 respectively.

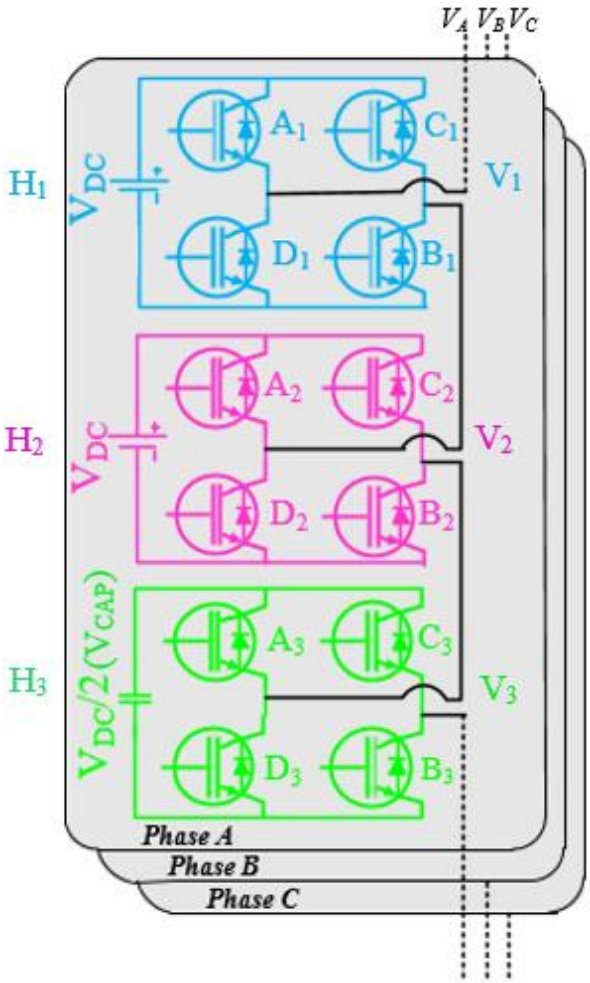


Fig. 2.1 Configuration of three-phase 11-level HC-MLI.

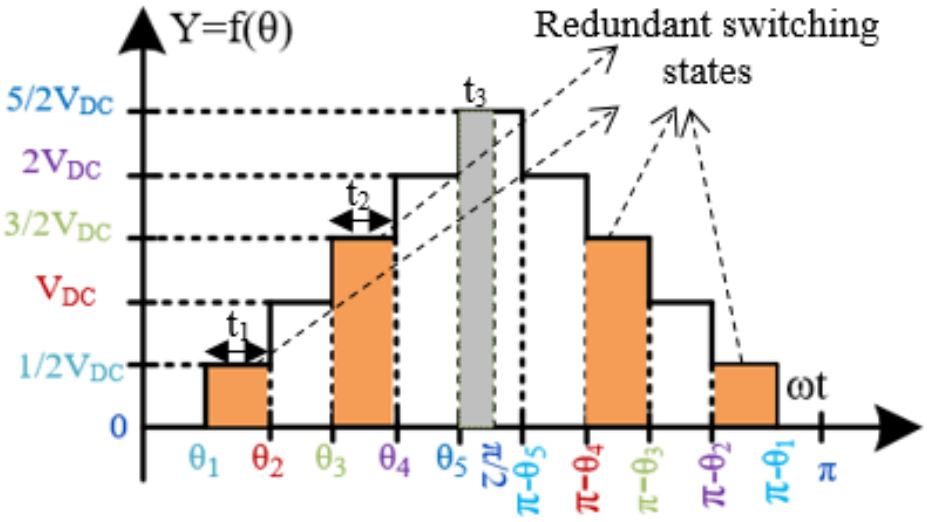


Fig. 2.2 Staircase waveform of 11-level HC-MLI.

Table 2.1
Switching States for Voltage Level Synthesis

Level	A_1	C_1	D_1	B_1	A_2	C_2	D_2	B_2	A_3	C_3	D_3	B_3	Output
	0	1	1	0	0	1	1	0	0	1	1	0	$-5V_{dc}$
	0	1	1	0	0	1	1	0	1	1	0	0	$-2V_{dc}$
	1	1	0	0	0	1	1	0	0	1	1	0	$-3V_{dc}/2$ (Redundancy1)
	0	1	1	0	1	1	0	0	0	1	1	0	$-3V_{dc}/2$ (Redundancy2)
	0	1	1	0	0	1	1	0	1	0	0	1	$-3V_{dc}/2$ (Redundancy3)
Negative	0	1	1	0	1	1	0	0	1	1	0	0	$-V_{dc}$ (Redundancy1)
	1	1	0	0	0	1	1	0	1	1	0	0	$-V_{dc}$ (Redundancy2)
	1	1	0	0	1	1	0	0	0	1	1	0	$-V_{dc}/2$ (Redundancy1)
	0	1	1	0	1	1	0	0	1	0	0	1	$-V_{dc}/2$ (Redundancy2)
	1	1	0	0	0	1	1	0	1	0	0	1	$-V_{dc}/2$ (Redundancy3)
	1	1	0	0	1	1	0	0	1	1	0	0	0
Zero	1	0	0	1	0	1	1	0	1	1	0	0	0
	0	1	1	0	1	0	0	1	1	1	0	0	0
	1	1	0	0	1	1	0	0	1	0	0	1	$+V_{dc}/2$ (Redundancy1)
	1	0	0	1	1	1	0	0	0	1	1	0	$+V_{dc}/2$ (Redundancy2)
	1	1	0	0	1	0	0	1	0	1	1	0	$+V_{dc}/2$ (Redundancy3)
	1	0	0	1	1	1	0	0	1	1	0	0	$+V_{dc}$ (Redundancy1)
	1	1	0	0	1	0	0	1	1	1	0	0	$+V_{dc}$ (Redundancy2)
Positive	1	0	0	1	1	1	0	0	1	0	0	1	$+3V_{dc}/2$ (Redundancy1)
	1	1	0	0	1	0	0	1	1	0	0	1	$+3V_{dc}/2$ (Redundancy1)
	1	0	0	1	1	0	0	1	0	1	1	0	$+3V_{dc}/2$ (Redundancy1)
	1	0	0	1	1	0	0	1	0	1	1	0	$+5V_{dc}$
	1	0	0	1	1	0	0	1	1	1	0	1	$+2V_{dc}$

The generated output voltage V_0 of the 11-level HC-MLI is obtained using combinations of V_1, V_2 and V_3 as, $V_0 = V_1 \pm V_2 \pm V_3$. Utilizing the switches of H_1, H_2 and H_3 of Fig. 2.1 appropriately, V_0 can be made $+5V_{dc}/2$, $+2V_{dc}$, $+3V_{dc}/2$, $+V_{dc}$, $+V_{dc}/2$, 0, $-5V_{dc}/2$, $-2V_{dc}$, $-3V_{dc}/2$, $-V_{dc}$ and $-V_{dc}/2$. The output voltage V_0 and the redundant switching states of the staircase waveform is shown Fig. 2.2. The switching logic for the 11-level HC-MLI is given in Table 2.1.

2.3 Solution Using PSO

PSO algorithm is an evolutionary algorithm capable of solving difficult multidimensional and multi-objective optimization problems in various fields. In PSO, particles keep searching to find the optimum solution based on the best experience of the swarm (global best, or g_{best}) by using their past experiences (personal best, or p_{best}). The particles are randomly generated initially. Each particle i (i = 1 to swarm size) possesses a current position $x_i = [x_{i1}, x_{i2} \ldots l_{id}]$ and velocity $v_i = [v_{i1}, v_{i2} \ldots v_{id}]$, where, d is the dimension of search space. The velocity of the particle indicates the change in the position from one step to the next. Every particle in search space memorizes its *pbest*, which corresponds to the best fitness value in the searching places. Every particle tries to attain the *gbest* that is the whole best place searched by one member of the swarm. Exploration is the ability of a search algorithm to explore different region of the search space in order to locate a good optimum solution. Exploitation is the ability to concentrate around a suitable search space in order to get better solution. With their exploration and exploitation, the particle of the swarm fly through the space and have two essential capabilities: the memory of their own best *pbest* position and knowledge of the global or their neighborhood's *gbest.* The basic concept behind the PSO technique is to change the velocity of each particle towards its *pbest* and *gbest* positions at every time step.

Each particle tends to modify its current position and velocity. Let *x* and *v* denotes the co-ordinates (position) and fly speed (velocity) of a particle in a search space respectively [90]-[93]. The velocity and position of each particle can be calculated using the current velocity and the distance from $pbest_{id}$ and $gbest_{id}$ as

$$V_{id}^{k+1} = wV_{id}^{k+1} + c_1 r_1 \left(pbest_{id} - X_{id}^{k}\right) + c_2 r_2 \left(gbest_{id} - X_{id}^{k}\right) \quad (2.1)$$

$$x_{id}^{k+1} = x_{id}^{k} + v_{id}^{k+1} \quad (2.2)$$

where *k*: number of iterations; *d*: number of dimensions corresponds to number of members of each particle; v_{id}^{k+1}: velocity of member *d* of particle *i* at iteration *k*+1; v_{id}^{k}: velocity of member *d* of particle *i* at iteration *k*; x_{id}^{k+1}: position of member *d* of particle *i* at iteration *k*+1; x_{id}^{k}: position of member *d* of particle *i* at iteration *k*; c_1: constant weighing factor corresponding to *pbest*; c_2: constant weighing factor corresponding to *gbest*; r_1 and r_2: random number between 0 and 1. The constants c_1 and c_2 represents the learning co-efficient (cognitive and social) that tries to attract each particle toward its *pbest* and *gbest* position. The acceleration constants c_1 and c_2 are often set to 1.8 according to past experiences. The new velocity for every particle is based on the particle's previous velocity, location of the particle at which the best fitness has been achieved so far and the population's global location at which the best fitness achieved. PSO simple to implement and have few parameters to adjust and do not overlap or mutate.

2.3.1 Limitations of PSO

PSO locates nearly optimal solution with a fast convergence speed. However, the major limitation of PSO is that it fails to adjust its velocity step size for fine tuning in the search

space. This often leads to premature convergence. Moreover, increase in number of switching angles in PSO results in increase in complexity of the search space and ultimately it is trapped in the local optima of the search domain [90]-[94]. To take care of this problem, a local search technique, named as mesh adaptive direct search (MADS) is combined with PSO to accelerate the convergence to an adjacent local optimum and refine the local search of the algorithm to prevent it being stuck in the local optima [100]. The method thus evolved is named as modified PSO (MPSO). To increase the fitness value of particles, mutation in velocity is applied in MPSO. Mutation is also applied in MPSO on the velocities of those particles that are not able to find a better position in search space. Combining the advantages of MADS and mutation strategy in MPSO obtains time-optimal solutions.

2.4 Proposed Modified PSO

In the proposed MPSO, MADS is used for local refinement of particles because of its fast convergence towards local optima. MADS has two types of grids, known as mesh and frame. The mesh is the set of conventional grids and the frame consists of mesh points. MADS has two steps at each iteration; called the search step which is done around the mesh points and the poll step which is done when there is no more improvement found by the mesh points in the search step. MADS searches optimal solution by reducing the mesh size until a better solution is achieved. When the mesh size is reduced below the accepted value, MADS finds optimal solution and terminates the iteration process [100]. The proposed algorithm starts with initialization of random particles (switching angles). After evaluating fitness of each particle, personal best (*pbest*) and global best (*gbest*) positions are updated. In case of conventional PSO, the subsequent iteration starts and new particles are estimated according to their initial position, velocities, *pbest* and *gbest* positions. In contrast to this, in MPSO, the subsequent

iteration will not start till local refinement around the best particle is achieved. The best particles of the population are taken as starting search points in MADS. Finally, MPSO locates the local minimum around each initial point. The idea of using mutation in MPSO is that, if a particle cannot improve its fitness in search domain, its future velocity will not be affected by its previous velocity. So, if n^{th} particle fails to achieve a better fitness at the end of i^{th} iteration, its velocity components $V_{nd}(i)$ are mutated. In MPSO, mutation mechanism is achieved using differential evolution (DE)/current-to-best/1 mutation strategy [101]-[103]. The magnitude of mutation is determined by past velocity, *pbest* and *gbest*. The iteration of mutation process does not terminate till better fitness of particles are found.

2.4.1 Improvement in Weighting Factor

To control the search speed of the particle, proper tuning of weight factor (w) is necessary. The balance between exploitation and exploration is maintained by w. The direction of particle in which it was moving previously is also maintained by w. This operation is advantageous at the start of the search operation, where the particles are extensively dispersed. MPSO has drawback of increasing the convergence time when the particles oscillate near *gbest* position. So, a non-linear w is more useful than linearly decreasing w. A new exponential decaying weighting factor $(w_{\exp})$, which adapts the value of w with respect to distance of the ith particle from the *gbest* position. It decays to a low value, resulting in reducing convergence time with number of iterations. The modified weight factor is given as

$$w_{i,\exp}^{k} = \left(\left(\frac{x_{gb} - x_i^k}{v_{\text{orms}}} \right) - f_1 \right) \cdot \exp\left(\frac{k_{\max}}{f_2 + k_{\max}} \right) \tag{2.3}$$

where f_1 and f_2 are controlling factors taken as 0.2 and 5 respectively, $k_{\max}$ is number of iterations and v_{orms} is the rms value of output voltage whose value depend upon modulation indices of HC-MLI.

2.4.2 Improvements in Cognitive and Social Parameters

The cognitive c_1 and social c_2 parameters are modified in this proposed algorithm as

$$c_1 = \frac{c_2 \cdot v_{\text{orms}}}{\left| d_{\text{lbest}} - d_{\text{gbest}} \right| + 1} \tag{2.4}$$

$$c_2(k) = c_{2,\min} + \frac{k}{k_{\max}}(c_{2,\max} - c_{2,\min}) \tag{2.5}$$

where d_{lbest} and d_{gbest} are the local best and global best positions of the particle, v_{orms} is the rms output voltage of inverter, $c_{2,\max}$, and $c_{2,\min}$ are the maximum and minimum values of social parameter.

The values of $c_{2,\min}$ and $c_{2,\max}$ lie between 0.1 to 2 respectively. The cognitive parameter c_1 and social parameter c_2 are used to calculate velocity of each particle in MPSO algorithm. The cognitive parameter c_1 helps the particles to explore the search space, while the social parameter c_2 helps the particles to exploit the search space. The expression of c_1 has been proposed in this work which decreases linearly in each iteration. This helps the particles to escape any local minima. This adaptive nature of cognitive parameter ensures faster convergence of the algorithm towards the global best.

The modified velocity expression utilizing the modified weight factor and cognitive factor as follows

$$V_{id}^{k+1} = w_{i\exp}^{k} \cdot V_{id}^{k} + c_1 r_1 (x_{lb\_i} - x_{id}^{k}) + c_2 r_2 (x_{gb\_i} - x_{id}^{k}) \tag{2.6}$$

$$x_{id}^{k+1} = x_{id}^{k} + v_{id}^{k+1} \tag{2.7}$$

where k is the pointer of iterations, d is the position number of D-dimensions, V_{id}^{k+1} is the velocity particle of i at $(k+1)^{\text{th}}$ iteration, V_{id}^{k} is the velocity of particle i at k^{th} iteration, x_{id}^{k+1} is

the position of particle *i* at $(k+1)^{th}$ iteration, x_{id}^{k} is the position of particle *i* at k^{th} iteration, c_1 is the cognitive parameter corresponding to *pbest*, c_2 is the social factor corresponding to *gbest* and $r_1, r_2 \in R(0,1)$.

2.4.3 Mutation in Velocity Using DE/best/1 Mutation Strategy

The list of procedures for mutation in velocity are as follows:

Step1: Initialization

Generate V_P, initial particle's velocity vectors and $vel_g = \{v_{1g}, v_{1g} \cdot v_{N_P,g}\}$, which denotes population of velocity vector. It consists of number of target velocity particles. Each particle in velocity vector, $v_{ig} = (v_{i,1,g}, v_{i,2,g} \cdots v_{i,\mathrm{D},g})$ is a *D*-dimensional vector. A mutant vector is generated using mutation operator for each target vector v_{ig} .

Step 2: Mutation in Velocity Vector

Two different particles (v_{r1}, v_{r2}) are chosen from population. The best velocity vector is obtained by sorting the generated population vector according to their fitness value. The mutant vector is generated as follows

$$vel_{i,g}(mut) = v_{pbest,g} + f \cdot (v_{r1,g} - v_{r2,g}) \tag{2.8}$$

where $v_{pbest,g}$ best velocity particle in the population and *f* is the DE scaling factor lies between 0 to 1.

2.4.4 Velocity Limits

The velocity operator updates the position of the particle which depends on the distance from the *gbest* to *lbest* position. If the distance between *gbest* and *lbest* is less, the velocity changes

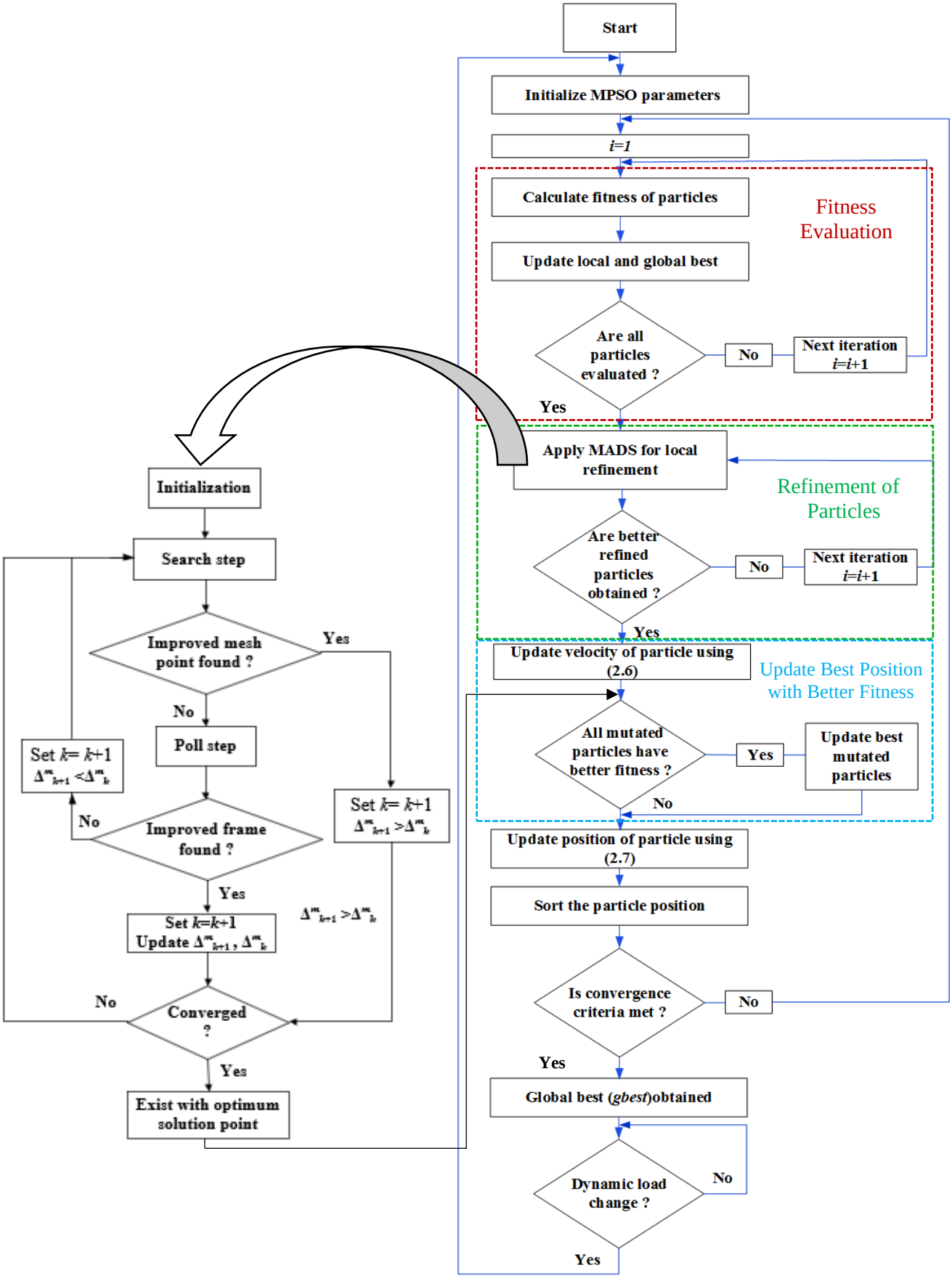


Fig. 2.3 Flow chart of MPSO.

is small, and if they are large, the corresponding velocity is large. This creates interruption in algorithm for detecting the global position. The solution to this problem is to limit the velocity up to certain maximum value, such that $\left[-\Delta v_{\max}, \Delta v_{\max}\right]$. In case of violation of these limits, the closest point to the boundary is selected. The flowchart of the complete algorithm is shown in Fig. 2.3.

The algorithm for solving the harmonics optimization problem is as follows:

Step 1: Generate initial population with randomly generated particles.

Step 2: Evaluate fitness values of all particle in the population and discard the particles those have same fitness value.

Step 3: If the fitness is better than the best fitness value, i.e., *lbest*, set current value as the new *lbest*. The particle with the best fitness value among all the particles is chosen as the *gbest*.

Step 4: Apply MADS for local refinement of particles.

Step 5: Adjust particle position and velocity.

Step 6: The global maximum value changes during dynamic loading conditions. In such a case, the particles are reinitialized to search the new global maximum again.

Step 7: Go to step 2, until the termination condition is met.

2.5 SHE-PWM Applied to MPSO Optimized HC-MLI

The mathematical representation of proper fitness function *f* is defined as

$$f = \min\left\{\left(100\frac{V_1^* - V_1}{V_1^*}\right)^4 + \sum_{s=4}^{S}\frac{1}{h_s}\left(50\frac{V_{h_s}}{V_1}\right)^2\right\} \tag{2.9}$$

subjected to

$$0 \le \theta_1 \le \theta_2 \le \theta_3 \cdots \theta_n < \frac{\pi}{2} \tag{2.10}$$

where V_1^* is the desired fundamental component and h_s is the order of s^{th} harmonic e.g., h_2 =5, h_3 = 7, h_4=11 and h_5=13. The weighting factors specify the reduction of lower harmonics. The fitness function signifies THD minimization. The population size and number of iterations are taken as 100 and 300 respectively. The iteration is started with the initialization of particles (switching angles) and then the fitness value of each particle is evaluated. In MPSO, local refinement of particles is achieved using MADS and particles with more precise value are taken. Mutation is applied to the velocity of particles to obtain better fitness value. The above process is repeated for different modulation indices until last iteration is achieved. Fig. 2.4 shows the optimal switching angles versus modulation index (m_a) for MPSO optimized HC-MLI to eliminate lower order harmonics using SHE-PWM. It can be noticed that switching angles decrease by increasing the modulation indices. Fig. 2.5 shows the content of lower order harmonics (5^{th}, 7^{th}, 11^{th} and 13^{th}) versus modulation indices using the proposed MPSO algorithm. It clearly shows that the lower-order harmonics have decreased significantly.

To verify the effectiveness of the proposed algorithm, cumulative distribution function (CDF) is determined for the proposed MPSO and compared with PSO and GA at different fitness function values as shown in Fig. 2.6 [104], [105]. The results obtained establishes the superiority of MPSO in terms of convergence rate as compared to PSO and GA. Table 2.2 gives the comparison of convergence rate and fitness values of different algorithms. It can be noticed that the convergence rate and fitness value of MPSO is better than GA and PSO.

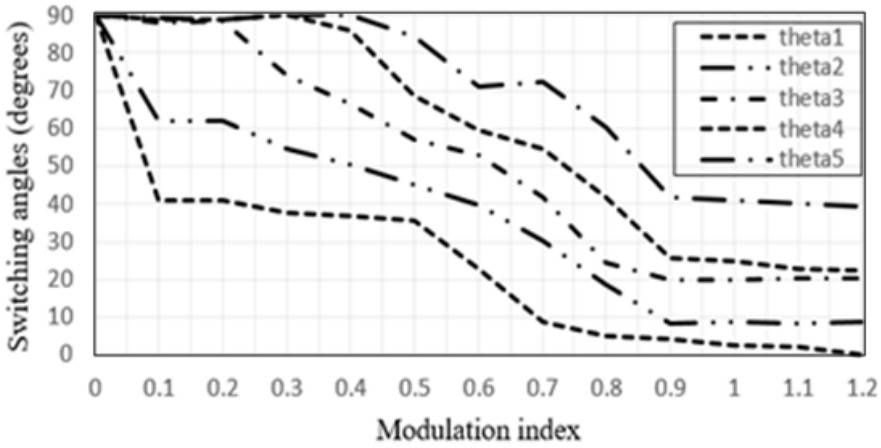


Fig. 2.4 Switching angles for different modulation indices.

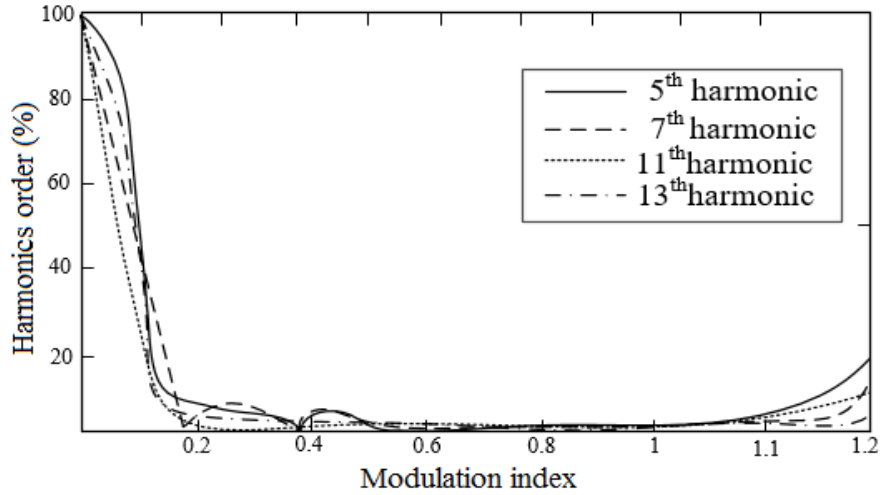


Fig. 2.5 The 5^{th},7^{th},11^{th} and 13^{th} harmonics versus modulation indices.

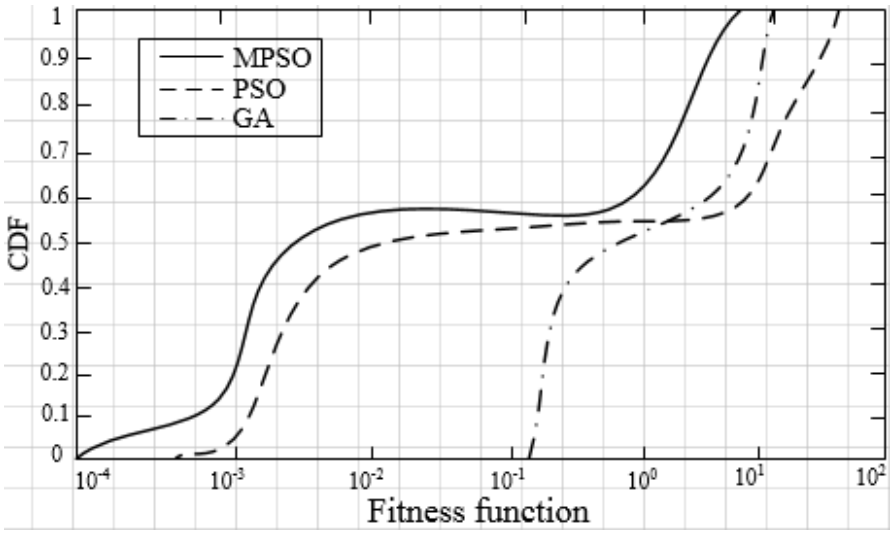


Fig. 2.6 Comparison of convergence rate between GA, PSO and MPSO.

Table 2.2
Constraints of MPSO, PSO and GA
Population size =100 and No. of Iteration=300

Parameters	MPSO	PSO	GA
Fitness value	$6.05X10^{-13}$	$1.15X10^{-03}$	0.4670
Convergence rate towards global minima	very high	high	low

Table 2.3
%THD Comparison for Different Algorithms

Modulation index	%THD (MPSO)	%THD (PSO)	%THD (GA)
0.5	8.41	10.27	13.87
0.6	7.53	9.21	12.35
0.7	7.69	9.73	12.86
0.8	5.23	7.42	11.32
0.9	4.17	6.05	10.85
1	5.03	7.09	9.87
1.1	5.64	7.71	8.05
1.2	6.21	8.03	9.31

%THD at different modulation indices are calculated for MPSO, PSO, and GA as given in Table 2.3. The result shows that for MPSO, the %THD is less as compared to GA and PSO.

2.6 Capacitor Voltage Balancing in HC-MLI Through MPSO

For proper operation of 11-level HC-MLI, the capacitor voltage has to be balanced over the entire cycle. The essential condition for capacitor voltage balance is to ensure that the net charge stored in the capacitor during the entire cycle must be greater than zero. If the net charge stored in the capacitor during the entire cycle is less than zero, the capacitor voltage falls, which leads to depletion of subsequent voltage levels [32], [33]. An optimal control strategy ensures that the net charge stored in the entire cycle should be greater than zero to

keep the average capacitor voltage constant. Different redundant switching states of the three-phase, 11-level HC-MLI are used for capacitor voltage balancing, depending on the direction of load current and sensed capacitor voltage. This is done as per the time interval of the staircase waveform and the available redundancies for that level. For obtaining the required voltage level, the capacitor voltage is used either in addition or in opposition with dc voltage sources. In one cycle, the net amount of stored charge is given as

$$Q_{stored} = Q_{charging} - Q_{discharging} \tag{2.11}$$

Applying fundamental switching to the 11-level HC-MLI and assuming the power factor angle to be Φ, load current is

$$I_{load} = I \sin(\theta - \Phi) \tag{2.12}$$

Capacitor charge balance condition for the MPSO optimized 11 HC-MLI is contented for a quarter cycle as

$$Q_{stored} = \pm \int_{\theta 1}^{\theta 2} I \sin(\theta - \Phi)\, d\theta \pm \int_{\theta 3}^{\theta 4} I \sin(\theta - \Phi)\, d\theta - \int_{\theta 5}^{\pi/2} I \sin(\theta - \Phi)\, d\theta \geq 0 \tag{2.13}$$

The ± sign in the period θ_1 to θ_2 and θ_3 to θ_4 indicates that there are both charging and discharging conditions.

2.6.1 Capacitor Voltage Balancing Conditions

The charging and discharging patterns of capacitor voltage are repeated in every quarter cycle. The first quarter cycle is divided into six intervals as shown in Fig. 2.2. Conditional switching states for capacitor voltage is given in Table 2.4. The voltage level of the capacitor

is investigated in each of the six intervals. The six intervals in one quarter cycle are as follows:

Interval 1: 0 to θ_1

No charging or discharging occurs in this interval.

Interval 2: θ_1 to θ_2

The capacitor charges or discharges in this interval. Fig. 2.7(a) and (b) shows charging interval for positive and negative load currents (I_{load}). Similarly, Fig. 2.7(c) and (d) shows discharging interval for positive and negative load currents. Considering charging interval for positive load current, the switches A_1, C_1 (of H_1), switches A_2, B_2 (of H_2) and switches C_3, D_3 (of H_3) are operated. The capacitor voltage is given by

$$V_c = (2V_{dc} - \frac{V_{dc}}{2} e^{-\frac{t_1}{\tau}}) \tag{2.14}$$

where $\tau = RC$ is the time constant. The capacitor voltage increment in this interval is given as

$$\Delta V_{C1} = \frac{V_{dc}}{2}(1 - e^{-\frac{t_1}{\tau}}) \tag{2.15}$$

Expanding the exponential term of (2.15) and considering that the capacitor used in H_3 is a large capacitor, the changes in the capacitor voltage is given as

$$\Delta V_{C1} = \frac{V_{dc}}{2} \cdot \frac{t_1}{\tau} \tag{2.16}$$

Substituting $t_1 = \frac{\theta_2 - \theta_1}{\omega}$ in (2.16)

$$\Delta V_{C1} = \frac{V_{dc}}{2} \cdot \frac{\theta_2 - \theta_1}{\omega\tau} \tag{2.17}$$

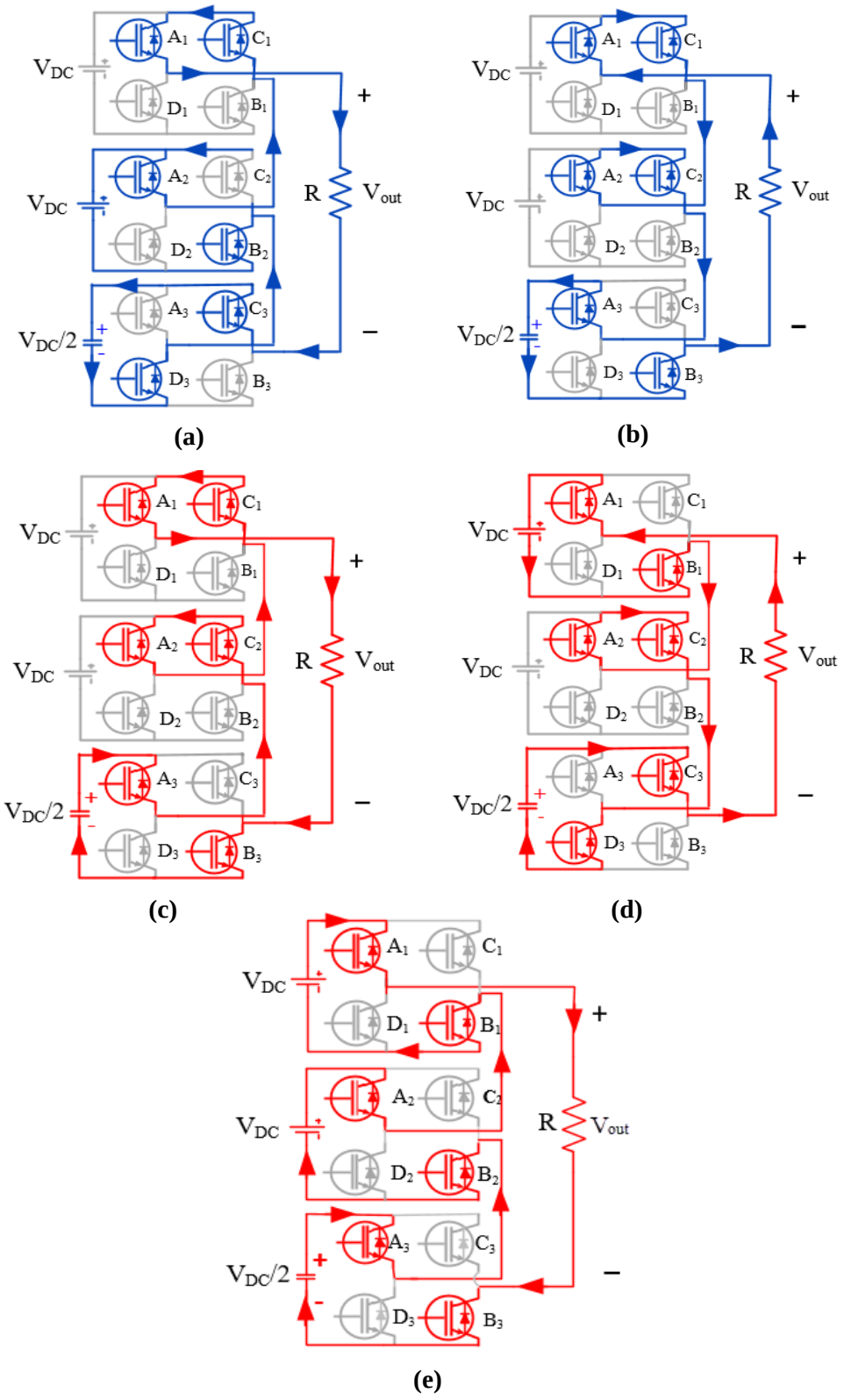


Fig. 2.7 Capacitor voltage balancing conditions.
Charging interval I_{load}>0. (b) Charging interval I_{load}<0. (c) Discharging interval I_{load}>0. (d) Discharging interval I_{load}<0. (e) Discharging interval (t_3) of peak voltage.

Table 2.4
Conditional Switching States for Capacitor Voltage Balance

Angles	Level	$V_{cap} > V_{dc}$		$V_{cap} < V_{dc}$	
		$I_{load}>0$	$I_{load}<0$	$I_{load}>0$	$I_{load}<0$
$0 \le \theta < \theta_1$	0	-	-	-	-
$\theta_1 \le \theta < \theta_2$	$V_{dc}/2$	Redundancy 1	Redundancy 2/3	Redundancy 2/3	Redundancy 1
$\theta_2 \le \theta < \theta_3$	V_{dc}	Redundancy 1/2	Redundancy 1/2	Redundancy 1/2	Redundancy 1/2
$\theta_3 \le \theta < \theta_4$	$3V_{dc}/2$	Redundancy 1/2	Redundancy 3	Redundancy 3	Redundancy 1/2
$\theta_4 \le \theta < \theta_5$	$2V_{dc}/2$	-	-	-	-
$\theta_5 \le \theta < 90$	$5V_{dc}/2$	-	-	-	-
$90 \le \theta < 180 - \theta_5$	$5V_{dc}/2$	-	-	-	-
$180 - \theta_5 \le 180 - \theta_4$	$2V_{dc}/2$	-	-	-	-
$180 - \theta_4 \le 180 - \theta_3$	$3V_{dc}/2$	Redundancy 1/2	Redundancy 3	Redundancy 3	Redundancy 1/2
$180 - \theta_3 \le 180 - \theta_2$	$V_{dc}/2$	Redundancy 1/2	Redundancy 1/2	Redundancy 1/2	Redundancy 1/2
$180 - \theta_2 \le 180 - \theta_1$	$V_{dc}/2$	Redundancy 1	Redundancy 2/3	Redundancy 2/3	Redundancy 1
$180 - \theta_1 \le 180$	0	-	-	-	-

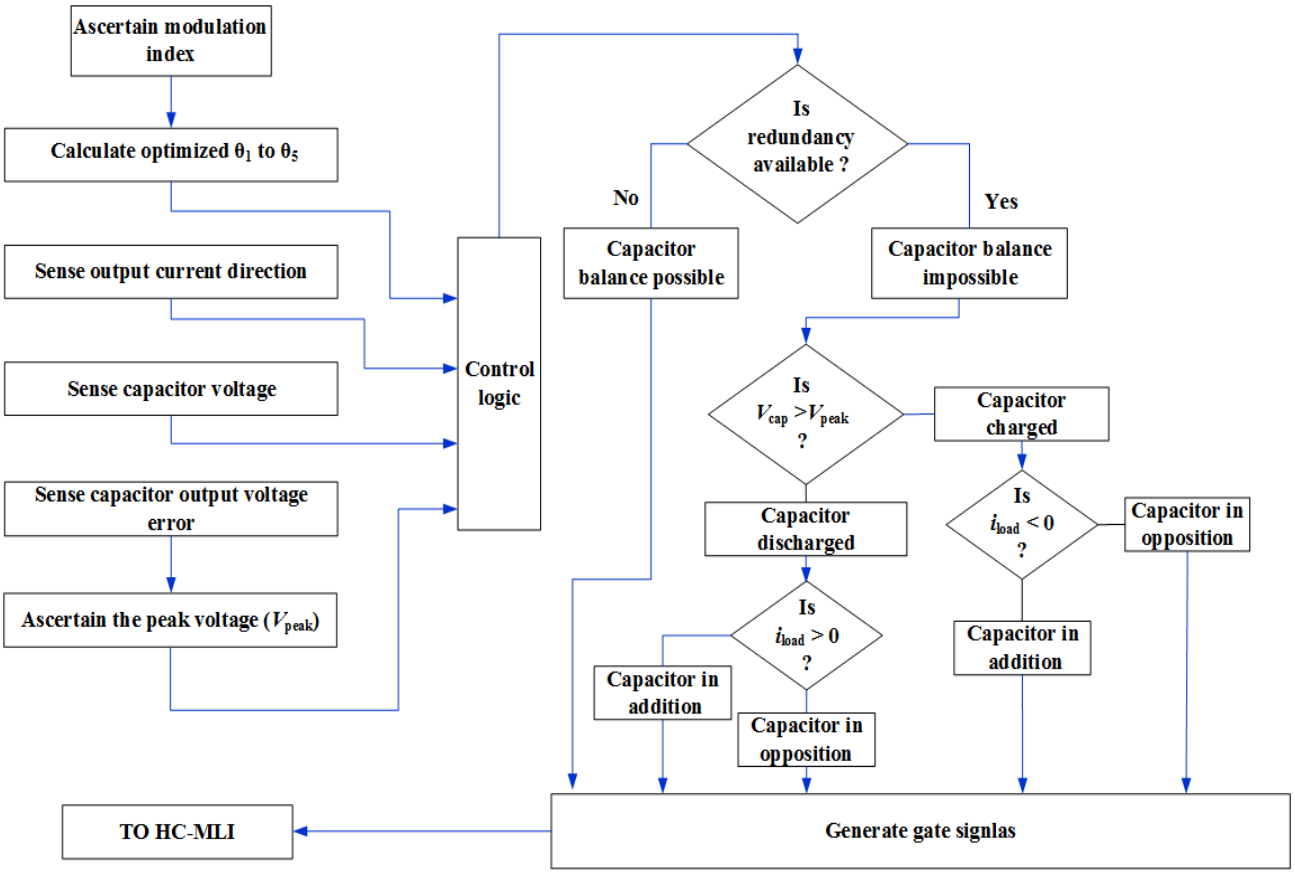


Fig. 2.8 Flow chart of control algorithm.

Interval 3: θ_2 to θ_3

No charging or discharging occurs in this interval.

Interval 4: θ_3 to θ_4

The capacitor charges or discharges in this interval. The changes in the capacitor voltage in this interval is given as

$$\Delta V_{C2} = \frac{V_{dc}}{2} \cdot \frac{t_2}{\tau} \tag{2.18}$$

Substituting $t_2 = \frac{\theta_4 - \theta_3}{\omega}$ in (2.18),

$$\Delta V_{C2} = \frac{V_{dc}}{2} \cdot \frac{\theta_4 - \theta_3}{w\tau} \tag{2.19}$$

Interval 5: θ_4 to θ_5

No charging or discharging occurs in this interval.

Interval 6: θ_5 to $\frac{\pi}{2}$

The capacitor must be discharged by the load current in this interval. Fig. 2.7(e) shows the discharging interval of the capacitor. The switches A_1, B_1 (of H_1), switches A_2, B_2 (of H_2) and switches A_3, B_3 (of H_3) are operated for discharging interval. The capacitor voltage increment in this interval is given as

$$\Delta V_{c3} = -(\frac{5V_{dc}}{2} + \Delta V_{C1} + \Delta V_{C2})(1 - e^{-\frac{t_3}{\tau}}) \tag{2.20}$$

Since the capacitor used in the third H-bridge cell is a large capacitor, using (2.17) and (2.19) in (2.20), the following is obtained

$$\Delta V_{C3} = -5\frac{V_{dc}}{2} \cdot (1 - e^{-\frac{t_3}{\tau}}) \simeq -5\frac{V_{dc}}{2} \cdot \frac{t_3}{\tau} \tag{2.21}$$

Substituting $t_3 = \dfrac{\frac{\pi}{2} - \theta_5}{\omega}$ in (2.21),

$$\Delta V_{C3} = -5\frac{V_{dc}}{2} \cdot \frac{\frac{\pi}{2} - \theta_5}{\omega\tau} \tag{2.22}$$

The capacitor voltage increment during the charging intervals should be more than the voltage decrement during the discharging interval to ensure capacitor voltage balancing. During the interval θ_1 to θ_2, the capacitor charges or discharges. It is assumed that the output voltage is constant in this interval. The capacitor current in this interval is given as

$$I_{C1} = \frac{V_{dc}}{2R} \tag{2.23}$$

where R is output resistance. Increment in the capacitor charge in this interval can be expressed as

$$\Delta Q_1 = \frac{V_{dc}}{2R} \cdot \frac{\theta_2 - \theta_1}{\omega} \tag{2.24}$$

During the interval θ_3 to θ_4, the capacitor charges or discharges. It is assumed that the output voltage is constant in this interval. The capacitor current in this interval given as

$$I_{C2} = \frac{V_{dc}}{2R} \tag{2.25}$$

Changes in the capacitor charge in this interval (θ_3 to θ_4) is given as

$$\Delta Q_2 = \frac{V_{dc}}{2R} \cdot \frac{\theta_4 - \theta_3}{\omega} \tag{2.26}$$

During the interval θ_5 to $\frac{\pi}{2}$, the capacitor discharges. The capacitor current is opposite to the load current in this interval and is given as

$$I_{C3} = -\frac{5V_{dc}}{2R} \tag{2.27}$$

Changes in the capacitor charge in this interval is given as

$$\Delta Q_3 = -\frac{5V_{dc}}{2R} \cdot \frac{\frac{\pi}{2} - \theta_5}{\omega} \tag{2.28}$$

The capacitor voltage can be balanced if the net charge stored in quarter cycle of operation is greater than zero. In other words, the balancing of capacitor voltage is possible if

$$\Delta Q_1 + \Delta Q_2 + \Delta Q_3 > 0 \tag{2.29}$$

Using (2.24), (2.26) and (2.28) in (2.29),

$$\frac{V_{dc}}{2R} \cdot \frac{\theta_2 - \theta_1}{\omega} + \frac{V_{dc}}{2R} \cdot \frac{\theta_4 - \theta_3}{\omega} - \frac{5V_{dc}}{2R} \cdot \frac{\frac{\pi}{2} - \theta_5}{\omega} > 0 \tag{2.30}$$

(2.30) can be simplified as

$$\theta_2 + \theta_4 + 5\theta_5 - (\theta_1 + \theta_3) > \frac{5\pi}{2} \tag{2.31}$$

For capacitor voltage balancing, (2.31) is to be satisfied. The modulation indices are obtained by using the constraint presented in (2.31) to ensure capacitor voltage balancing. Using the redundancies of 11-level HC-MLI, the conditional switching states for capacitor voltage balancing is given in Table 2.4. If $V_{CAP} < V_{dc}/2$, the capacitor has to be charged and if $V_{CAP} > V_{dc}/2$, the capacitor has to be discharged depending on the available redundancies. As the steady state error in the capacitor voltage decreases in subsequent voltage levels, capacitor voltage averaging technique is used to reduce the steady state error by charging the capacitor to a value slightly higher than $V_{dc}/2$ during allowable periods. The average DC voltage of the capacitor is compared with the reference voltage value ($V_{dc}/2$) and then the optimum gate signals for the proposed three-phase HC-MLI are generated. The flow chart of the control algorithm for capacitor voltage balance is shown in Fig. 2.8.

2.6.2 Capacitor Voltage Balancing at Higher Modulation Indices

The capacitor charge is unable to balance at higher modulation indices ($m_a > 0.9$) because of long discharging periods at voltage peaks. At a higher modulation index, discharging period is more than the charging period for which net charge accumulation in capacitor is less than zero [32]. To balance charge at higher modulation indices, third harmonic voltage is injected into the output voltage of HC-MLI through a square wave having frequency three times the fundamental frequency with magnitude $V_{dc}/2$ as shown in Fig. 2.9. Fig. 2.9(a) shows original 11-level voltage waveform. Fig. 2.9(b) shows injected third harmonic voltage and Fig. 2.9(c) shows final output voltage waveform. The Fourier series expression of the injected third harmonic voltage can be written as:

$$V_{(\omega t)} = \sum_{1,3,5..n}^{\infty} \frac{2V_{dc}}{n\pi} \cos n\theta_3 \cdot \sin 3n\omega t \qquad (2.32)$$

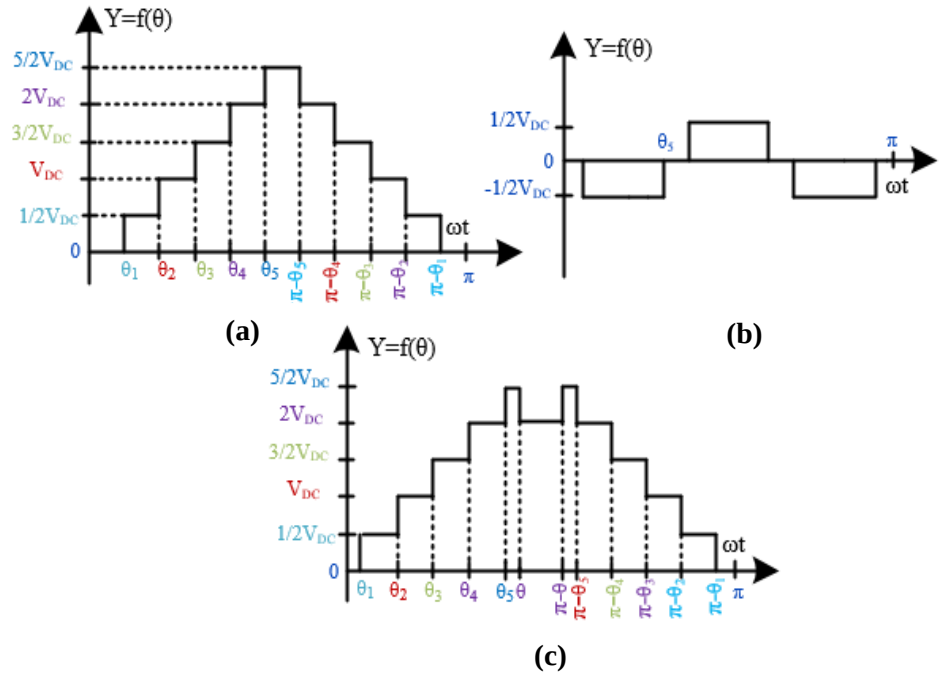


Fig. 2.9 Capacitor voltage balancing at higher modulation index for 11-level HC-MLI. (a) Original 11-level waveform. (b) Injected 3rd harmonic voltage. (c) Final voltage waveform.

The triplen-harmonic voltages will automatically cancel in the line-line voltages of three-phase systems, and will not change the fundamental frequency contents. The only effect is to change the charging period and discharging period. The condition of capacitor voltage balancing for the elven level HC-MLI in a quarter cycle operation at higher modulation index is given as:

$$Q_{stored} = \pm \int_{\theta_1}^{\theta_2} I \sin(\theta - \Phi)\ d\theta\ \pm \int_{\theta_3}^{\theta_4} I \sin(\theta - \Phi)\ d\theta\ - \int_{\theta_5}^{\theta} I \sin(\theta - \Phi)\ d\theta - \int_{\pi-\theta}^{\pi-\theta_5} I \sin(\theta - \Phi)\ d\theta \geq 0 \tag{2.33}$$

2.7 Closed-loop control of HC-MLI Using Proposed Algorithm

In the closed-loop operation of the HC-MLI, the controller generates optimized gate signals in such a way that the AC bus voltage (V_{AC}) is regulated to the reference value V_{AC}^{*}. The analog to digital converter (ADC) of DSP converts the analog signals (V_{CAP}, V_{AC}, V_{DC}) and

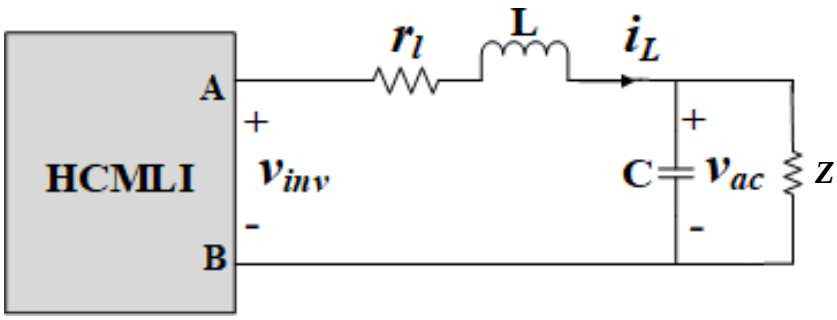


Fig. 2.10 Equivalent circuit of HC-MLI feeding an AC load (r_l: DC series resistance of the inductor L, R: impedance of load).

i_{AC}) into digital domain by sensing the feedback signals of HC-MLI. These feedback signals along with the reference signals and DC capacitor voltage are given as inputs to the controller blocks. The controller has two different control loops for controlling the capacitor voltage (V_{CAP}) and output voltage (V_{AC}). The AC output controller is designed using synchronous

reference control (SRF) method [106]-[108]. The outer voltage loop generates reference current I_L^* for the inner current loop and the inner current loop generates the gate signals.

2.7.1 Voltage Controller

The equivalent circuit of HC-MLI feeding a resistive load is shown in Fig. 2.10. The three-phase HC-MLI can be represented as

$$\frac{di_x}{dt} = -\frac{r_x}{L} + \frac{1}{L}(\mathrm{V}_{inv} - V_{ox}); x = a, b, c \tag{2.34}$$

$$\frac{dV_{ox}}{dt} = \frac{1}{C} i_{lx} - \frac{V_{ox}}{Z.C}; x = a,\ b,\ c \tag{2.35}$$

The variables *a*, *b*, *c* in three-phase stationary coordinates are transformed into rotating *d*-*q* coordinates as

$$\frac{d}{dt}\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} -\frac{r_l}{L} & \omega \\ -\omega & \frac{-r_l}{L} \end{bmatrix} \cdot \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \frac{1}{L} \cdot \begin{bmatrix} V_{invd} - V_d \\ V_{invq} - V_q \end{bmatrix} \tag{2.36}$$

$$\frac{d}{dt}\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} -\frac{1}{RC} & \omega \\ -\omega & -\frac{1}{ZC} \end{bmatrix} \cdot \begin{bmatrix} V_d \\ V_q \end{bmatrix} + \frac{1}{C} \cdot \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{2.37}$$

The output transfer functions of inner current control loop and outer voltage control loop are obtained by transforming (2.36) and (2.37) into *s* domain as

$$\begin{cases} \dfrac{I_d(S)}{U_{id}(S)} = \dfrac{I_q(S)}{U_{iq}(S)} = \dfrac{1}{sL + r_l} \\ \dfrac{V_d(S)}{U_{id}(S)} = \dfrac{V_q(S)}{U_{iq}(S)} = \dfrac{Z}{ZCS + 1} \end{cases} \tag{2.38}$$

$$\begin{cases} U_{id} = V_{invd} - V_d + \omega \cdot L \cdot I_q \\ U_{iq} = V_{invq} - V_q - \omega \cdot L \cdot I_d \\ U_{vd} = I_d + \omega \cdot C \cdot V_q \\ U_{vq} = I_q - \omega \cdot C \cdot V_d \end{cases} \tag{2.39}$$

The controller of converter adopts a double feedback loop control strategy including an outer voltage feedback loop and an inner current feedback loop. The schematic of complete DSP-based controller for HC-MLI is shown in Fig. 2.11(a). Fig. 2.11(b) and 2.11(c) show the schematics of the inner current controller and outer voltage controller of the proposed HC-MLI. The output of *d* and *q* axis voltage controller are u_{vd}^* and u_{vq}^*. From these reference signals, the inner control loop currents i_d^* and i_q^* are written as

$$\begin{cases} i_d^* = u_{vd}^* - \omega c v_q \\ i_q^* = u_{vq}^* + \omega c v_d \end{cases} \tag{2.40}$$

Similarly, the outputs of *d* and *q* axis voltage controllers are u_{iq}^* and u_{id}^*. respectively. From these signals, *d-q* components of modulating signals can be written as

$$\begin{cases} V_{mq} = \frac{1}{V_{dc}} . \left(u_{iq}^* + \omega L i_d + v_q \right) \\ V_{md} = \frac{1}{V_{dc}} . \left(u_{id}^* - \omega L i_q + v_d \right) \end{cases} \tag{2.41}$$

The AC voltage controller outputs are the modulation signals V_{md} and V_{mq} in *d-q* reference frame. The sinusoidal modulation signal, $V_{\mathrm{m}}(t)$ of the HC-MLI is obtained as

$$V_m(t) = m_a = V_{\mathrm{md}} \sin\theta + V_{\mathrm{mq}} \cos\theta \tag{2.42}$$

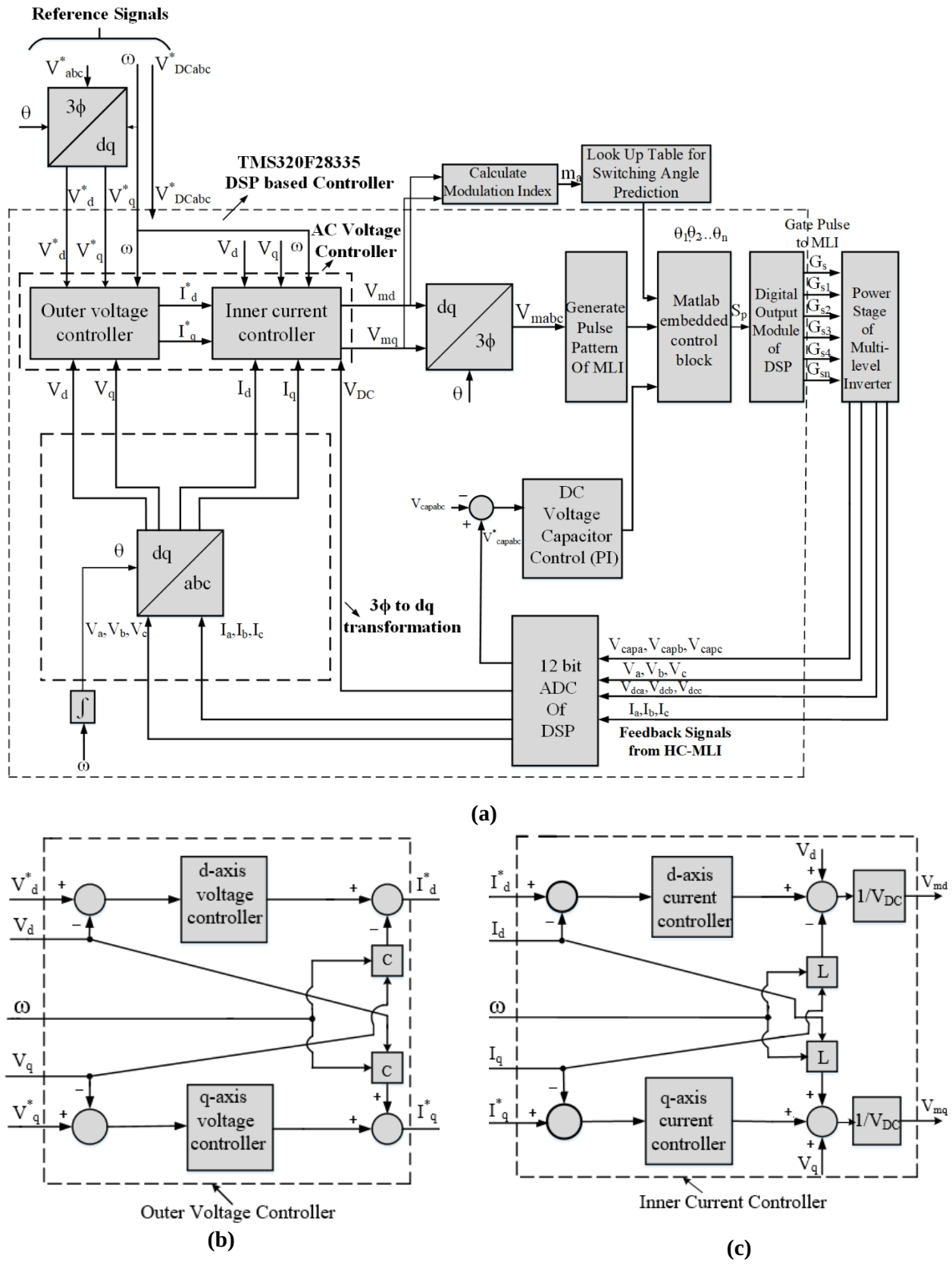


Fig. 2.11 Closed loop controller of HC-MLI.
(a) DSP based closed loop control of HC-MLI. (b) Schematic of inner current controller. (c) Schematic of DSP-based controller for HC-MLI.

An inner current loop control based on *d-q* synchronous reference frame is used to follow the accuracy of the desired reference current. The modulation index can be obtained from *d*-axis and *q*-axis voltages as

$$m_a = \frac{\sqrt{{v_{md}}^2 + {v_{mq}}^2}}{V_{DC}} \tag{2.43}$$

2.8 Capacitor Calculation

To calculate appropriate value of capacitance, the intermittent discharging period of the capacitor is considered. The capacitor has the intermittent discharging period in the interval θ_1 - θ_2; in the interval θ_3 - θ_4; in the interval θ_5 - $\pi/2$. The maximum discharging value Q_c is given as

$$Q_c = \frac{2}{\omega}\left[\int_{\theta_1}^{\theta_2} i_l d\theta + \int_{\theta_3}^{\theta_4} i_l d\theta + \int_{\theta_5}^{\pi/2} i_l d\theta\right] \tag{2.44}$$

For inductive load, load current (i_l) can be represented as

$$i_l = i_0 \sin(\omega t - \phi) \tag{2.45}$$

The maximum allowable voltage ripple across the capacitor is kV_{dc}, where *k* is the ripple factor. The optimal value of capacitance is given as

$$C_{Opt} \geq \frac{Q_c}{kV_{dc}} \tag{2.46}$$

Substituting (2.45) in (2.44) and using (2.46), the optimum capacitance for inductive loading condition can be obtained as

$$C_{Opt} = \frac{1}{k \times \omega \times |Z|} \cdot \left[\begin{array}{l} \sin\left(\frac{\theta_1 + \theta_2}{2} - \phi\right) \cdot \sin\left(\frac{\theta_2 - \theta_1}{2}\right) + \sin\left(\frac{\theta_3 + \theta_4}{2} - \phi\right) \cdot \sin\left(\frac{\theta_4 - \theta_3}{2}\right) \\ + \cos(\theta_5 - \phi) - \sin\phi \end{array}\right] \tag{2.47}$$

For 10% voltage ripple (k = 0.1), power factor $\cos\phi$ = 0.7 and load impedance Z = 17 Ω (R=12 Ω and L= 37 mH), the optimum capacitance value is calculated using (2.47) for different m_a are given in Table 2.5.

Table 2.5
Capacitance Values at Different m_a

m_a	Capacitance
0.6	234 µF
1	323 µF
1.1	351 µF

Table 2.6
Parameters Used for Simulation

Parameters	Attributes
Switching frequency	50 Hz
Output Filter Inductor	20 mH
Output Filter Capacitor	10 µF
Load (Resistive)	10 Ω
DC-link Capacitors	350 µF/200 V

2.9 Simulation Studies

A 1.5-kW three-phase, 11-level HC-MLI is simulated through MATLAB/Simulink using proposed MPSO optimization method. Table 2.6 lists the parameters used to verify the proposed work. The population size is taken as 100. The MPSO optimized switching angles θ_1 to θ_5 are calculated for different modulation indices and are shown in Fig. 2.4. The DC sources (V_{DC}) of two primary H-bridges and capacitor voltage (V_{CAP}) of supplementary H-bridge are taken as 60 V and 30 V. Device switching frequency is kept at 50 Hz. The SHE-PWM modulation technique using MPSO has been used for generating the optimal gate

control signals. The reference signal for the closed-loop control of the HC-MLI is taken as V_{AC}^{*} = 240 V (peak-peak) in the controller of HC-MLI as shown in Fig. 2.11. The value of capacitor voltage is controlled using proportional integral (PI) controller. The values of K_p and K_i obtained through MPSO algorithm are 0.14 and 4, respectively. The sensed capacitor voltages (V_{CAP}) of the respective three-phases phase *A*, phase *B* and phase *C* are fed back to the ADC of DSP through a signal conditioning circuit. The sensed average capacitor voltage is compared with the reference value and given to the embedded code logic block of MATLAB/Simulink. The direction of the load current is sensed using a current sensor for capacitor voltage balancing at available redundancies. During allowable periods, the capacitor is allowed to charge up to the maximum voltage decided by the PI controller as shown in Fig. 2.15. The steady state mean error is eliminated and the average capacitor voltage is maintained at 30 V.

2.9.1 Operation at m_a = 0.55

Based on Fig. 2.4, obtained switching angles are θ_1 = 32.14, θ_2 = 49.25, θ_3 = 61.15, θ_4 = 71 .45 and θ_5 = 84 .68. As shown in Fig. 2.12 the output voltages of the H_1, H_2 and H_3 are V_{a1}, V_{a2} and V_{a3} respectively. The total output voltage of the elven level HC-MLI is V_a, and the voltage of the capacitor is V_c. The output voltages of each H-bridge cell of 11-level HC-MLI are shown in Fig. 2.12. It can be observed that the average value of the capacitor is maintained at 30 V.

2.9.2 Operation at m_a = 1.2

For higher modulation index m_a=1.4, using on Fig. 2.4, switching angles are obatained as θ_1=5.21, θ_2=18.45, θ_3=30.05, θ_4= 41.67 and θ_5=65.47. With these set of switching angles, the constraint for the capacitor voltage balance as given in (2.31) is not satisfied. Therefore, the

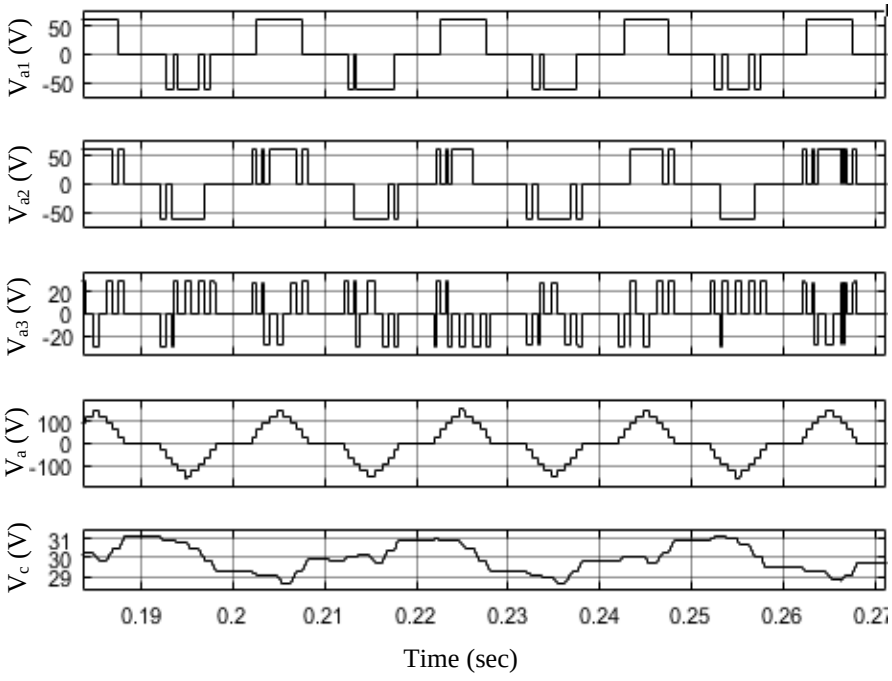


Fig. 2.12 Output voltages of each H-bridge cells with total output voltage at m_a =0.55.

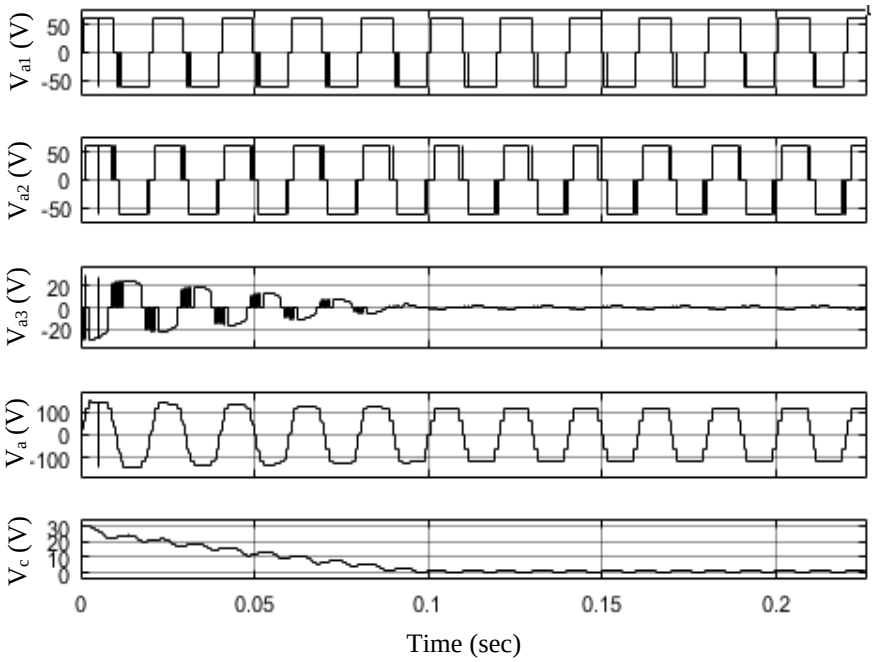


Fig. 2.13 Output voltages of each H-bridge cells with total output voltage at m_a =1.2 without capacitor voltage balance.

capacitor voltage will not remain at a constant level and will decrease continuously until it discharges completely as shown in Fig. 2.13. In such a situation, the third harmonic voltage

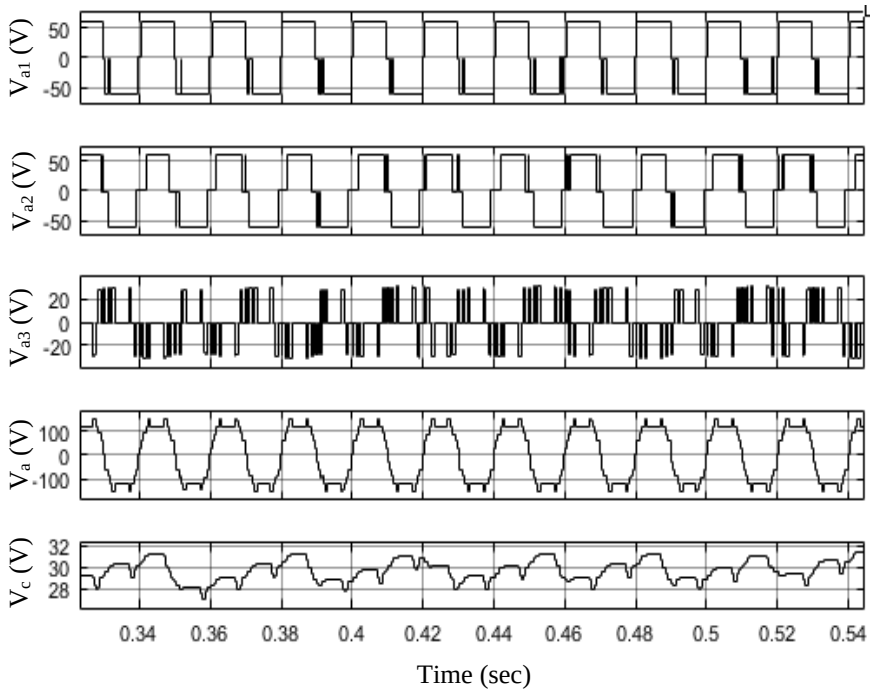
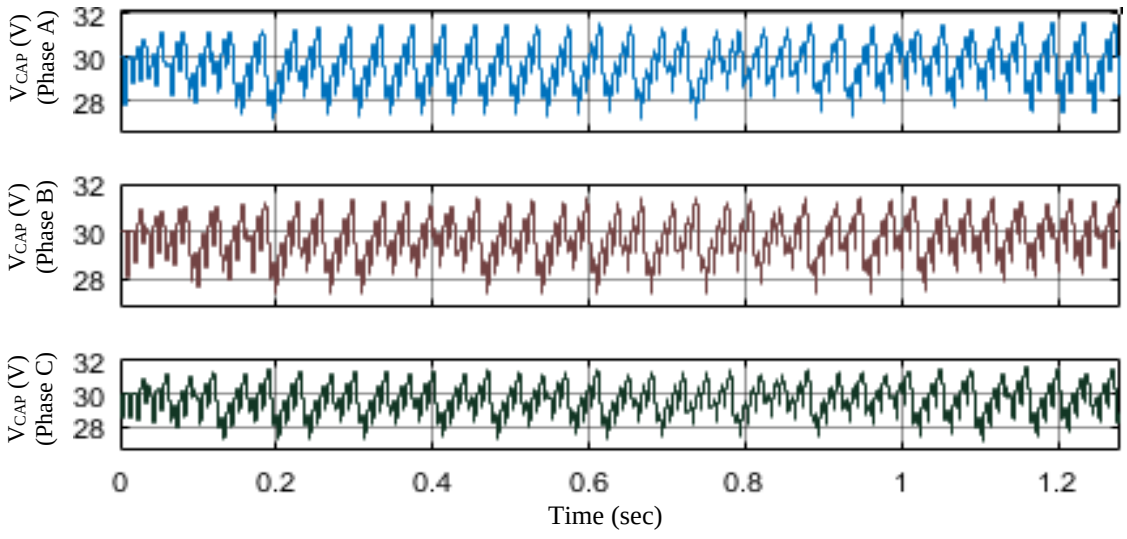
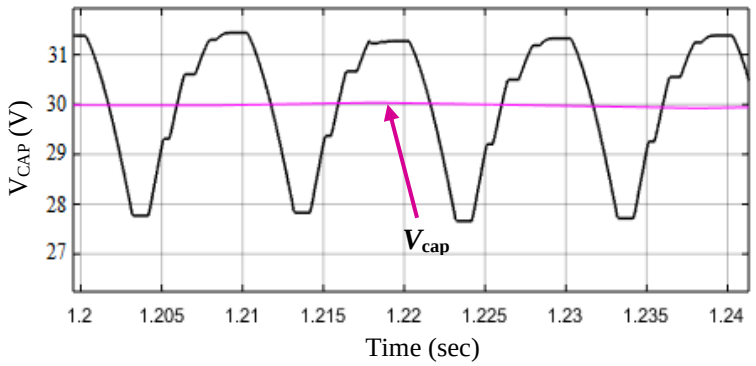


Fig. 2.14 Output voltages of each H-bridge cells with total output voltage at m_a =1.2 with capacitor voltage balance.

is injected to balance the capacitor voltage. The capacitor voltage balance at higher modulation index is shown in Fig. 2.14. The averge capacitor voltage is maintained constant at 30 V using capacitor voltage averaging technique. The simulated three-phase capacitor voltages are shown in Fig. 2.15(a) and average capacitor voltage is shown in Fig. 2.15(b).



(a)

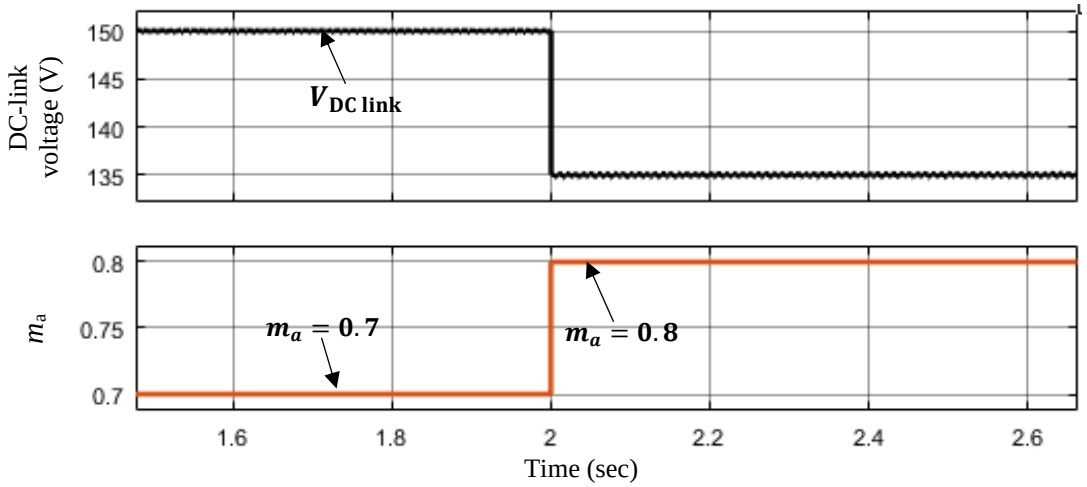


(b)

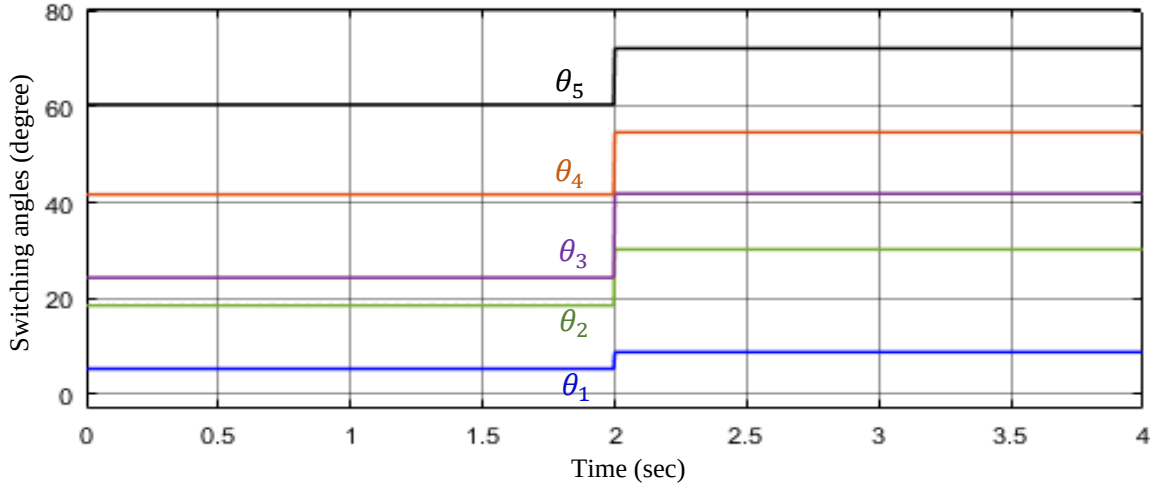
Fig. 2.15 Simulation results of three-phase capacitor voltages.
(a) Three-phase capacitor voltages with voltage averaging. (b) Capacitor voltage with voltage averaging (V_{CAP}).

2.9.3 Controller Performance During Change in DC-Link Voltage

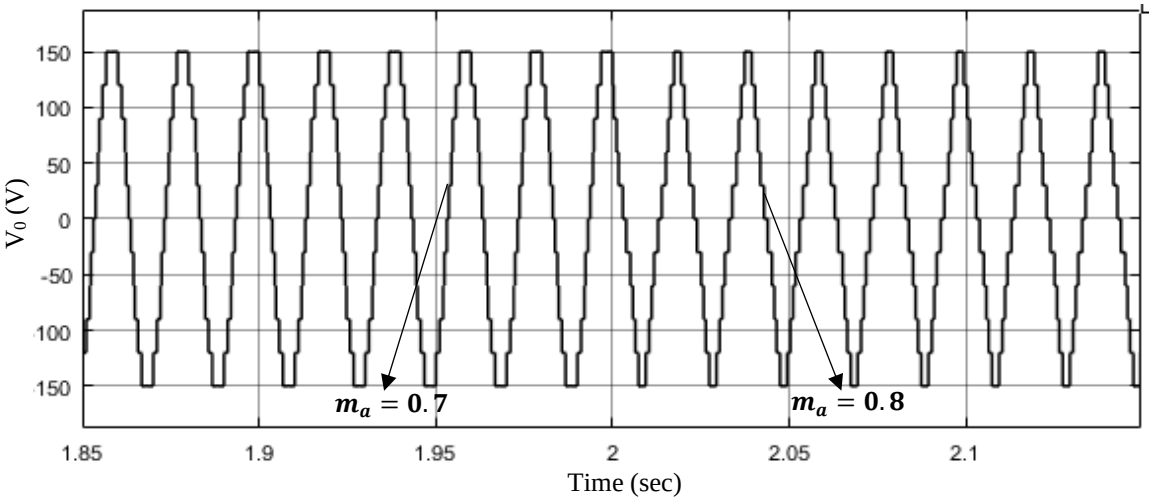
In closed loop control, the controller maintains the output voltage constant irrespective of the fluctuations in the DC-link voltage. During any fluctuations in the DC-link voltage, the modulation index (m_a) changes and the switching angle changes according to the corresponding modulation index. Please refer Fig. 2.11, where the AC voltage controller outputs are V_{md} and V_{mq} in *d-q* reference frame. The switching angles for different m_a values are stored in a look-up table. During fluctuations in DC-link voltage, m_a changes and the corresponding switching angles are obtained from the look-up table. Subsequently, the gate



(a)



(b)



(c)

Fig. 2.16 Simulation results of HC-MLI for change in DC-link voltage.
(a) Change in DC-link voltage due to change in m_a from 0.7 to 0.8. (b) Change in switching angles for change in m_a from 0.7 to 0.8. (c) Change in output voltage for change in m_a from 0.7 to 0.8.

control signals (S_1, S_2, S_3, ... S_n) are generated using the DSP which regulates the DC-link voltage. For verifying the control of DC-link voltage through simulation studies, a change in DC-link voltage from 150 V to 137 V is made. Consequently, the modulation index m_a changes from 0.7 to 0.8 to take care of the change in DC-link voltage as shown in Fig. 2.16(a). The change in corresponding switching angles due to change in m_a are shown in Fig. 2.16(b) and the generated output voltage is shown in Fig. 2.16(c).

2.9.4 Harmonic Analysis of Output Voltages at Different m_a

The output line voltage (V_{AB}) and its harmonic spectrum at m_a = 0.55 are shown in Figs. 2.17 and 18 respectively. Similarly, the output line voltage (V_{AB}) and its harmonic spectrum at m_a = 0.8 are shown in Figs. 2.19 and 2.20.

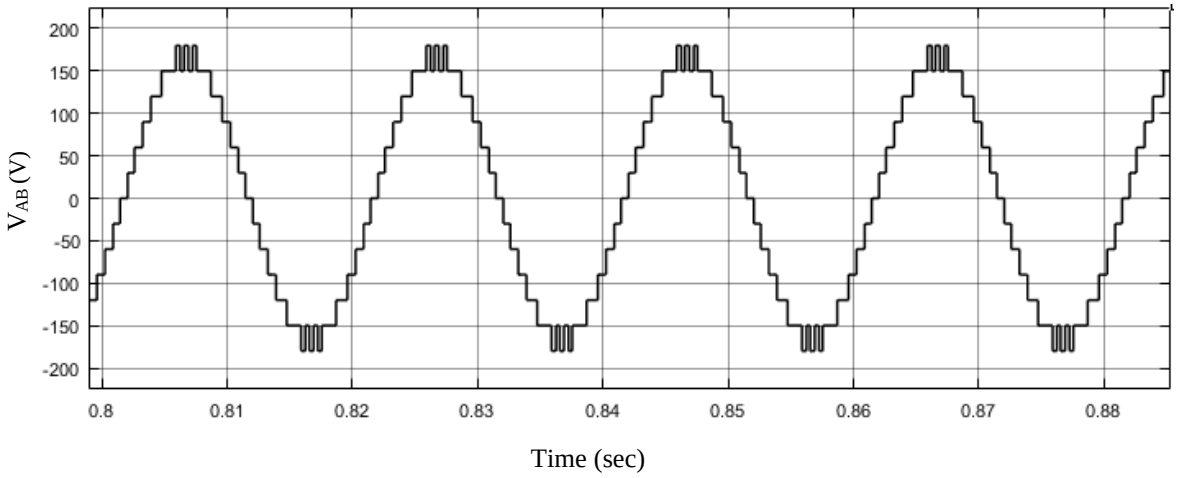


Fig. 2.17 Output voltage (V_{AB}) at m_a = 0.55.

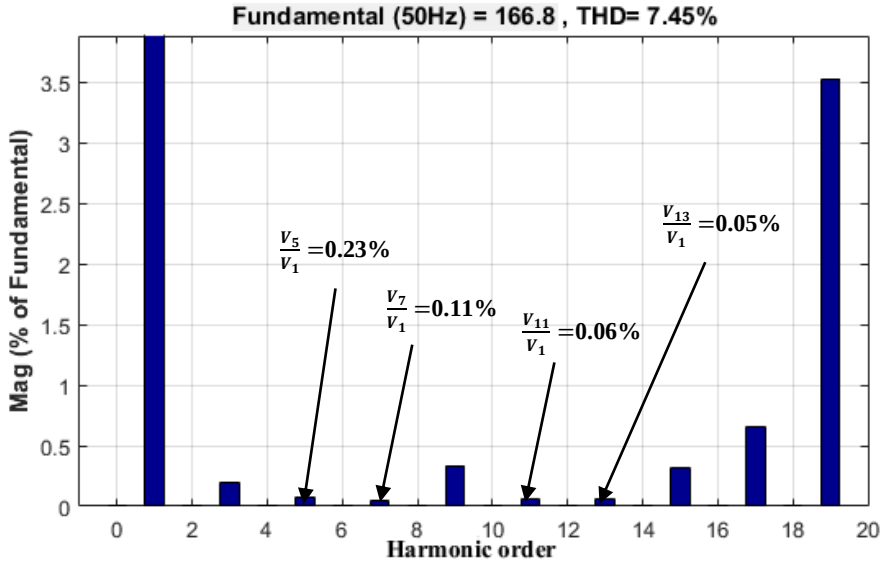


Fig. 2.18 Harmonic spectrum (V_{AB}) at m_a = 0.55.

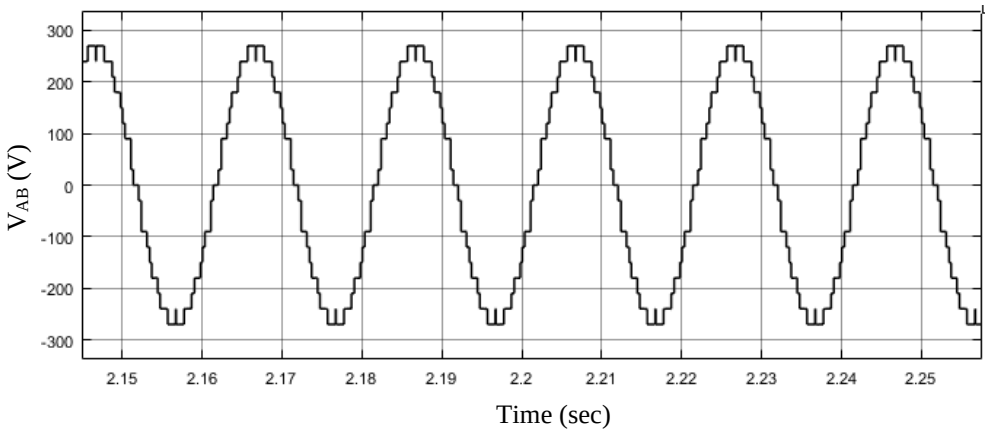


Fig. 2.19 Output voltage (V_{AB}) at $m_a = 0.8$.

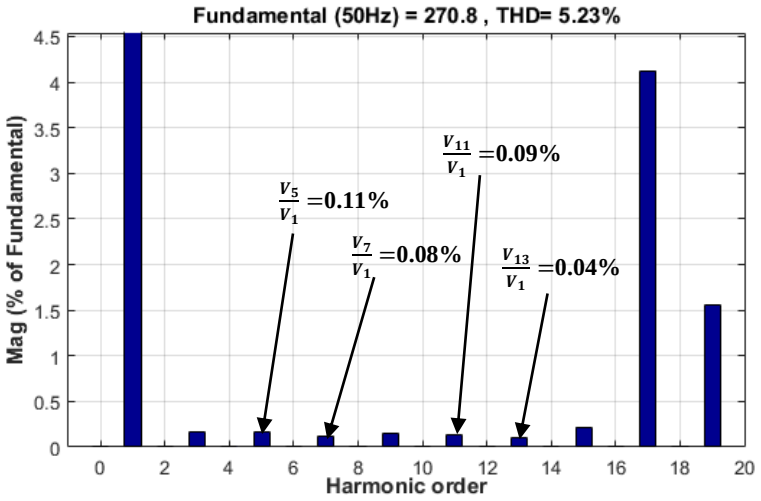


Fig. 2.20 Harmonic spectrum (V_{AB}) at $m_a = 0.8$.

2.9.5 Effects of Inductive Load on Capacitor Voltage Balancing at Higher Modulation Index

In (2.31), the load is assumed to be resistive. In HC-MLI, the maximum capacitor discharge occurs when the output voltage is at its maximum level. At this point, the current is also at its maximum level since the current is in phase with the voltage for resistive load. The capacitor discharges faster in case of resistive load in comparison to inductive and capacitive loads. In case of inductive and capacitive loads, the peak value of the output current does not coincide with the peak value of the output voltage. The phase shift between output voltage and load current of the inverter reduces the rate of discharging of the capacitor. It may be

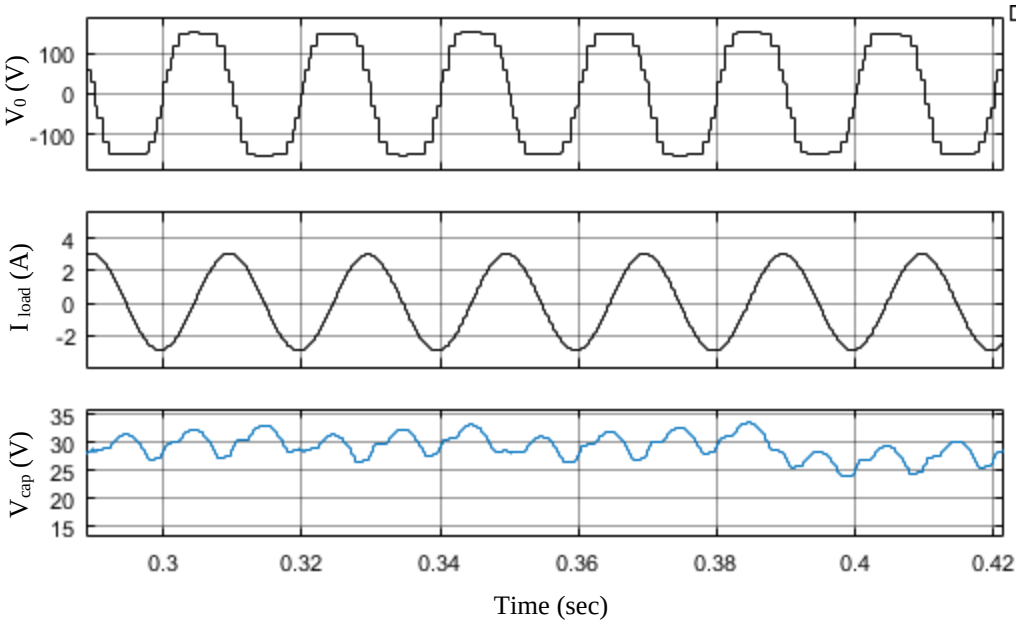


Fig. 2.21 Simulation results at m_a = 1.1 for inductive load.

concluded that if the constraint satisfies for resistive loads, it also satisfies for inductive and capacitive loads. In case of highly inductive loads, it is possible to keep the charge of the capacitor at the desired level even at higher modulation index, even if the constraint derived in (2.31) is not satisfied. The simulation is carried out for m_a = 1.1 for inductive load to observe the effects of regulation in capacitor voltage. The inductive load consists of (R=12 Ω and L=80 mH). Simulation results for the said load conditions are shown in Fig. 2.21. It can be observed from Fig. 2.21 that the capacitor voltage is regulated in this case. For resistive load, the same simulation results are shown in Fig. 2.22. It may be noted that the capacitor voltage regulation is not possible at m_a =1.1 in case of resistive load. Hence, it is always possible to balance the capacitor voltage in case of highly inductive loads even at higher values of m_a. For each individual value of power factor, the balancing of the capacitor is checked for the entire range of modulation indices and the maximum modulation index for each power factor is as shown in Fig. 2.23.

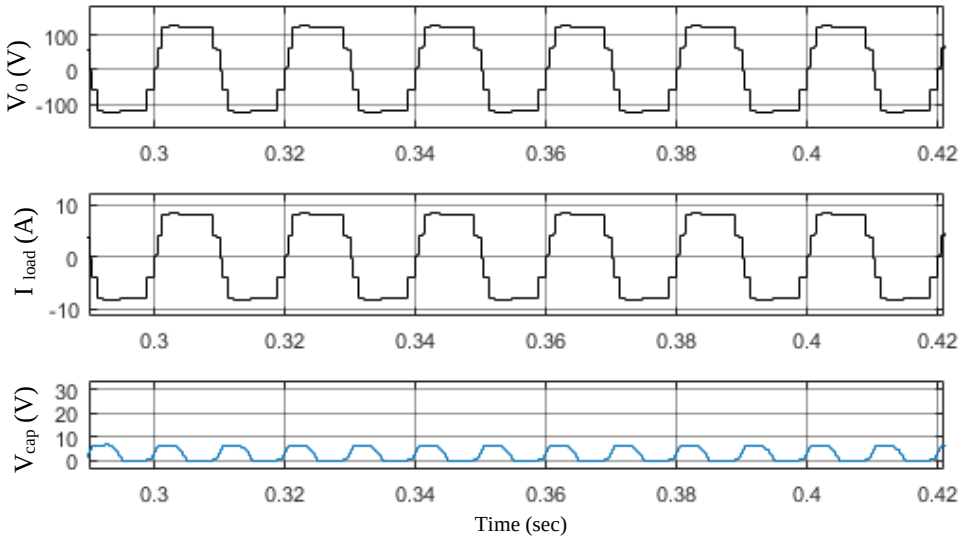


Fig. 2.22 Simulation results at m_a = 1.1 for resistive load.

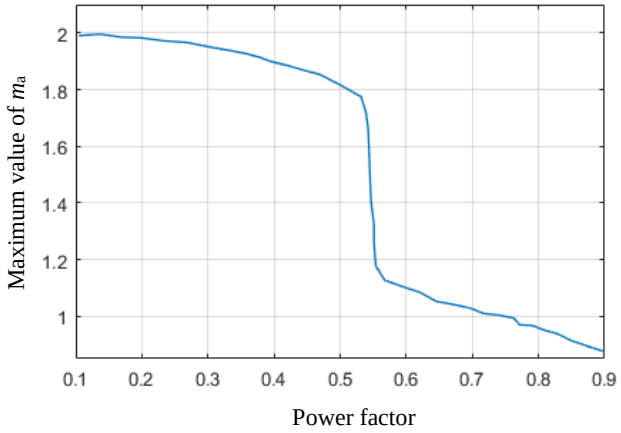


Fig. 2.23 Effect of power factor on capacitor voltage balancing.

Table 2.7
Components Used for Experiment

Components	Manufacturer
IGBT Modules	SK50GBO63D (Semikron)
IGBT Gate Driver	SKYPER 32R (Semikron)
Heat Sink	P3/250 mm
Optocoupler	FOD3182 (Fairchild)
Voltage Sensor	LV 55P (LEM)
Current Sensor	LA 25P (LEM)
OPAMP	LM3124n (IR Corporation)
DSP	TMS320F28335 (TI)

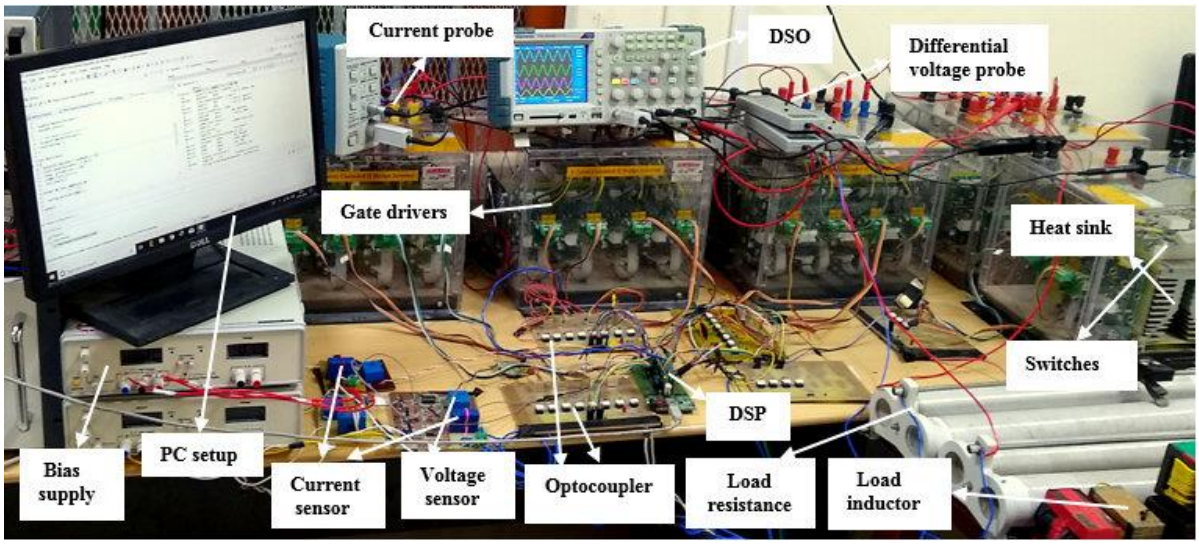


Fig. 2.24 Photograph of the experimental setup (11-level HC-MLI).

2.10 Experimental Verification

Fig. 2.24 shows the photograph of experimental setup. The control scheme has been implemented using a TI-TMS320F28335 DSP processor [109]. List of parameters used for experimentation are given in Table 2.7. In the experiments, the primary H-bridge cells (H_1, H_2) are fed by 60 V DC sources and 350 mF capacitor is connected to the supplementary H-bridge (H_3). The capacitor voltage (V_{CAP}) is 30 V. The sensed capacitor voltages (V_{CAP}) of the respective three-phases phase *A*, phase *B* and phase *C* are fed back to the ADC of DSP through a signal conditioning circuit. The sensed average capacitor voltage is compared with the reference value and given to the embedded code logic block of MATLAB/Simulink. The direction of the load current is sensed using a current sensor for capacitor voltage balancing at available redundancies. The capacitor voltage balancing is investigated experimentally for higher range of modulation indices. The output phase voltages (V_A, V_B, V_C) at $m_a = 0.55$ are shown in Fig. 2.25(a). The measured rms values of phase voltages (V_A, V_B, V_C) are 71.8 V. The performance of the HC-MLI has also been investigated for *R-L* load. The output voltage

V_A and output current I_L obtained through experiments for *R-L* load at m_a=0.55 is shown in Fig. 2.25(b). Fig. 2.25(c) and (d) shows the phase voltage (V_A) and phase voltages (V_A, V_B, V_C) at m_a = 1.2. The measured rms value of phase voltage (V_A) is 110.6 V. The experimental result confirms that capacitor voltage balancing is achieved at higher modulation index. It can be observed that capacitor voltage is maintained at 30 V. Table 2.8 shows the magnitudes of lower order harmonics at different modulation index. Harmonic magnitudes are within IEEE Std 519-2014 [110].

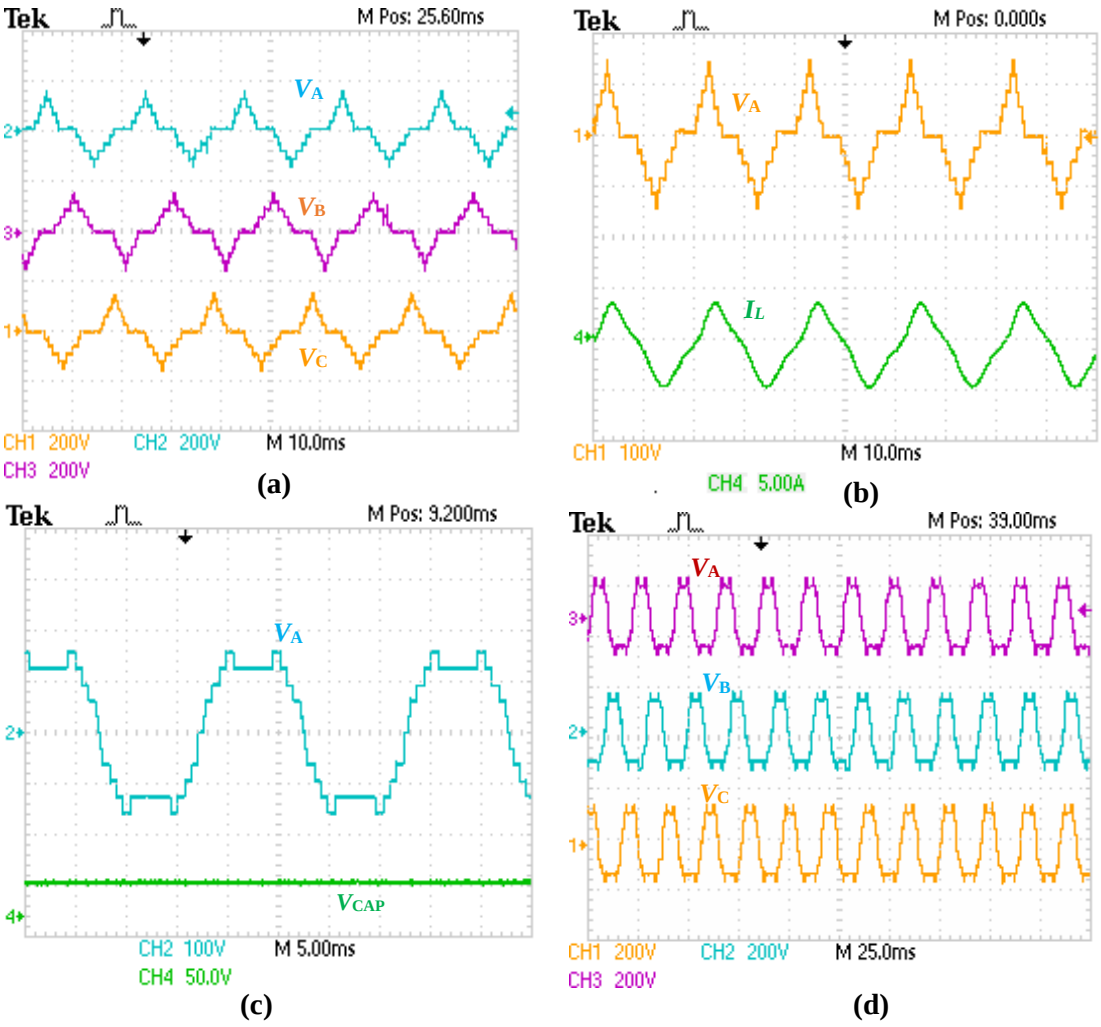


Fig. 2.25 Experimental results of the HC-MLI (Phase voltages).
(a) Phase voltages (V_A, V_B, V_C) at m_a = 0.55. (b) Phase voltage (V_A) for *R-L* load at m_a = 0.55. (c) Phase voltage (V_A) at m_a = 1.2 (3rd harmonic injected). (d) Phase voltages (V_A, V_B, V_C) at m_a = 1.2.

The experimental results of line voltage (V_{AB}) at m_a=0.55 and its harmonic spectrum are shown in Fig. 2.26(a) and (b). The measured rms value of line voltages is 118.5 V. It is observed from Fig. 2.26(b) that 5th,7th,11th and 13th order harmonics are eliminated from the output voltage of the HC-MLI. The experimental results of line-line voltages (V_{AB}, V_{BC}, V_{CA}) at m_a = 0.55 and m_a = 1.2 are shown in Fig. 2.26(c) and (d) respectively. Fig. 2.27(a) shows the steady state output voltage V_{AB} and load current I_L along with capacitor voltage V_{CAP}. The output voltage is maintained at 84.82 V for load current of 17 A by closed loop control. Fig. 2.27(b) shows the harmonic spectrum of V_{AB} at m_a = 0.55 after connecting LC filter. Table 2.9 shows the magnitudes of lower order harmonics at different modulation indices.

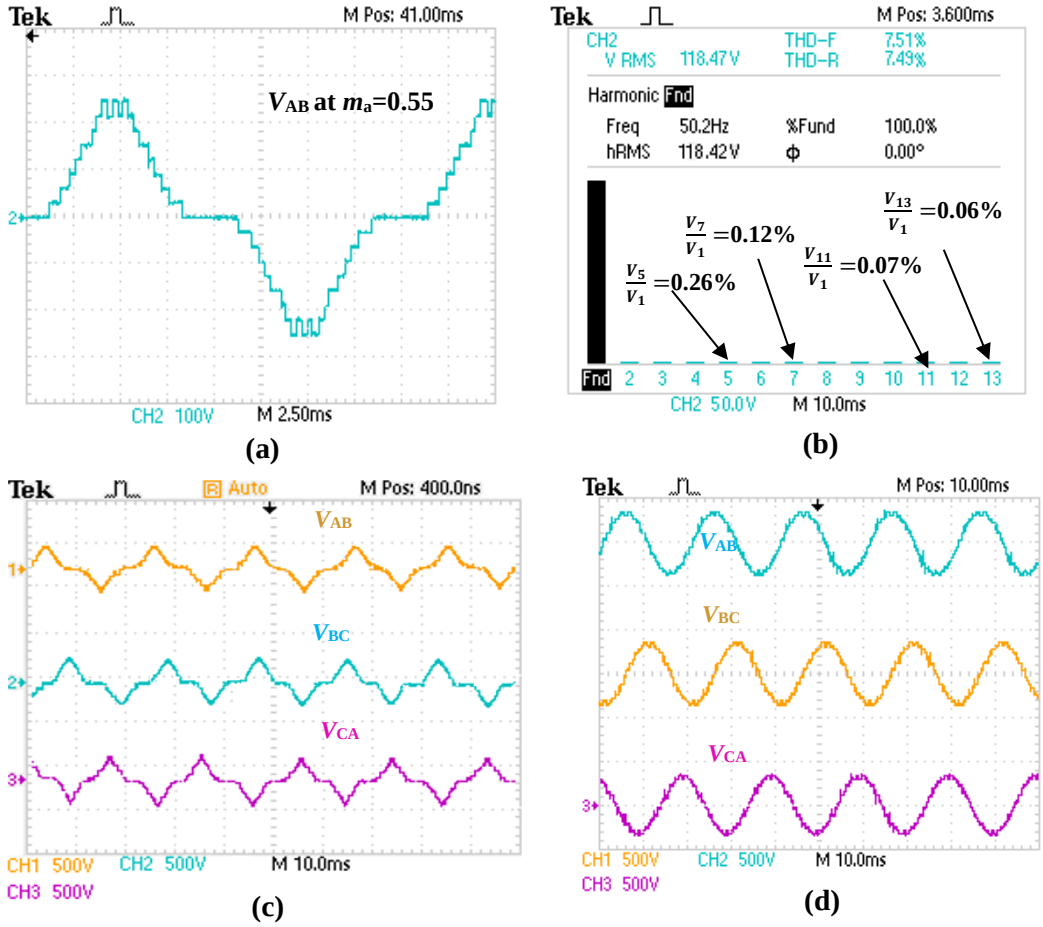


Fig. 2.26 Experimental results of the HC-MLI (Line voltages).
(a) Line voltage (V_{AB}) at m_a = 0.55. (b) Harmonic spectrum of V_{AB} at m_a = 0.55. (c) Line voltages (V_{AB}, V_{BC}, V_{CA}) at m_a = 0.55. (d) Line voltages (V_{AB}, V_{BC}, V_{CA}) at m_a = 1.2.

Table 2.8
Harmonic Magnitudes and % THD of V_{AB} Through Experiment at Different Modulation Indices

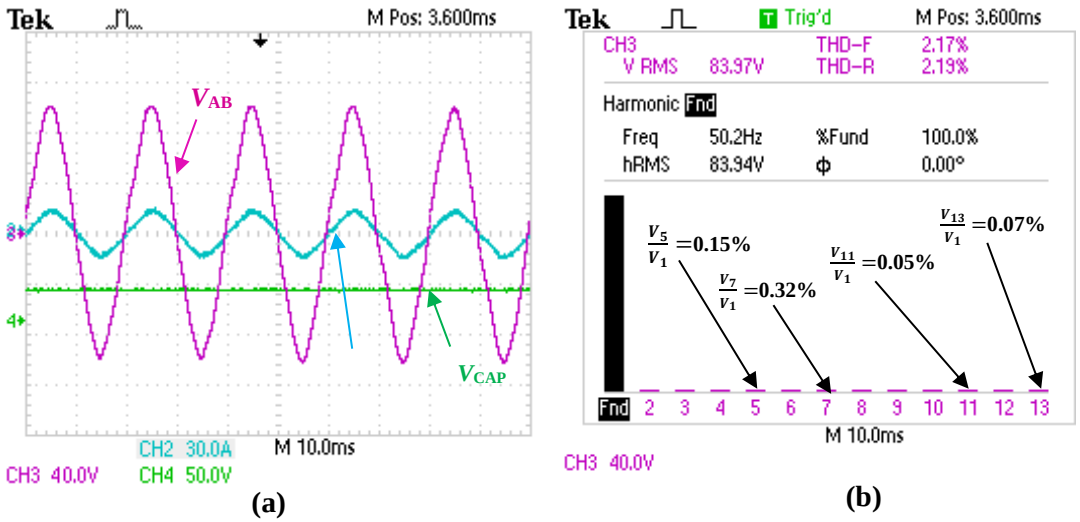
Modulation index	%h5	%h7	%h11	%h13	%THD
0.5	0.25	0.08	0.27	0.31	8.71
0.6	0.30	0.18	0.07	0.09	7.67
0.7	0.55	0.68	0.10	0.47	7.83
0.8	0.14	0.09	0.11	0.06	5.47
0.9	0.12	0.08	0.43	0.09	4.35
1	0.26	0.15	0.18	0.19	5.09
1.1	0.67	0.37	0.07	0.08	6.03
1.2	0.62	0.45	0.13	0.07	6.51

Table 2.9
Harmonic Magnitudes and %THD of line voltage V_{AB} at Different Modulation Indices

Modulation index	% h5	% h7	% h11	% h13	%THD
0.5	0.42	0.77	0.68	0.50	3.12
0.6	0.15	0.32	0.05	0.07	2.14
0.7	0.16	0.73	0.12	0.04	2.31
0.8	0.2	0.53	0.16	0.15	2.04
0.9	0.15	0.53	0.1	0.07	1.09
1	0.41	0.16	0.36	0.22	1.29
1.1	0.33	0.52	0.18	0.11	2.03
1.2	0.15	0.31	0.09	0.06	2.29

Table 2.10
Experimental %THD Comparison of Different Algorithms

Modulation index	%THD (MPSO)	%THD (PSO)	%THD (GA)
0.5	8.51	10.73	13.89
0.6	7.62	9.25	12.52
0.7	7.73	9.67	12.91
0.8	5.28	7.51	11.41
0.9	4.21	6.11	10.91
1	5.09	7.13	9.92
1.1	5.71	7.76	8.13
1.2	6.25	8.08	9.41



(a) (b)

Fig. 2.27 Experimental results of the HC-MLI after connecting LC filter.
(a) Line voltage (V_{AB}) with load current (I_L) and capacitor voltage (V_{CAP}) at m_a = 0.55.
(b) Harmonic spectrum of (V_{AB}) at m_a = 0.55.

It is worth mentioning that the harmonic magnitudes are well within IEEE Std 519-2014 [110]. Table 2.10 gives the comparison of experimentally obtained % THD at different modulation indices. The proposed MPSO gives improved result as compared to other reported algorithms. The output voltage and output current for *R-L* load (R=12 Ω and L= 37 mH) obtained through experiment are shown in Fig. 2.28. The algorithm has been experimentally verified in real time for step change in m_a from 0.5 to 0.6 as shown in Fig. 2.29.

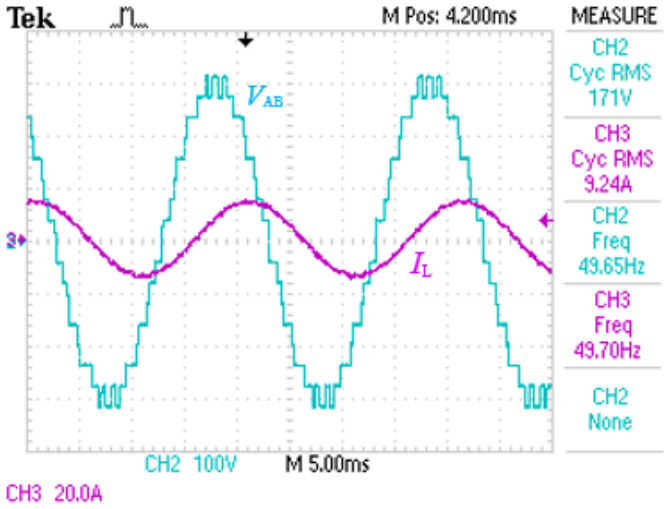


Fig. 2.28 Experimental result of HC-MLI of output line voltage versus load current for inductive load (R=12 Ω and L= 37 mH).

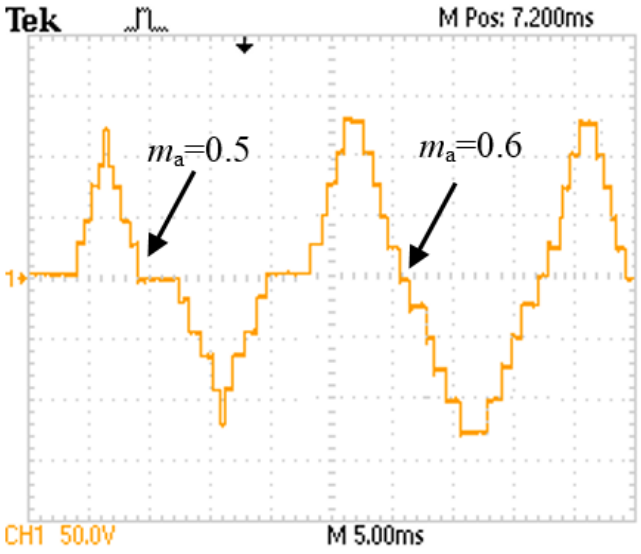


Fig. 2.29 Real time implementation of controller during step-change in m_a from 0.5 to 0.6.

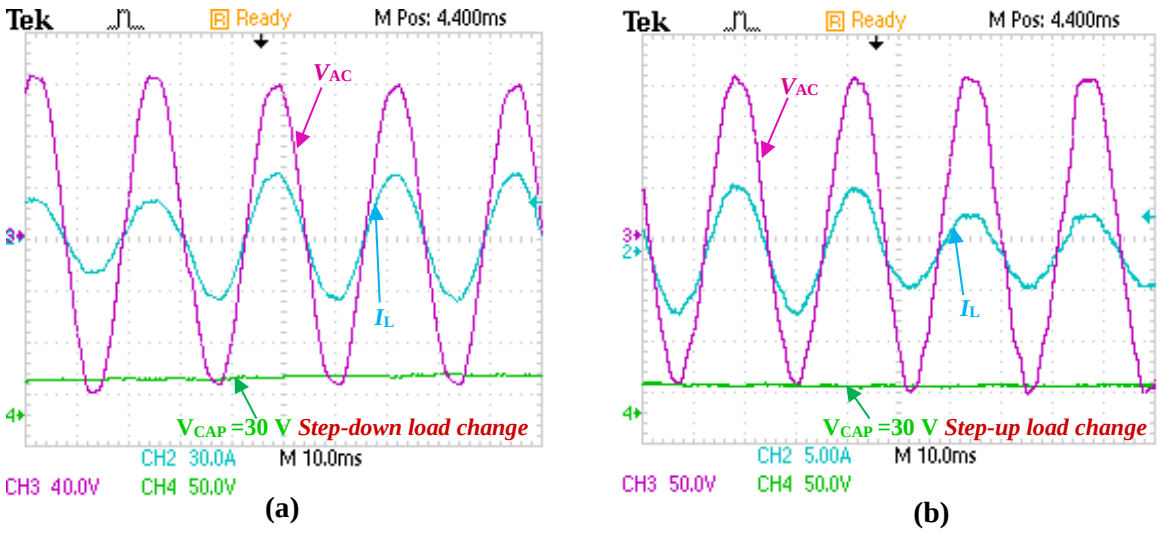


Fig. 2.30 Dynamic results of HC-MLI.
(a) 50% step-down change in load (b) 50% step-up change in load.

2.10.1 Dynamic Performance of HC-MLI

In order to validate the dynamic performance of the HC-MLI and capacitor voltage balance during load change, the output resistance is suddenly changed from 10 Ω to 5 Ω. It can be observed from Fig. 2.30(a) that after step-down change in load resistance, the load current increases from 9 A to 17 A but the output voltage (V_{AC}) and capacitor voltage (V_{CAP}) are maintained at 84.82 V and 30 V respectively. Similarly, Fig. 2.30(b) shows that during step-up load change and load current from decreases from 17 A to 9 A, output load voltage and capacitor voltage are also maintained constant.

2.11 Conclusion

This chapter presents MPSO optimized three-phase, 11-level HC-MLI using SHE-PWM technique. Improvements in weight and velocity factors in MPSO take care of local optima efficiently in this method leading to better convergence rate and reduced harmonic content. The proposed MPSO optimized HC-MLI ensures capacitor voltage balance even at higher modulation indices by utilizing the available redundancies of HC-MLI. It has been

demonstrated that the capacitor voltage balance in HC-MLI can be achieved even at higher modulation indices using harmonic injection method. Simulation and experimental studies are carried out to demonstrate steady state and dynamic performance of the proposed MPSO optimized three-phase HC-MLI. The proposed MPSO optimized SHE-PWM gives better results in terms harmonic content and convergence rate as compared to GA and PSO algorithms. In order to further improve the performance of HC-MLI, in terms of speed of convergence and harmonic content, a modified whale optimization (MWO) algorithm has been proposed in the next chapter.