Chapter 1

Introduction

1.1 Background and Motivation

Increasing higher power quality requirements in industrial applications and renewable energy sources such as photovoltaic, wind and fuel cell, classical three-level inverters have limitations in meeting the requirements of clean non-polluted sinusoidal waveforms with minimal distortion. To generate nearly sinusoidal waveform with low distortion, multilevel inverters (MLIs) have been evolved and have drawn much attention in medium and high voltage power applications [1]-[10]. The basic concept of MLIs is to perform the power conversion by synthesizing staircase voltage waveforms from input DC sources. Several low voltage DC capacitors, batteries and renewable energy voltage sources are used as input to the MLIs. The commutation of the power switches aggregates these multiple DC sources to achieve required AC voltage at the output. The rated voltage of the power switches depends only on the rating of the DC voltage sources to which they are connected. The attractive features of MLIs can be summarized as

- **Staircase waveform quality and modularity**

  MLIs generate staircase output voltages with very low distortion at reduced *dv/dt* stress, hence electromagnetic interference is reduced.

- **Common-mode voltage**

  MLIs generate reduced common-mode voltage and this can be further reduced using advanced modulation strategies.

- **Input current**

  MLIs draw input current with low distortion.

- **Switching frequency**

  MLIs can also operate at fundamental switching frequency leading to lower switching loss and higher efficiency.

Due to aforementioned advantages, MLIs have been widely utilized in many applications such as renewable energy [3], [4], flexible AC transmission systems, static compensators [5], dynamic voltage restorers, unified power flow controllers, active power filters [7], solid state transformers [8], motor drives, marine propulsion, mine hoists, conveyors, uninterred power supplies and fans/pumps [7]-[10].

1.2 Literature Review

Many MLI topologies have been proposed during the last two decades. MLIs are categorized according to number of DC sources used, such as common DC source and separate DC source based MLIs, as shown in Fig. 1.1. The common DC source based MLIs are diode clamped (neutral clamped) MLI [10]-[16] and flying capacitor (capacitor clamped) MLI [17]-[19]. The cascaded H-bridge MLIs [20]-[28], hybrid cascaded H-bridge [29]-[34] and switched capacitor MLIs [35]-[63] utilize separate DC sources to generate the output voltage levels. Different pulse width modulation (PWM) techniques have been reported to control the output voltage of MLIs, which are sinusoidal PWM (SPWM), selective harmonic elimination PWM (SHE-PWM), selective harmonic mitigation PWM, SHE pulse amplitude modulation and space vector modulation (SVM). This chapter reviews the state of the art of MLIs, their different structures and the different PWM schemes used in MLIs with their relative advantages and disadvantages.

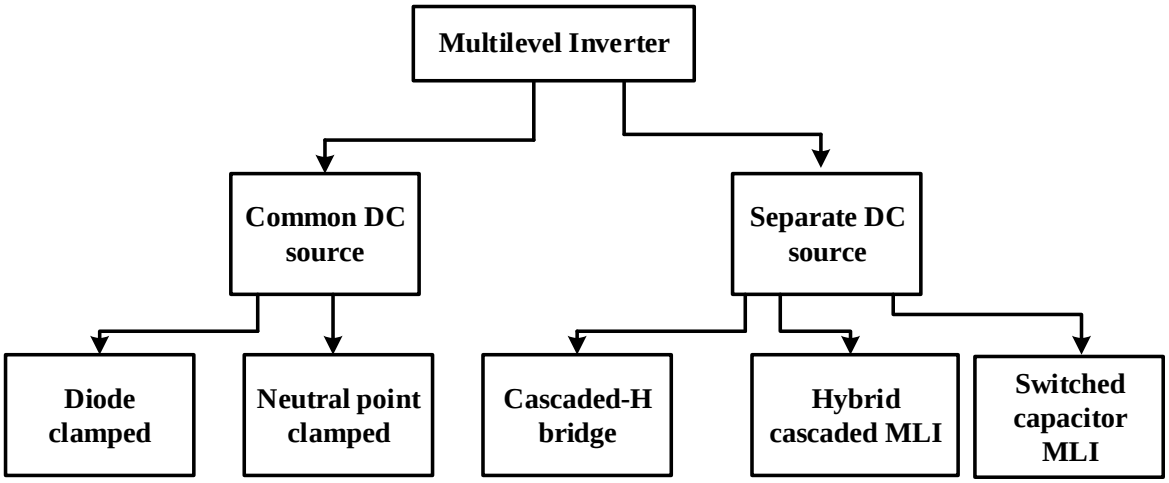


Fig. 1.1 Multilevel inverter topologies.

1.2.1 Neutral Point Clamped MLI

The neutral point clamped MLI (NPC-MLI) is also known diode clamped MLI, which consists of four pair of switches (upper and lower arm) as shown in Fig. 1.2 [10]. The switches are in parallel with series connected capacitors. The positive end of diode is connected to neutral point (O) of NPC-MLI and negative end is connected to the midpoint of upper or lower arm switches.

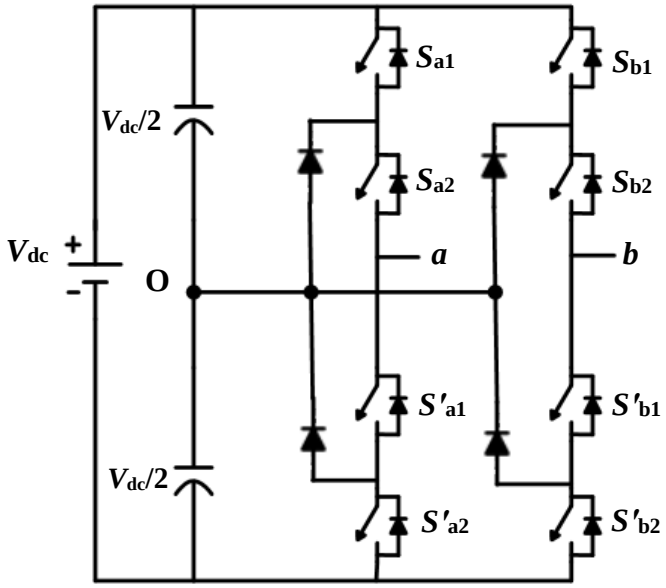


Fig. 1.2 Neutral point clamped MLI [10].

For a three-level NPC-MLI, as shown in Fig. 1.2, the generated output voltage levels are 0, $+1/2V_{dc}$ and $-1/2V_{dc}$.

The NPC-MLI has following advantages:

- All phases share a common DC bus voltage, which minimizes the number of capacitors required.
- Its efficiency is high, when operates at fundamental switching frequency.
- The capacitors can be pre-charged.

The NPC-MLI, however has following limitations:

- The number of diodes increases quadratically with number of voltage levels.
- Real-power flow is difficult to control as DC voltage levels fluctuate without precise control.
- Different current ratings of the switching power devices are required due to difference in conduction periods of devices.

1.2.2 Flying Capacitor MLI

A single-phase five level flying capacitor MLI (FC-MLI), also known as capacitor clamped MLI is shown in Fig. 1.3 [17]. The FC-MLI provides more flexibility in output voltage synthesis and capacitor voltage balancing. The voltage difference between the capacitors regulates the magnitude of output voltage levels.

The existing redundancy in switching states regulates the voltage of capacitor and obtain required voltage level. In the present circuit, switches S_{a1}, S_{a2} and S'_{a1}, S'_{a2} are complementary to each other. The voltage of capacitor is maintained at $V_{dc}/2$. The generated five level output voltage levels in FC-MLI are $+V_{dc}$, $+ V_{dc/2}$, 0, $-V_{dc}$ and $-V_{dc/2}$. In FC-MLI, the output voltage is generated by utilizing different combinations of switches.

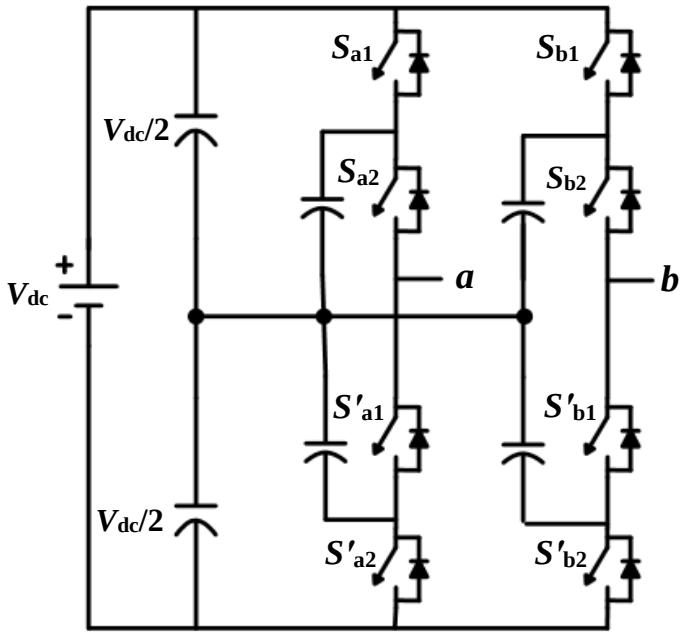


Fig. 1.3 Flying capacitor MLI [17].

The different switching combinations are used to charge or discharge the capacitors, which helps in balancing of capacitor voltages. The advantages of FC-MLI are as follows:

- Redundancies are available for balancing the voltage levels of the capacitors.
- Active and reactive power flow can be controlled.

FC-MLI, however has some disadvantages also, which are:

- The large number of capacitors makes the overall system expensive and bulkier.
- Packaging is more difficult with higher number of voltage levels.
- Complex control is required to maintain the voltages across capacitors.

1.2.3 Cascaded H-Bridge MLI

CHB-MLI uses series connected H-bridge inverters to generate several voltage levels, as shown in Fig.1.4 [20]. The output of each H-bridge has three discrete voltage levels such as $+V_{dc}$, 0 and $-V_{dc}$, which results into a staircase waveform. A single-phase five level CHB-MLI generates voltages $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$ respectively.

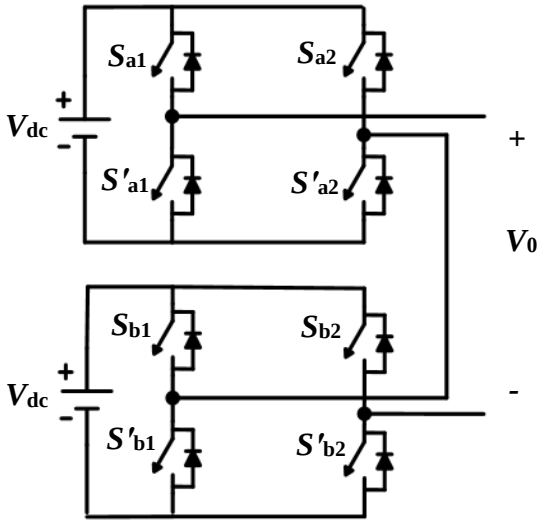


Fig. 1.4 Cascaded H-bridge MLI [20].

The switches S_{a1}, S_{a2}, S'_{a1}, S'_{a2} and S_{b1}, S_{b2}, S'_{b1}, S'_{b2} are used to generate five different voltage levels such as $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$. When four switches S_{a1}, S'_{a2}, S_{b1} and S'_{b2} are turned ON, the output voltage level is $2V_{dc}$ obtained; when S_{a1} and S'_{a2} or S_{b1} and S'_{b2} are ON, the generated voltage level is V_{dc}; when either pair S_{a1} and S_{a2}, or S_{b1} and S_{b2} are ON, the voltage level is 0. Switch pairs S_{a1}, S'_{a1} and S_{b1}, S'_{b1} are complementary to each other. The voltage levels can be increased by including identical inverters in cascade.

The advantages for CHB-MLI are as

- It can be easily extended to obtain higher voltage levels and control circuit is simple.
- Clamping diodes and balancing capacitors are not required.

However, CHB-MLI has a disadvantage that separate DC sources are required for each of the H-bridges. This limits its application and increases the cost.

1.2.4 Hybrid Cascaded MLI

To reduce the number of DC sources and switches in CHB-MLIs, hybrid cascaded MLI (HC-MLI) has been proposed. HC-MLIs use a single DC voltage source and the remaining DC

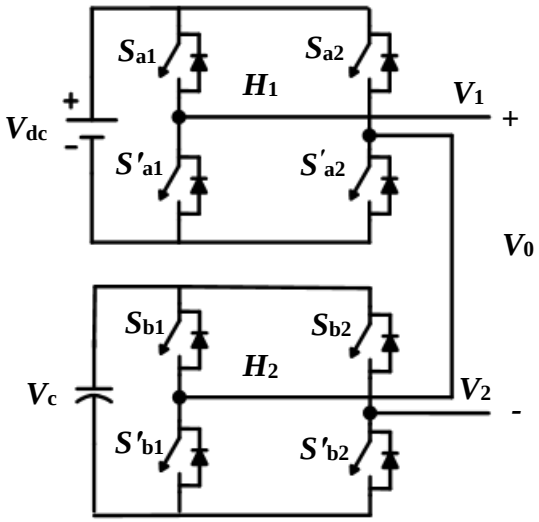


Fig. 1.5 Hybrid cascaded MLI [29].

sources are replaced by capacitors, as shown in Fig. 1.5 [29]. The DC source of the first H-bridge (H_1) is a battery or fuel cell, which generates output voltage of V_{dc}, while the DC source of the second H-bridge (H_2) is a capacitor, whose voltage is held at V_C.

The output voltage of the first H-bridge is denoted by V_1 and the output of the second H-bridge is denoted by V_2, so that the output voltage of HC-MLI is $V_0 = V_1 + V_2$. By using the switches of H_1 properly, the output voltages are $+V_{dc}$, 0 and $-V_{dc}$, while the output voltage of H_2 are $+V_c$, 0 and $-V_c$. Hence, the output voltage of HC-MLI can have the values $+(V_{dc} + V_c)$, $+V_{dc}$, $+V_c$, 0, $-V_c$, $-V_{dc}$ and $-(V_{dc} + V_c)$, which constitute 7 possible output voltage levels. A 7-level output voltage is generated through voltage steps $+3V_{dc}/2$, $+V_{dc}$, $+V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$ and $-3V_{dc}/2$, when the capacitor's voltage V_c is chosen as $V_{dc}/2$.

The HC-MLI have some disadvantages which are as follows:

- As HC-MLI uses capacitors and DC sources, balancing of capacitor voltages is an inherent problem in these topologies.
- The possibility of extending the number of output voltage levels is not feasible in HC-MLIs.

1.2.5 Switched Capacitor MLI

SC-MLIs have been reported to mitigate the use of large number of circuit components and the challenges of capacitor voltage balancing in conventional MLIs [35]-[60]. The SC-MLIs use capacitors in combination with power switches in a specific way to generate the output voltage. Using different circuit configurations and connections of switched capacitor (SC) cell can generate high or low-voltage gains. The low-voltage gain SC-MLI has a simple structure with fewer elements and also its control is simple. On the contrary, high-voltage gain SC-MLIs have bulky circuit due to the use of multiple SC circuits. The basic circuit of SC cell consists of switches, diodes and capacitors as shown in Fig. 1.6(a) [38]. The DC voltage source is connected to capacitor *C* using switches *S* and *P*. The switches *S* and *P* have opposite operation. When switch *S* is switched ON, switch *P* is OFF and vice versa. Fig. 1.6(b) and (c) shows different the operation modes of basic unit of SC cell. In the positive half cycle, when switch *P* is switched ON, the diode *D* is forward biased and capacitor *C* is charged to input DC voltage, shown in Fig. 16(b). During the second half of cycle, when switch *S* is turned ON, capacitor *C* starts discharging and diode *D* becomes reverse-biased. The voltage source is connected in series with the previously charged capacitor *C*. So, the two voltages are added to generate $V_L = V_{dc} + V_c$, as shown in Fig. 16(c). In order to obtain higher voltage levels, multiple units of SC cells are connected in cascade.

A switched capacitor based 9-level circuit is made up of a SC cell at front end and cascaded H-bridge at back end is shown in Fig. 1.7 [39]. If the numbers of voltage levels obtained by SC cell at front end and cascaded H-bridge back end are N_1 and N_2 respectively, then the number of obtained voltage levels are $(2\times N_1\times N_2) +1$ in entire operation cycle. The switches S_1, S_2, S'_1 and S'_2 of SC cells (SC_1 and SC_2) connect the capacitors C_1 and C_2 with the voltage source V_{dc1} and V_{dc2} in series or parallel to generate the output voltage levels.

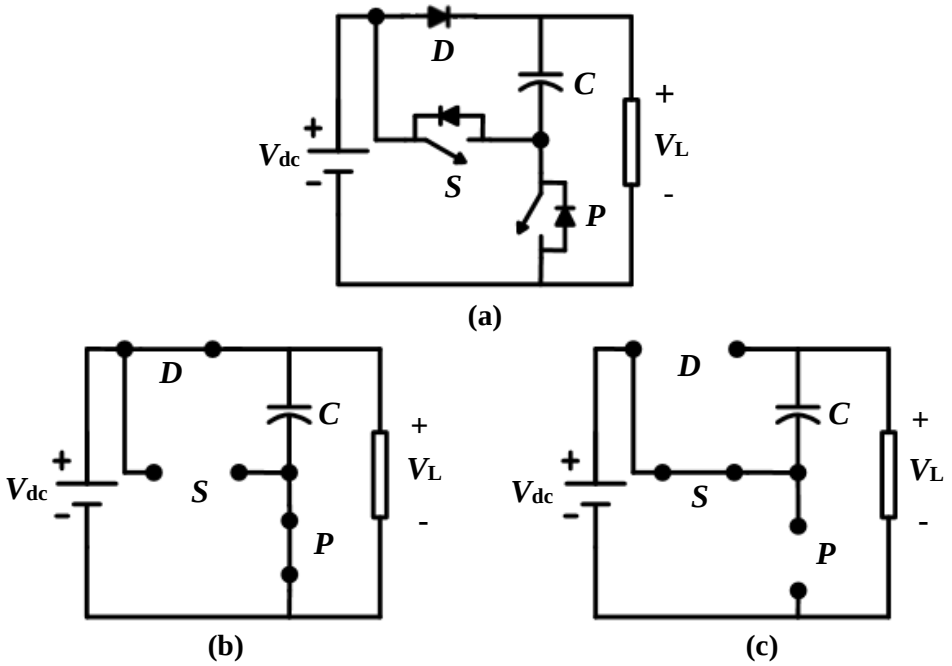


Fig. 1.6 SC cell operation. (a) Basic unit of SC cell. (b) Capacitor charging. (c) Capacitor discharging [35].

The switches S_{1a}, S_{1b}, S_{1c}, S_{1d}, S_{2a}, S_{2b}, S_{2c} and S_{2d} of the cascaded H-bridge are used for polarity generation of the output voltage and the diodes D_1 and D_2 are used to restrict the current direction.

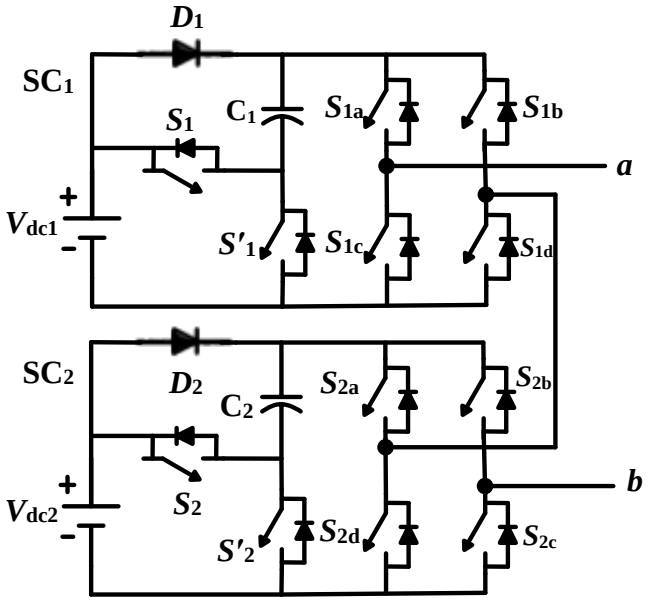


Fig. 1.7 Cascaded switched capacitor MLI [39].

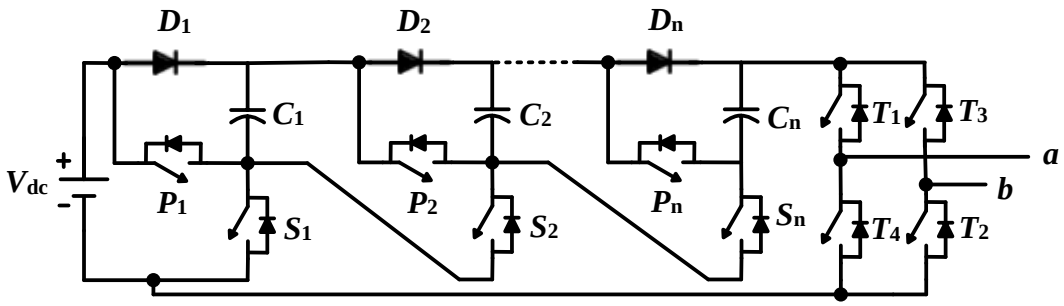


Fig. 1.8 Switched capacitor cell [38].

One of the major limitations of the said SC-MLI is that it requires higher number of DC sources and power switches to generate output voltage levels and this limitation increases at higher voltage levels. As the PIV of switches becomes high, the application of the said SC-MLI is restricted.

In order to achieve higher voltage gain using reduced the number of DC voltage source, another SC-MLI has been proposed in [38], as shown in Fig. 1.8. This proposed SC-MLI uses the series combination of different basic SC cells to generate multiple voltage levels. The capacitors are connected in series using switches S_i (i = 1, 2, . . ., n) and in parallel with the voltage sources by the use of switches P_i (i = 1, 2, . . ., n). An H-bridge is used at the front end to generate polarity. One of the advantages of the proposed topology is that the voltage blocked by each switch is limited to input voltage V_{dc}. The other advantage of the proposed SC-MLI is its high voltage boosting capability due to cascaded connection of several SC cells. However, the reported SC-MLI requires large number of power switches to generate the output voltage at higher voltage levels and the PIV of switches are also high due to the presence H-bridge.

Subsequently, another single sourced SC-MLI with front end H-bridge is proposed in [40], as shown in Fig. 1.9, where in each SC cell consists of a capacitor, an active switch and two diodes. The output voltage levels of the proposed SC-MLI can be changed by utilizing

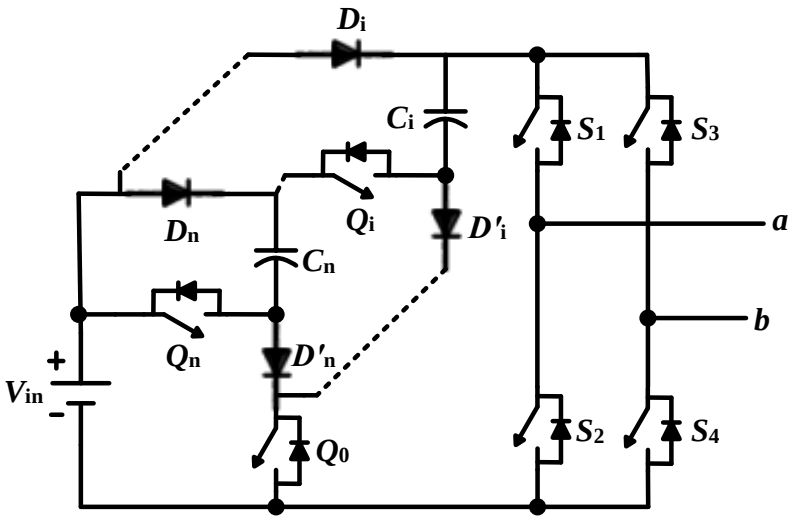


Fig. 1.9 Topology of the proposed switched capacitor MLI [40].

different SC cells. A total of $2n + 3$ voltage levels 0, $\pm V_{in}$, $\pm 2V_{in}$, ..., $\pm (n + 1) V_{in}$ can be generated using the proposed topology, where n is the number of SC cells. To obtain zero voltage level, Q_0 is turned ON, while the other switches are in OFF condition. The voltage across capacitors C_i are equal to input voltage V_{in}, i.e., $V_{Ci} = V_{in}$ ($i = 1, 2, \ldots, n$), when switches S_1 and S_4 are turned ON and S_2 and S_3 are in OFF condition. Similarly, when S_2 and S_3 are ON and S_1 and S_4 are OFF, the generated output voltage is $-V_{in}$. One of the major advantages of this SC-MLI is that it requires a single DC voltage source to produce output voltage levels. However, the total standing voltage (TSV) and peak inverse voltage (PIV) of the proposed SC-MLI increases drastically for higher number of voltage levels, which restricts its applications.

To reduce the number of active/passive components and obtain comparatively higher voltage gain, a new high step-up SC-MLI has been proposed in [54], as shown in Fig. 1.10. The proposed SC-MLI has two separate DC sources (V_{S1} and V_{S2}) along with several SC cells in each side of H-bridge. When the switch T_1 is ON, the capacitor C_1 is connected in parallel with the DC voltage source V_{S1} and C_1 is charged to V_{S1}.

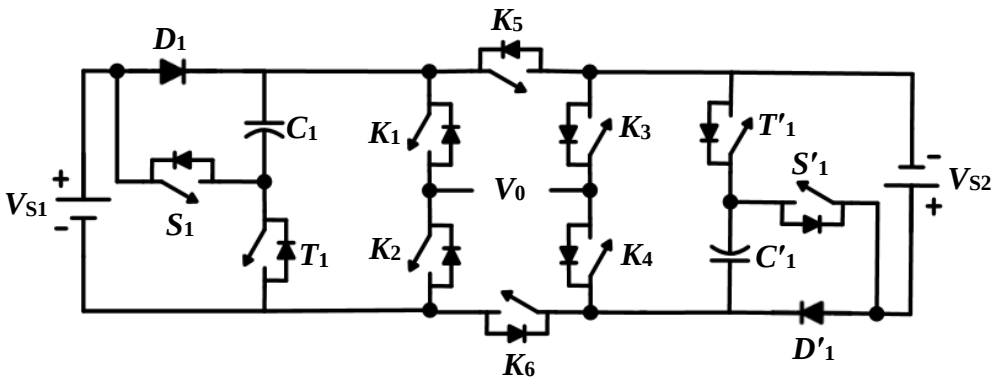


Fig. 1.10 Proposed switched capacitor-based unit [54].

Similarly, when the switch T'_1 the capacitor C'_1 charged to V_{S2}. When switches S_1 and S'_1 are in ON, both the capacitors C_1 and C'_1 are in series with V_{S1} and V_{S2} to generate high voltage gain. The switches K_1-K_5 of H-bridge module are used for voltage addition and polarity generation in SC-MLI. In this topology, higher number of voltage levels are obtained using lesser number of passive components. However, the number of DC sources required is high which leads to increased cost and restricted operation.

1.3 Pulse Width Modulation (PWM) Techniques for Control of MLI

Different pulse width modulation (PWM) techniques are reported in literature for the control of the output voltage of MLIs and reducing the distortion in it [64]-[76]. They are classified according to their switching frequency as

- High switching frequency PWM
- Fundamental switching frequency PWM

The well-known high switching frequency PWM techniques for the control of MLIs are multicarrier sinusoidal pulse width modulation (SPWM) [64] and space vector PWM (SVM-PWM) [66]. The fundamental switching frequency PWM methods are selective harmonic elimination PWM (SHE-PWM) and space vector modulation (SVM). The different modulation techniques are shown in Fig. 1.11.

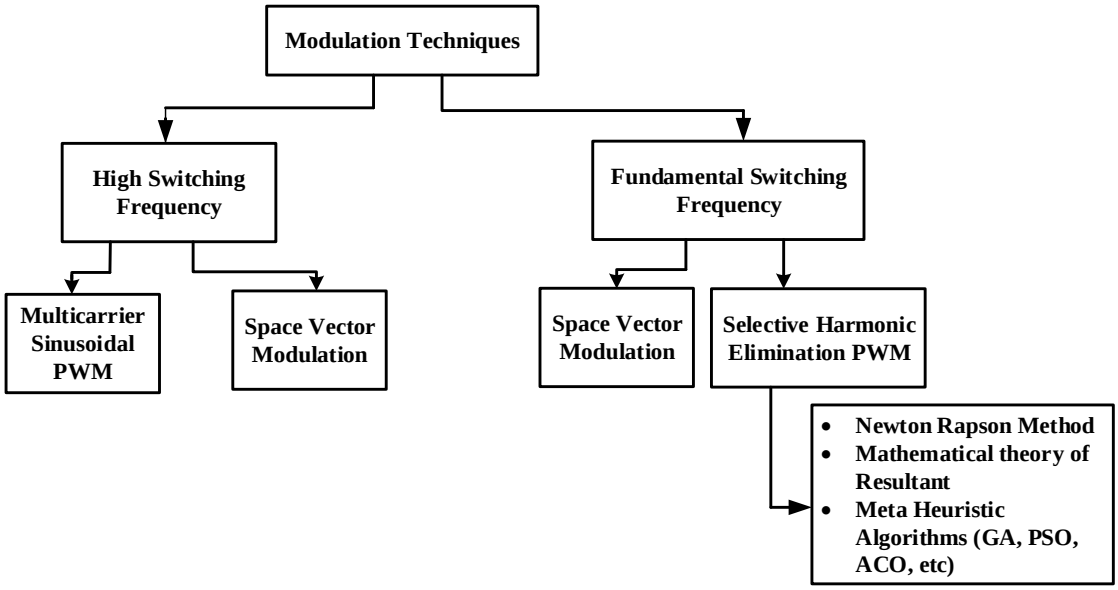
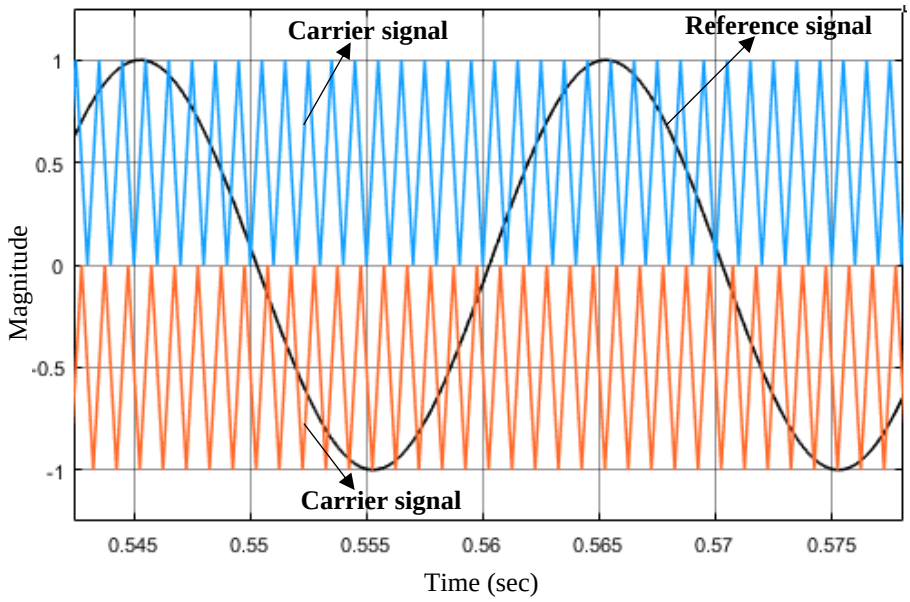


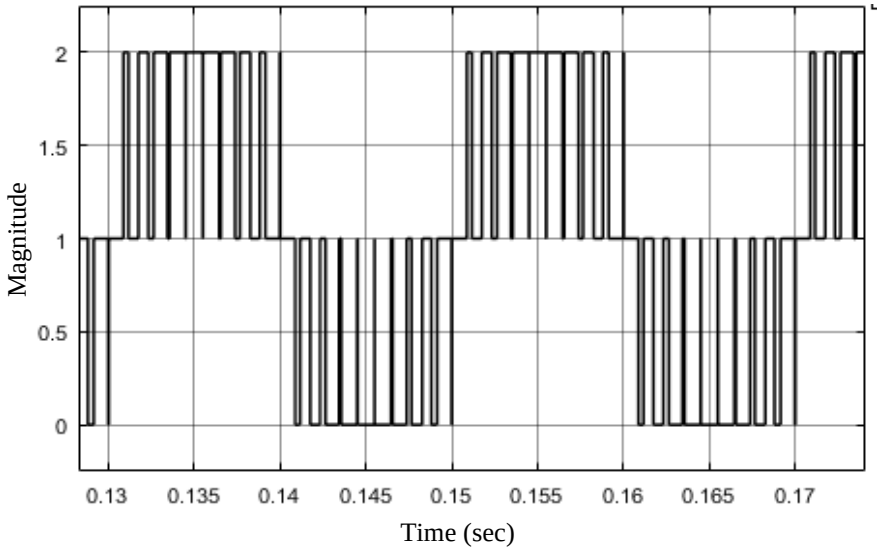
Fig. 1.11 PWM techniques for the control of MLIs.

1.3.1 Multicarrier SPWM

Different multicarrier SPWM techniques have been developed over the years to reduce the distortion in the output voltage of MLIs based on phase shifting and disposition of several carrier signals [70]-[75]. In SPWM, a reference signal is used to compare the carrier signals. If the reference signal is higher than the carrier signal, the output voltage is positive, otherwise it negative as shown in Fig. 1.12. One of the major advantages of multicarrier SPWM is that the switching frequency of the output voltage is the number of cascaded cells used times the switching frequency of each cell. Hence, the switching frequency of each cell decreases, which reduces the switching loss. However, the major limitation of multicarrier SPWM is that it cannot totally mitigate the low order dominant harmonics and thus additional filters are required at the output end of the MLIs.



(a)



(b)

Fig. 1.12 Multicarrier SPWM. (a) Reference signal and carrier signals. (b) Output voltage.

1.3.2 Space Vector Modulation PWM

SVM-PWM is one of the popular modulation techniques to regulate the output voltage of MLIs [66]. Fig. 1.13 shows basic diagram of SVM for conventional three-level MLI. In SVM-PWM, the output voltage is obtained as weighted mean of three different vectors in *d*-*q* reference frame. The reference voltage vector is generated by switching the three adjacent

voltage vectors and these vectors synthesize the required voltage vector by calculating the duty cycle of each the vectors using

$$\vec{V} = \frac{\vec{V}_J\vec{T}_J+\vec{V}_{J+1}\vec{T}_{J+1}+\vec{V}_{J+2}\vec{T}_{J+2}}{T} \quad (1.1)$$

where V_J, T_J are voltage and time vectors and T is the total time.

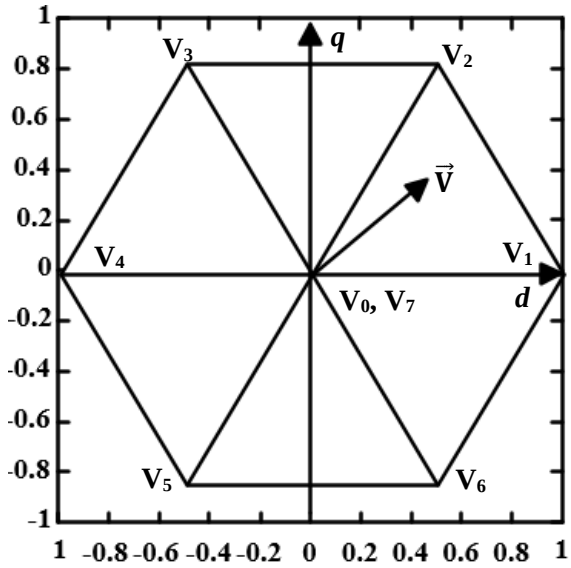


Fig. 1.13 Vector diagram of SVM-PWM [76].

Generally, SVM is relatively easy to control and flexible in improving the switching's per cycle and provides better performance in low modulation range. However, difficulty of selecting switching states increase at higher voltage levels [66]. SVM cannot also entirely eliminate the low order dominant harmonics from the output voltage of inverters.

1.3.3 Selective Harmonic Elimination PWM

In general, MLI generates quarter-wave symmetric staircase voltage waveform, synthesized by several DC voltages [77]. The generalized Fourier expression of the output voltage V_0 is given by

$$V_0 = \sum_{n=1,3,5\ldots}^{\infty} b_n \sin(n\omega t) + a_n \cos(n\omega t) \quad (1.2)$$

where b_n is the magnitude of nth harmonic component and ω is the fundamental switching frequency. Due to half and quarter wave symmetry of the output voltage, $a_n = 0$. The expression of b_n can be written as

$$b_n = \begin{cases} \frac{4V_{DC}}{n\pi}[cos(n\theta_1) + cos(n\theta_2) + \cdots\cdots + cos(n\theta_n)] & \text{for odd} \\ 0 & \text{for even} \end{cases} \quad (1.3)$$

$$0 \leq \theta_1 \leq \theta_2 \leq \theta_3 \cdots \theta_n < \frac{\pi}{2} \quad (1.4)$$

A 7-level staircase output voltage waveform using SHE-PWM is shown in Fig. 1.14. The set of non-linear transcendental equations for the output voltage waveform of a three-phase, 7-level MLI are

$$\begin{cases} m_a = \frac{1}{3}(cos(\theta_1) + cos(\theta_2) + cos(\theta_3) + cos(\theta_4) + cos\,\theta_5)) \\ 0 = cos(5\theta_1) + cos(5\theta_2) + cos(5\theta_3) + cos(5\theta_4) + cos(5\theta_5) \\ 0 = cos(7\theta_1) + cos(7\theta_2) + cos(7\theta_3) + cos(7\theta_4) + cos(7\theta_5) \end{cases} \quad (1.5)$$

where m_a is the modulation index and is defined as

$$m_a = \frac{V_{\text{desired}}}{4S\left(\frac{V_{DC}}{\pi}\right)} \quad (1.6)$$

where V_{desired} is the desired fundamental component of the output voltage and S is the number of separate DC sources.

In general, the most significant low frequency harmonics (5^{th} and 7^{th}) are eliminated by properly selecting the switching angles and high frequency harmonics are eliminated by using additional filters. The step angles of the MLI can be optimized to cancel some of the specified harmonics in SHE-PWM. The major complexity associated with SHE-PWM is that to solve nonlinear transcendental equations. Newton-Raphson theory or mathematical resultant theory are used to solve these transcendental equations [78]-[81].

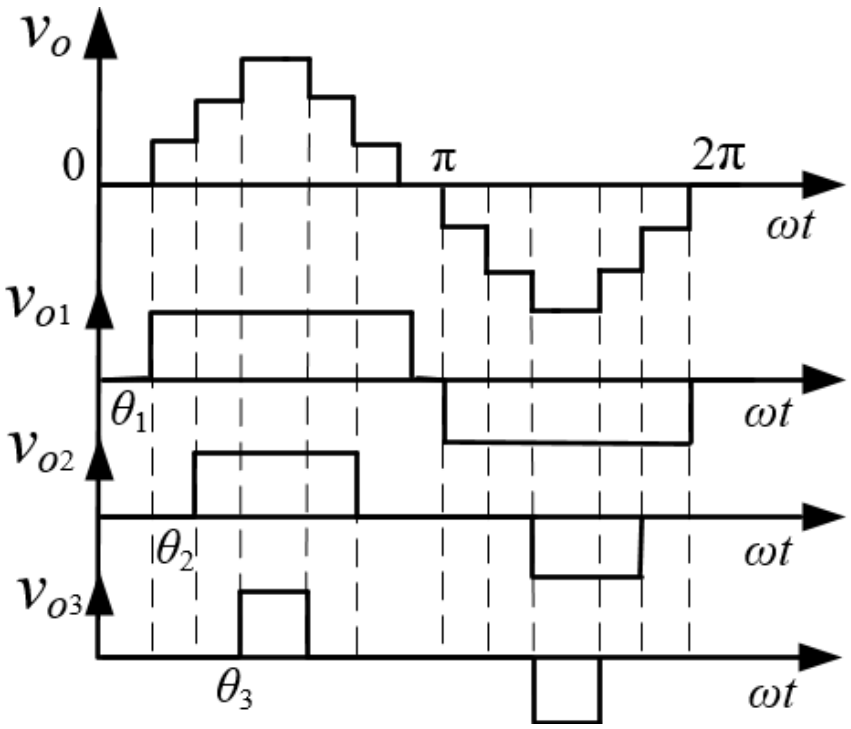


Fig. 1.14 Staircase output voltage waveform in SHE-PWM.

However, the degrees of the polynomials in those transcendental equations increase with the increase switching angles and it becomes difficult to solve them.

1.4 Meta-Heuristic Optimization Algorithms

Meta-heuristic optimization techniques become extremely popular over past a few decades for solving the aforementioned problems because they are simple, flexible, derivation free and local minima avoided [82]-[98]. These techniques are inspired by animals' behaviour and evolutionary concepts. Meta-heuristic algorithms are grouped in two main categories, evolution-based and swarm-based algorithms. Evolution-based methods are stimulated by the laws of natural evolution. Some evolution and swarm inspired optimization algorithms such as genetic algorithm (GA), particle swarm optimization (PSO), ant colony optimization (ACO), grey wolf optimization (GWO) and wolf optimization (WO) are discussed in the following sub-sections [84]-[98].

1.4.1 Genetic Algorithm

GA is an evolution-based method inspired by the process of natural selection and is widely used for finding near optimal solutions [84]-[88]. The process of evolution of species in GA is mimicked by biologically inspired mechanisms e.g. selection, crossover and mutation. The GA is derivative free and can be used for both discrete and continuous optimization. However, GA can be time consuming for large and complex problems due to its repeated fitness function evaluation. The slow, untimely convergence rate and weak local search capability are the limitations of GA. The flow chart of GA is shown in Fig. 1.15.

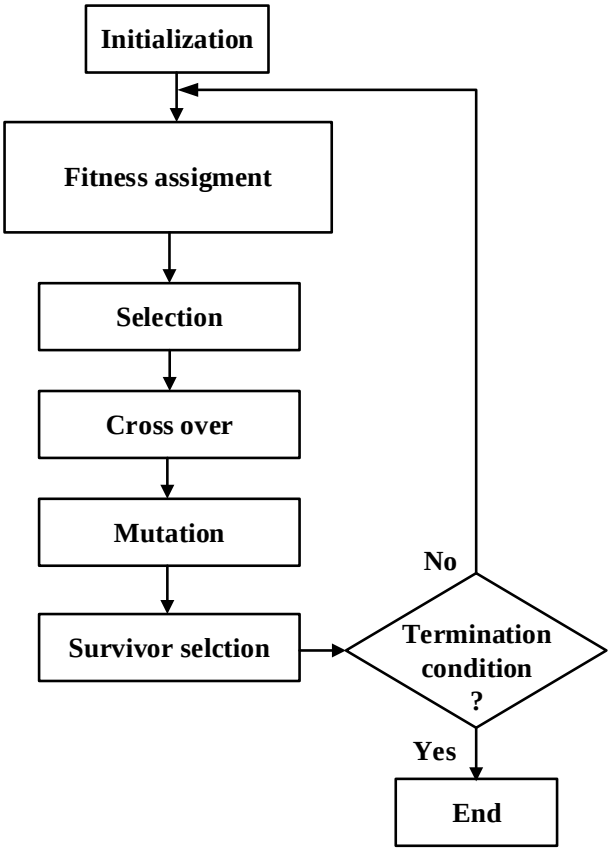


Fig. 1.15 Flow chart of GA [88].

1.4.2 Particle Swarm Optimization

PSO algorithm is inspired by social behaviour organisms such as birds or fish [89]-[94]. This method searches the optimal solution through agents, referred as particles. Every particle is

influenced by its own best position (*pbest*) and the group best position (*gbest*). The basic diagram of PSO is depicted in Fig. 1.16. PSO algorithm does not possesses any evolutionary variables such as crossover and mutation, which improves its convergence rate and local search ability. It also requires short computational time and can be used precisely to solve optimization problems. However, the primary drawback of PSO is that it cannot modify its velocity step size for fine tuning in local search, which results in premature convergence and stagnation in local optima. Also, it is difficult to define initial design parameters accurately in PSO.

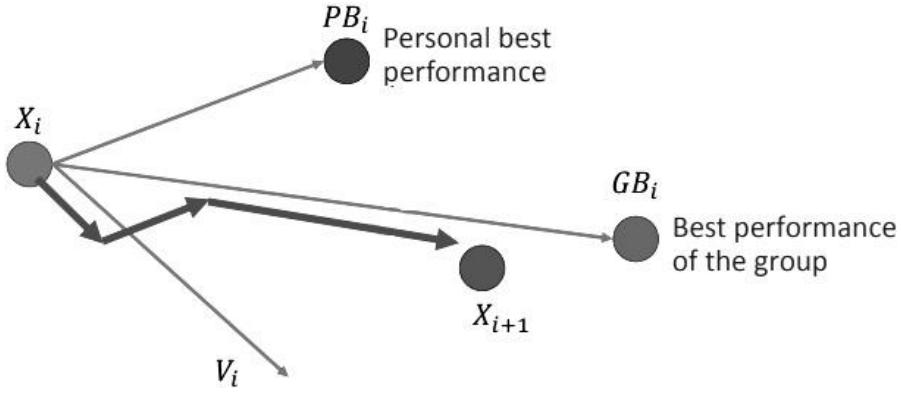


Fig. 1.16 Basic diagram of PSO [89].

1.4.3 Ant Colony Optimization

ACO algorithm is inspired by the social behaviour of ants [94]. The social intelligence of ants used for searching the closest path from the nest to the source of food, is the key inspiration ACO algorithm. A pheromone matrix is evolved over the course of iteration for finding the optimal solution in ACO algorithm. The artificial ants locate optimal solutions by moving through a parameter space, which represents all possible solutions. In ACO, ants lay down pheromones, directing each other towards the resources while exploring their environment. The simulated ants record their positions, so that in later simulation iterations more ants locate better solutions. The ACO can adapt to changes such as new distances and

guarantees the convergence probability in each iteration. However, ACO needs a difficult theoretical analysis and requires more experimentation than theoretical analysis to reach global optima. It also suffers from uncertainty in convergence rate. The flow chart of ACO is shown in Fig. 1.17.

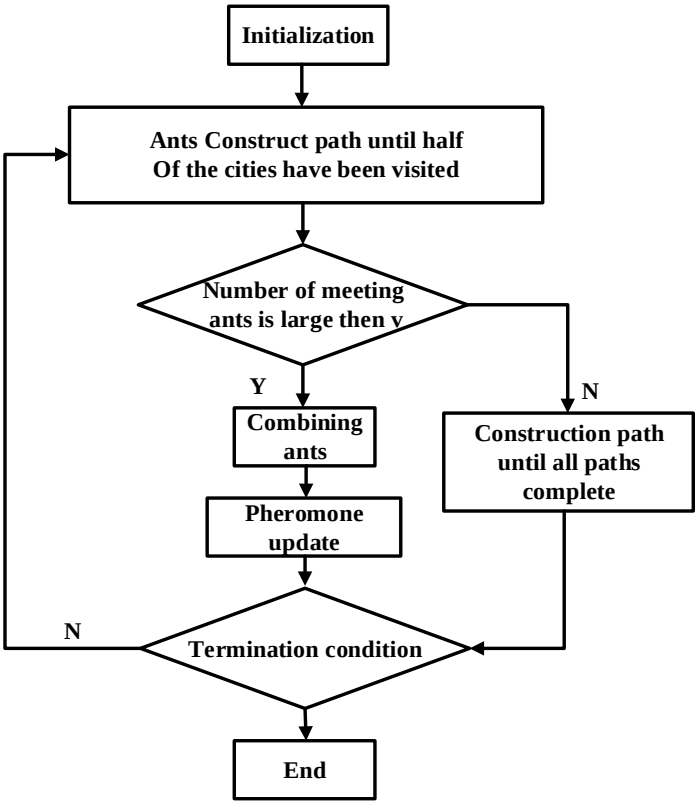


Fig. 1.17 Flow chart of ACO [85].

1.4.5 Whale Optimization

WO algorithm is swarm based meta-heuristic optimization method, which mimics the social behaviour of humpback whales. The humpback whales use a special hunting method, known as bubble-net hunting [95], [96]. Humpback whales prefer to hunt small fishes close to the surface. Hunting mechanism is done by creating bubbles along a spiral path as shown in Fig. 1.18. The humpback whales find two movements named as upward-spirals and double loops in their search mechanism. The location update in WO algorithm is divided into three phase

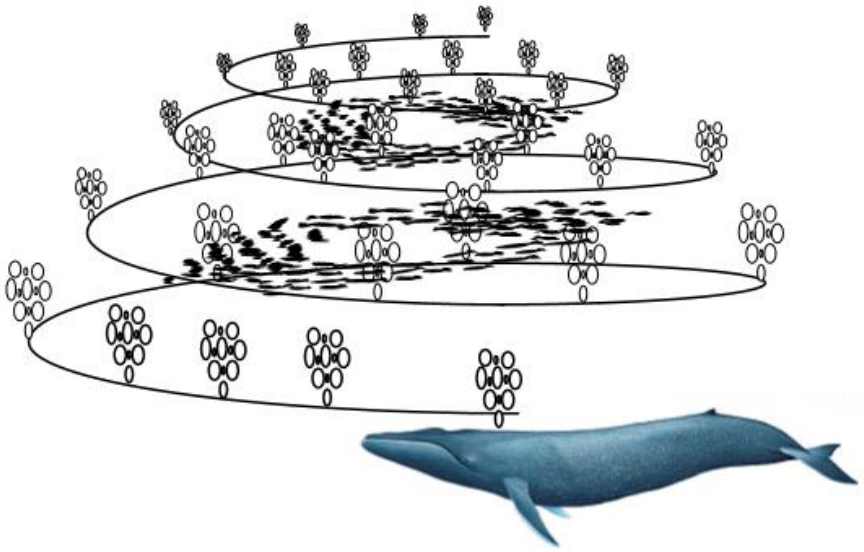


Fig. 1.18 Movement of whale [95].

such as encircling prey, spiral bubble-net feeding movement and search for prey. During the exploitation process, humpback whales adjust their positions toward the global optima using two mechanisms which are encircling the prey and spiral bubble-net feeding movement. The exploration phase deals with search for prey.

WO algorithm is simple, flexible, easy to programmed and maintains good balance between exploitation and exploration. Also, it has very few algorithm parameters. In WO, the position of the optimal design in the search space is not known earlier. This procedure of update of WO may bring about getting caught in local optima.

1.4.4 Grey Wolf Optimization

GWO algorithm is a swarm intelligent technique, which mimics the leadership hierarchy of grey wolves [97], [98]. Grey wolf belongs to canidae family and mostly prefer to live in groups. They have a strict social dominant hierarchy; the leader is a male or female, called alpha (α). The α is generally responsible for decision making. The beta (β) wolves are subordinate wolves, which help the α wolves in decision making. The β is an advisor to α

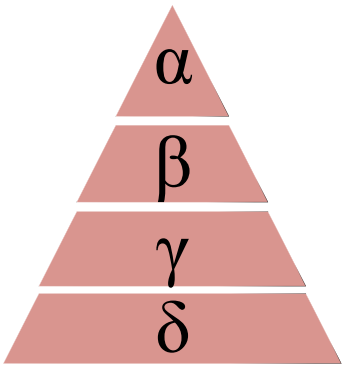


Fig. 1.19 Hierarchy diagram of GWO [97].

and maintains the discipline of the entire pack. The lower ranking grey wolf is omega (ω), which has to pass the information to all other dominant wolves. The wolves which do not fall in α, β and ω are called delta (δ). The δ wolves dominate ω and reports to α and β. The social hierarchy of wolves in GWO algorithm is shown in Fig. 1.19. The GWO algorithm has superior exploration and exploitation characteristics than other swarm intelligence techniques. Further, the GWO has been successfully applied for solving various engineering optimization problems. GWO requires only few parameters and is easy to implement, which makes it superior than earlier discussed evolutionary algorithms. However, GWO simulates internal leadership hierarchy of wolves, thus, in the searching process, the position of best solution is evaluated by using three solutions (three different wolves) instead of a single solution, which decreases the probability of premature convergence and falling into the local optima.

1.5 Objectives of Thesis

It is evident from the literature study that there is scope of further improvement with regard to MLIs in terms of harmonic content in the output voltage, number active/passive components used, PIV and TSV of devices and the cost involved in MLI configurations. The following points have been identified as the main objectives of the thesis.

- Applying optimization techniques in HC-MLI for harmonic minimization and faster convergence.
- Selecting a PWM technique for harmonic optimized HC-MLIs.
- Capacitor voltage balancing in HC-MLIs, specially at higher modulation indices using modified optimization techniques.
- Proposing SC-MLIs for active and passive components reduction and reduced TSV and PIV of devices used.

1.6 Conclusion

In this chapter, different MLI topologies such as NPC-MLI, FC-MLI, CHB-MLI, HC-MLI and SC-MLIs with their relative advantages and disadvantages are discussed in detail. For controlling the output voltage of MLIs different types of PWM schemes such as SPWM, SVM and SHE-PWM have been proposed in the literature over the years. The salient features of these PWM schemes has been critically examined and it has been found that as the number of harmonics to be eliminated increases, the degrees of the polynomials in the transcendental equations become so large that solving them becomes very difficult. This problem can be solved by meta-heuristic optimization methods such as GA, PSO, ACO, WOA, GWO, etc. Out of the different optimization methods reported in the literature PSO, WOA and GWO has been selected for further investigation in this thesis. With modifications in the algorithm of these optimization methods and subsequently applying to HC-MLI, it has been found that the performance these optimization methods can be improved in terms of convergence speed and harmonic minimization.

The balancing of capacitor voltage is an inherent challenge in HC-MLI. Several schemes have been reported for capacitor voltage balance in HC-MLIs. However, these schemes make the overall control technique complicated. The control schemes become even more complex with the increase in voltage levels, which makes the overall system expensive and bulky.

Advanced MLI topologies like SC-MLIs have emerged in recent years as a promising technology to counter these problems. In SC-MLIs, capacitor voltage is balanced inherently without using extra control circuit. However, in SC-MLIs, the number of circuit components increases with higher number of output voltage levels. Further, TSV and PIV also increase rapidly with the increase in voltage levels. In this work, two new configurations of SC-MLI, named as diode assisted switched-capacitor MLI (DASC-MLI) and reduced voltage stress switched-capacitor MLI (RVSC-MLI) have been proposed, which can generate up to 17-level output voltages using lesser number circuit components as compared to other existing SC-MLIs. The proposed SC-MLIs can generate even higher output voltage levels with lesser number of DC sources and passive components as compared to the existing SC-MLIs. The PIV of the power switches reduce in the proposed SC-MLIs in comparison to existing topologies, leading to reduction in cost of the proposed SC-MLIs.

1.7 Organization of Thesis

Apart from this chapter, the thesis consists of six more chapters. The brief description of the remaining chapters is outlined as follows:

Chapter 2 presents modified particle swarm optimization (MPSO) method for harmonic minimization in three-phase, HC-MLI using SHE-PWM. Simulation and experimentation have been carried out to exhibit the merits MPSO optimized HC-MLI as compared to GA and PSO optimized HC-MLI.

Chapter 3 represents modified whale optimization (MWO) for selective harmonic elimination in three-phase, HC-MLI so as to eliminate the lower order harmonics from the output voltage. A comparison is made among GA, PSO, WO and MWO optimized HC-MLIs through simulation and experimental studies.

Chapter 4 represents a modified grey wolf optimization (MGWO) technique through SHE-PWM for harmonic reduction in three-phase, HC-MLI. The performance of the proposed MGWO is validated through simulation and experimentation. The results obtained show that MGWO algorithm is more efficient and accurate than other reported algorithms such as GA, PSO and GWO in terms of performance, harmonic reduction and convergence rate.

Chapter 5 represents a new diode assisted switched-capacitor MLI (DASC-MLI). The proposed DASC-MLI is compared with other existing SC-MLIs to exhibits its advantages in terms of circuit components, voltage gain, TSV and cost.

Chapter 6 represents a new reduced voltage stress switched-capacitor MLI (RVSC-MLI). The proposed RVSC-MLI is compared with other existing SC-MLIs to exhibits its merits in terms of circuit components, PIV and TSV.

Chapter 7 delineates the overall conclusion of the thesis and discusses the scope of future work in this field.