Chapter 6

Conclusion and Future Scope

6.1 Introduction

The basic objective of the present thesis is to develop some theoretical models for the subthreshold characteristics of DG-JLFETs with channel profile engineering as well as dielectric pocket (DP) engineering. In this regard, we have developed analytical models for the channel potential, the threshold voltage, subthreshold current and subthreshold swing (SS) of the DG-JLFETs with a vertical Gaussian-like channel doping profile and DG-JLFETs with dielectric pockets (DPs) at the source and drain sides. This chapter has been devoted to summarize and conclude the major works carried out in this thesis as described in the following.

6.1 Chapter-Wise Summary and Conclusions

Chapter 1 briefly introduces various short-channel effects (SCEs) due to scaling on the progress and development of MOSFET technology. Different techniques to mitigate/optimize the SCEs have also been discussed in this chapter. Various multiple-gate non-classical MOS structures have been introduced to sustain MOSFET scaling for future generation IC technology. It has been discussed that the DG-JLFETs have tremendous potential for scaling of MOS transistors even below sub-10 nm technology nodes with reasonable SCEs. The general review of some important state-of-the-art literatures related to the JLFETs shows that there are ample opportunities for theoretical

investigations of the subthreshold characteristics of DG-JLFETs with non-uniform channel doping engineering as well as dielectric pocket engineering. Based on the literature survey, the scopes of the present thesis have been outlined in the last section of this chapter.

Chapter 2 presents the analytical modeling and simulation of the channel potential and threshold voltage of DG-JLFETs with a vertical Gaussian-like doping profile in the channel region. The analytical solution of Poisson's equation has been solved by using the superposition method (evanescent mode analysis) to obtain the potential distribution function in the channel. The 2D channel potential has been assumed to be the summation of the potential function of the conventional long-channel device obtained by solving 1D Poisson equation and 2D potential function obtained by solving the 2D Laplace equation. The position of the conduction path has also been modeled to calculate the potential at different positions of the conduction path. The channel potential at the effective conduction path has been used to model the threshold voltage of the device. The proposed model results have been validated by comparing them with the simulation data obtained by using the commercially available ATLAS^{TM} device simulation software from the Silvaco International. The major observations can be given as follows:

- Unlike the conventional MOSFETs, the threshold voltage of the DG-JLFETs is decreased with increase in the peak doping concentration of the Gaussian-like function.

- The threshold voltage can be increased by reducing the value of the straggle parameter of the DG-JLFETs.

- The threshold voltage is increased with the decrease in t_{si} as well as in t_{ox} due to the increased gate control over the channel of the device.

- For DG-JLFETs with gate lengths below ~60 nm, the source–channel potential barrier as well as threshold voltage is observed to be decreased with the decrease in the channel length and peak doping concentration of the Gaussian profile and with the increase in the drain–source voltage, silicon channel thickness, gate-oxide thickness and straggle parameter of the Gaussian profile in the channel.

- The straggle parameter of the channel profile can be used as an extra parameter in addition to the peak doping concentration and projected range of the channel profile for the optimization of the threshold voltage, DIBL and SCEs in the device.

- The model results are well matched with the simulation data obtained by using the commercially available ATLAS^{TM} 2D device simulator.

The study shows that, besides the conventional device parameters of the DG-MOSFETs with a uniform channel doping, the projected range and straggle parameter of the Gaussian channel doping profile can serve as two additional parameters for optimizing

the channel potential distribution and threshold voltage characteristics of the DG-JLFETs.

Chapter 3 includes the analytical modeling and simulation of the subthreshold current and SS characteristics of DG-JLFETs considered in Chapter 2 with a vertical Gaussian-like doping profile in the channel region**.** The minimum channel potential model proposed in Chapter 2 has been utilized for developing the present subthreshold current model. The SS model has been developed by using the concept of the effective conduction path parameter. The major observations of Chapter 3 are given in the following.

- The subthreshold leakage current is increased with the decreased channel length, increased straggle parameter, increased oxide thickness and increased peak channel concentration of the Gaussian profile.
- SS is deteriorated very rapidly with the increased channel thickness and gate oxide thickness for channel lengths below 60 nm.
- The subthreshold current and SS of the Gaussian doped DG-JLFETs can be optimized by the proper choice of the gate oxide thickness, channel thickness, peak concentration and straggle parameter.
- A good agreement of the model results with the ATLAS TCAD simulation data confirms the validity of the proposed model.

Clearly, the parameters of the Gaussian doping profile can provide better flexibility in optimizing the subthreshold current and SS characteristics of the DG-JLFETs.

Chapter 4 presents the analytical modeling of the channel potential and the threshold voltage of the DG-JLFETs with dielectric pockets (DPs) at the source and drain sides. The channel potential function and threshold voltage of the DP-DG-JLFETs have been modelled in the similar manner as discussed in **Chapter 2**. The effects of source and drain depletion regions have been included for improving the accuracy of the model. The effects of the DP thickness and DP length on the SCEs of the DP-DG-JLFETs have been investigated in this chapter. The major observations of **Chapter 4** are as follows:

- The channel potential and threshold voltage of the DP-DG-JLFETs are dependent on the DP length and DP thickness.
- The degradation in threshold voltage and DIBL due to the SCEs can be improved by increasing DP length and DP thickness in the structure.
- The close matching of the model results with the ATLAS-based 2D device simulation data confirms the validity of our proposed model.

Clearly, the length and thickness of the DP in the proposed device structure can be used as two additional parameters for optimization of the threshold voltage characteristics of the DP-DG-JLFETs considered in this chapter.

Chapter 5 presents the analytical modeling of the subthreshold current and SS of the DP-DG-JLFETs following the similar method used in the **Chapter 4**. The main results of chapter-5 can be written as follows:

- The subthreshold current is decreased with the increase in the DP length and DP thickness.

- For a fixed value of DP length and DP thickness, the subthreshold current is increased with the decreased channel length, increased gate oxide thickness, increased channel thickness and increased channel doping concentration.

- SS can be improved by increasing the DP length and DP thickness. However, SS becomes nearly constant for the DP thickness beyond ~5 nm, possibly due to the complete suppression of lateral electric field in the channel.
- A reasonable agreement between the model results and ATLAS^{TM} TCAD simulation data has confirmed the validity of the proposed model.

The study demonstrates that the DP length and DP thickness can be used as two additional parameters for optimizing subthreshold current and SS of the DP-DG-JLFETs considered in this thesis.

6.3 Future Scopes of Work

We know that research is a never ending process and no thesis is complete in every respect. The works carried out in this thesis may lead to some future scopes of research in the related areas as given below:

- A continuous drain current model valid in all regimes of the device operation for short-channel DG-JLFETs with vertical Gaussian doping profile in the channel of the device can be worked out.

- A capacitance model for short-channel DG-JLFETs with vertical Gaussian channel profile in the channel may be useful.

- A continuous drain current model valid in all regimes of the device operation for short-channel DP-DG-JLFETs can be worked out.

- The RF and analog study of DP-DG-JLFETs will be useful to understand the circuit behavior of the device.

- The modeling presented in this thesis for DG-JLFET may be the good foundation to develop model for junctionless FinFETs, junctionless Tri-gate and Gate All around (GAA) JLFETs devices.