References

J. E. Lilienfeld, “Method and apparatus for controlling electric currents,” *US Patent 1,745,175*. pp. 1–4, 1930.

O. Heil, “British Patent 439, 457.” 1935.

D. Kahng, “U. S. Patent No.,” *4988386*, 1960.

M. Riordan, L. Hoddeson, and C. Herring, “The invention of the transistor,” vol. 99, no. 2, pp. S336–S345, 1999.

Gordon E. Moore, “Cramming more components onto integrated circuits,” *Electronics*, Vol. 38, No.8. April 19, 1965.

C. Mead, “Fundamental limitations in microelectronics – I. MOS technology,” Solid State Electronics, vol. 15, pp. 819–829, 1972.

R. H. Dennard, F. H. Gaensslen, H-N, Yu, V.I. Rideout, E. Bassous, and A. R. LeBlanc, “Design of ion-implanted MOSFET’s with very small physical dimensions,” IEEE Journal of Solid-State Circuits, SC-9, pp.256–268, 1974.

G. E. Moore, “Progress in Digital Integrated Electronics,” Technical Digest 1975, IEEE International Electron Devices Meeting, pp. 11-13, 1975.

S. Borkar, “Design challenges of technology scaling,” *IEEE MICRO*, vol. 19, no. 4, pp. 23–29, 1999.

B. Davari, R. H. Dennard, and G. G. Shahidi, “CMOS scaling for high performance and low power-the next ten years,” *Proc. IEEE*, vol. 83, no. 4, pp. 595–606, 1995.

I. Ferain, C. a. Colinge, and J.-P. Colinge, “Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors,” *Nature*, vol. 479, no. 7373, pp. 310–316, 2011.

ITRS, “International Technology Roadmap for Semiconductors,” *Int. Technol. roadmap Semicond.*, 2011.

T. Standaert, G. Beique, H. C. Chen, S. T. Chen, B. Hamieh, J. Lee, P. McLaughlin, J. McMahon, Y. Mignot, F. Mont, K. Motoyama, S. Nguyen, R. Patlolla, B. Peethala, D. Priyadarshini, M. Rizzolo, N. Saulnier, H. Shobha, S. Siddiqui, T.

Spooner, H. Tang, O. Van Der Straten, E. Verduijn, Y. Xu, X. Zhang, J. Arnold, D. Canaperi, M. Colburn, D. Edelstein, V. Paruchuri, and G. Bonilla, "BEOL process integration for the 7 nm technology node," *2016 IEEE Int. Interconnect Technol. Conf. / Adv. Met. Conf. IITC/AMC 2016*, pp. 2–4, 2016.

Q. Xie, X. Lin, Y. Wang, S. Chen, M. J. Dousti, and M. Pedram, "Performance Comparisons Between 7-nm FinFET and Conventional Bulk CMOS Standard Cell Libraries," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 62, no. 8, pp. 761–765, 2015.

D. L. Critchlow, MOSFET Scaling: the Driver of VLSI Technology, Proceedings of the IEEE, 87, 659-667, 1999.

T. Sekigawa and Y. Hayashi, "Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate," *Solid State Electron.*, vol. 27, no. 8–9, pp. 827–828, 1984.

G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized Scaling Theory and Its Application," *IEEE Trans. Electron Devices*, vol. 41, no. 4, pp. 1283–1290, 1984.

Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, vol. 25, no. 11. 1998.

H.-S. P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wann, and J. J. Welser, "Nanoscale CMOS," *Proc. IEEE*, vol. 87, no. 4, pp. 537–570, 1999.

Mark S. Lundstrom, "Moore ' s Law Forever ?," *Science (80-.).*, vol. 299, no. 5604, pp. 210–211, 2003.

R. W. Keyes, "Physical limits in digital electronics," *Proc. IEEE*, vol. 63, no. 5, pp. 740–767, 1975.

S. Borkar, "Design challenges of technology scaling," *IEEE MICRO*, vol. 19, no. 4, pp. 23–29, 1999.

B. Davari, R. H. Dennard, and G. G. Shahidi, "CMOS scaling for high performance and low power-the next ten years," *Proc. IEEE*, vol. 83, no. 4, pp. 595–606, 1995.

J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions.," *Nat. Nanotechnol.*, vol. 5, no.

February, pp. 225–229, 2010a.

R. R. Troutman, “VLSI Limitations from Drain-Induced Barrier Lowering,” *IEEE J. Solid-State Circuits*, vol. 14, no. 2, pp. 461–469, 1979.

B. G. Streetman and S. K. Banerjee, “Solid State Electronic Devices,” *PHI Learn. Priv. Limited,New Delhi-110020.*, p. 321, 2009.

N. Arora, “MOSFET Modeling for VLSI Simulation Theory and Practice,” *World Sci. Publ. Co. Re. Ltd*, pp. 243–251, 2007.

Y.-B. Kim, “Challenges for Nanoscale MOSFETs and Emerging Nanoelectronics,” *Trans. Electr. Electron. Mater.*, vol. 11, no. 3, pp. 93–105, 2010.

R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, “High- /Metal–Gate Stack and Its MOSFET Characteristics,” *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 408–410, 2004.

E. P. Gusev, V. Narayanan, and M. M. Frank, “Advanced high-K dielectric stacks with polySi and metal gates: Recent progress and current challenges,” *IBM J. Res. Dev.*, vol. 50, no. 4.5, pp. 387–410, 2006.

B. J. SEALY, “Review of III-V semiconductor materials and,” *J. Inst. Electron. Radio Eng.*, vol. 57, no. 1, pp. S2–S12, 1987.

S. Oktyabrsky and P. D. Ye, “Fundamentals of III-V Semiconductor MOSFETs,” *Springer New York Dordr. Heidelb. London*, 2010.

O. Ueda, “A Review of Materials Issues and Degradation of III-V Compound Semiconductors and Optical Devices,” *ECS Trans.*, vol. 33, no. 13, pp. 73–92, 2010.

M. Passlack, P. Zurcher, K. Rajagopalan, R. Droopad, J. Abrokwah, M. Tutt, Y. Park, E. Johnson, A. Zlotnicka, P. Fejes, R. J. W. Hill, D. A. J. Moran, X. Li, H. Zhou, D. Macintyre, S. Thoms, A. Asenov, K. Kalna, and I. G. Thayne, “High Mobility Ill-V MOSFETs,” in *IEDM Tech. Dig*, 2007, pp. 1–4.

Y. Xuan, Y. Q. Wu, and P. D. Ye, “High-performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm,” *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 294–296, 2008.

S. Takagi, “Strained-Si CMOS Technology,” *Springer, 2007*, 2007.

K. Rim, R. Anderson, D. Boyd, F. Cardone, K. Chan, H. Chen, S. Christansen, J. Chu, K. Jenkins, T. Kanarsky, S. Koester, B. H. Lee, K. Lee, V. Mazzeo, A. Mocuta, D. Mocuta, P. M. Mooney, P. Oldiges, J. Ott, P. Ronsheim, R. Roy, A. Steegen, M. Yang, H. Zhu, M. Ieong, and H. S. P. Wong, "Strained Si CMOS (SS CMOS) technology: Opportunities and challenges," *Solid. State. Electron.*, vol. 47, no. 7 SPEC., pp. 1133–1139, 2003.

F. M. Bufler and W. Fichtner, "Hole and electron transport in strained Si: Orthorhombic versus biaxial tensile strain," *Appl. Phys. Lett.*, vol. 81, no. 1, pp. 82–84, 2002.

S. E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C. H. Jan, C. Kenyon, J. Klaus, K. Kuhn, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, P. Nguyen, S. Sivakumar, R. Shaheed, L. Shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. El-Mansy, "A 90-nm logic technology featuring strained-silicon," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1790–1797, 2004.

S. E. Thompson, S. Member, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-Process-Induced Strained-Si : Extending the CMOS Roadmap," vol. 53, no. 5, pp. 1010–1020, 2006.

S. Ogura, P. J. Tsang, W. W. Walker, D. L. Critchlow, and J. F. Shepard, "Design and Characteristics of the Lightly Doped Drain-Source (LDD) Insulated Gate Fieldeffect Transistor," *IEEE J. Solid-State Circuits*, vol. 15, no. 4, pp. 424–432, 1980.

A. Kumar, E. Kalra, S. Haldar, and R. S. Gupta, "1/f noise model of fully overlapped lightly doped drain MOSFET," *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1426–1430, 2000.

F.-C.Hsu and K.-Y.Chiu, "Evaluation of LDD'MOSFET's Based on ectron-Induced Degradation," *Electron, Ieee Lett. Device*, vol. 2, no. 5, pp. 162–165, 1984.

C. H. Shih, Y. M. Chen, and C. Lien, "An Insulated Shallow Extension Structure for Bulk MOSFET," *IEEE Trans. Electron Devices*, vol. 50, no. 11, pp. 2294–2297, 2003.

H. H. H. Hwang, D.-H. L. D.-H. Lee, and J. M. H. J. M. Hwang, "Degradation of

MOSFETs drive current due to halo ion implantation," in *International Electron Devices Meeting. Technical Digest*, 1996, pp. 567–570.

M. Jurczak, T. Skotnicki, R. Gwoziecki, M. Paoli, B. Tormen, P. Ribot, D. Dutartre, S. Monfray, and J. Galvier, "Dielectric pockets-a new concept of the junctions fordeca-nanometric CMOS devices," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1770–1774, 2001.

O. P. Kok and K. Ibrahim, "Simulation of two-dimensional 50 nm vertical metal oxide semiconductor field-effect transistor incorporating a dielectric pocket," *Jpn. J. Appl. Phys.*, vol. 48, pp. 111201–111205, 2009.

C. H. Shih, Y. M. Chen, and C. Lien, "An analytical model of short-channel effect for metal-oxide-semiconductor field-effect transistor with insulated shallow extension," *Japanese J. Appl. Physics, Part 1 Regul. Pap. Short Notes Rev. Pap.*, vol. 43, no. 12, pp. 7993–7996, 2004.

S. K. Jayanarayanan, S. Dey, J. P. Donnelly, and S. K. Banerjee, "A novel 50 nm vertical MOSFET with a dielectric pocket," *Solid. State. Electron.*, vol. 50, pp. 897–900, 2006.

V. Kumari, M. Saxena, R. S. Gupta, and M. Gupta, "Two-dimensional analytical drain current model for double-gate MOSFET incorporating dielectric pocket," *IEEE Trans. Electron Devices*, vol. 59, no. 10, pp. 2567–2574, 2012.

E. Gili, T. Uchino, M. M. Al Hakim, C. H. de Groot, O. Buiu, S. Hall, and P. Ashburn, "Shallow junctions on pillar sidewalls for sub-100-nm vertical MOSFETs," *IEEE Electron Device Lett.*, vol. 27, no. 8, pp. 692–695, 2006.

S. Tam, P.-K. Ko, and C. Hu, "Lucky-Electron Model of Channel Hot-Electron Injection in MOSFET's," *IEEE Trans. Electron Devices*, vol. 31, no. 9, pp. 1116–1125, 1984.

M. Shur, "Split-gate field-effect transistor," *Appl. Phys. Lett.*, vol. 54, no. 2, pp. 162–164, 1989.

X. Zhou and W. Long, "A novel hetero-material gate (HMG) MOSFET for deep-submicron ULSI technology," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2537–2545, 1998.

X. Zhou, “Exploring the novel characteristics of hetero-material gate field-effect transistors (HMGFET’s) with gate-material engineering,” *IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 113–120, 2000.

Xuejue Huang, Wen-Chin Lee, Charles Kuo, D. Hisamoto, Leland Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Yang-Kyu Choi, K. Asano, V. Subramanian, Tsu-Jae King, J. Bokor, and Chenming Hu, “Sub 50-nm FinFET: PMOS,” *Int. Electron Devices Meet. 1999. Tech. Dig. (Cat. No.99CH36318)*, pp. 67–70, 1999.

J. P. Colinge, “Multiple-gate SOI MOSFETs,” *Solid. State. Electron.*, vol. 48, pp. 897–905, 2004.

B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, “High performance fully-depleted tri-gate CMOS transistors,” *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 263–265, 2003.

J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, “Silicon-on-insulator ‘gate-all-around device,’” in *International Technical Digest on Electron Devices*, 1990, pp. 595–598.

J. T. Park, J. P. Colinge, and C. H. Diaz, “Pi-gate SOI MOSFET,” *IEEE Electron Device Lett.*, vol. 22, no. 8, pp. 405–406, 2001.

Fu-Liang Yang, Hao-Yu Chen, Fang-Cheng Chen, Cheng-Chuan Huang, Chang-Yun Chang, Hsien-Kuang Chiu, Chi-Chuang Lee, Chi-Chun Chen, Huan-Tsung Huang, Chih-Jian Chen, Hun-Jan Tao, Yee-Chia Yeo, Mong-Song Liang, and Chenming Hu, “25 nm CMOS Omega FETs,” *Dig. Int. Electron Devices Meet.*, vol. 0, no. 6, pp. 255–258, 2002.

K. Suzuki, Y. Kataoka, S. Nagayama, C. W. Magee, T. H. Büyüklimanli, and T. Nagayama, “Analytical model for redistribution profile of ion-implanted impurities during solid-phase epitaxy,” *IEEE Trans. Electron Devices*, vol. 54, no. 2, pp. 262–271, 2007.

G. Zhang, Z. Shao, and K. Zhou, “Threshold voltage model of short-channel FD-SOI MOSFETs with vertical Gaussian profile,” *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 803–809, 2008.

S. M. Sze, *Physics of Semiconductor Devices*, 2end Editi. Sons, John Wiley &, 1981.

P. Pandey, B. B. Pal, and S. Jit, “A New 2-D Model for the Potential Distribution and Threshold Voltage of Fully Depleted,” vol. 51, no. 2, pp. 246–254, 2004.

P. K. Tiwari and S. Jit, “Threshold Voltage Model for Symmetric Double-Gate (DG) MOSFETs With Non-Uniform Doping Profile,” *J. Electron Devices*, vol. 7, pp. 241–249, 2010.

A. Dasgupta and S. K. Lahiri, “An analytical threshold voltage model of short-channel MOSFET’s with implanted channels,” *Int. J. Electron.*, vol. 34, no. 5, pp. 655–669, 1987.

A. Dasgupta and S. Lahiri, “A two-dimensional analytical model of threshold voltages of short-channel MOSFETs with Gaussian-doped channels,” *Electron Devices, IEEE Trans.*, vol. 35, no. 3, pp. 390–392, 1988.

J. P. Colinge, A. Kranti, R. Yan, C. W. Lee, I. Ferain, R. Yu, N. D. Akhavan, and P. Razavi, “Solid-State Electronics Junctionless Nanowire Transistor (JNT): Properties and design guidelines,” *Solid. State. Electron.*, vol. 65–66, pp. 33–37, 2011.

H.-S. P. Wong, “Beyond the Conventional MOSFET,” in 31st European Solid-State Device Research Conference, 2001, pp. 20–22.

D. J. Frank, S. E. Laux, and M. V. Fischetti, “Monte Carlo Simulation of a 30,” in *International Electron Devices Meeting, (IEDM) Technical Digest.*, 1992, pp. 553–556.

C. Fiegna, H. Iwai, T. Saito, E. Sangiorgi, and B. Riccb, “D e. e,” in *VLSI Technology, Digest of Technical Papers*, 1993, pp. 33–34.

C. W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J. P. Colinge, “Performance estimation of junctionless multigate transistors,” *Solid. State. Electron.*, vol. 54, no. 2, pp. 97–103, 2009a.

C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, “Junctionless multigate field-effect transistor,” *Appl. Phys. Lett.*, vol. 94, no. 5, p. 53511, 2009b

J. P. Colinge, C. W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. N.

Nazarov, and R. T. Doria, “Reduced electric field in junctionless transistors,” *Appl. Phys. Lett.*, vol. 96, no. May 2014, pp. 94–97, 2010b.

J. P. Colinge, A. Kranti, R. Yan, C. W. Lee, I. Ferain, R. Yu, N. D. Akhavan, and P. Razavi, “Junctionless Nanowire Transistor (JNT): Properties and design guidelines,” *Solid. State. Electron.*, vol. 65–66, no. 1, pp. 33–37, 2011.

E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, “Theory of the junctionless nanowire FET,” *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 2903–2910, 2011.

E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, “Physical model of the junctionless UTB SOI-FET,” *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 941–948, 2012.

G. Leung and C. O. Chui, “Variability impact of random dopant fluctuation on nanoscale junctionless FinFETs,” *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 767–769, 2012.

Y. Taur, H. P. Chen, W. Wang, S. H. Lo, and C. Wann, “On-off charge-voltage characteristics and dopant number fluctuation effects in junctionless double-gate MOSFETs,” *IEEE Trans. Electron Devices*, vol. 59, no. 3, pp. 863–866, 2012.

A. Gnudi, S. Reggiani, E. Gnani, and G. Baccarani, “Analysis of threshold voltage variability due to random dopant fluctuations in junctionless FETs,” *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 336–338, 2012.

L. Ansari, B. Feldman, G. Fagas, J. P. Colinge, and J. C. Greer, “Simulation of junctionless Si nanowire transistors with 3 nm gate length,” *Appl. Phys. Lett.*, vol. 97, no. July, pp. 62105-1-62105–3, 2010.

R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. De Souza, C. W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. Kranti, and J. P. Colinge, “Junctionless multiple-gate transistors for analog applications,” *IEEE Trans. Electron Devices*,

vol. 58, no. 8, pp. 2511–2519, 2011.

P. Mondal, B. Ghosh, and P. Bal, “Planar junctionless transistor with non-uniform channel doping,” *Appl. Phys. Lett.*, vol. 102, no. May, pp. 3–6, 2013.

P. Mondal, B. Ghosh, P. Bal, M. W. Akram, and A. Salimath, “Effects of non-uniform doping on junctionless transistor,” *Appl. Phys. A*, pp. 2–7, 2015.

J. P. Duarte, S. Choi, D.-I. Moon, and Y. Choi, “Simple Analytical Bulk Current Model for Long-Channel Double-Gate Junctionless Transistors,” vol. 32, no. 6, pp. 704–706, 2011.

E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, “Physical model of the junctionless UTB SOI-FET,” *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 941–948, 2012.

Z. Chen, Y. Xiao, M. Tang, Y. Xiong, J. Huang, J. Li, X. Gu, and Y. Zhou, “Surface-potential-based drain current model for long-channel junctionless double-gate MOSFETs,” *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3292–3298, 2012.

C. Sahu, P. Swami, S. Sharma, and J. Singh, “Simplified drain current model for pinch-off double gate junctionless transistor,” *Electron. Lett.*, vol. 50, no. 2, pp. 116–118, 2014.

A. Cerdeira, M. Estrada, S. Member, D. Trevisoli, T. Doria, M. De Souza, and M. A. Pavanello, “Analytical model for potential in double-gate juntionless transistors,” in *Microelectronics Technology and Devices (SBMicro)*, 2013, no. 6, pp. 2–4.

X. Jin, X. Liu, M. Wu, R. Chuai, J. H. Lee, and J. H. Lee, “A unified analytical continuous current model applicable to accumulation mode (junctionless) and inversion mode MOSFETs with symmetric and asymmetric double-gate structures,” *Solid. State. Electron.*, vol. 79, pp. 206–209, 2013.

Y. Taur, X. Liang, W. Wang, and H. Lu, “A Continuous, Analytic Drain-Current Model

for DG MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 2, pp. 107–109, 2004.

J. M. Sallese, N. Chevillon, C. Lallement, B. Iñiguez, and F. Prégaldiny, "Charge-based modeling of junctionless double-gate field-effect transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2628–2637, 2011.

J. P. Duarte, S. J. Choi, and Y. K. Choi, "A full-range drain current model for double-gate junctionless transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4219–4225, 2011.

F. Lime, E. Santana, and B. Iñiguez, "A simple compact model for long-channel junctionless Double Gate MOSFETs," *Solid. State. Electron.*, vol. 80, pp. 28–32, 2013.

B. Hwang, J. Yang, S. Member, S. Lee, and A. F. Mode, "Explicit Analytical Current – Voltage Model for Double-Gate Junctionless Transistors," vol. 62, no. 1, pp. 171–177, 2015.

F. Jazaeri, L. Barbut, and J. M. Sallese, "Trans-capacitance modeling in junctionless symmetric double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4034–4040, 2013.

F. Jazaeri, L. Barbut, and J. M. Sallese, "Trans-capacitance modeling in junctionless gate-all-around nanowire FETs," *Solid. State. Electron.*, vol. 96, pp. 34–37, 2014.

T.-K. Chiang, "A Quasi-Two-Dimensional Threshold Voltage Model for Short-Channel Junctionless," vol. 59, no. 9, pp. 2284–2289, 2012.

X. Jin, X. Liu, M. Wu, R. Chuai, J.-H. Lee, and J.-H. Lee, "Modelling of the nanoscale channel length effect on the subthreshold characteristics of junctionless field-effect transistors with a symmetric double-gate structure," *J. Phys. D. Appl. Phys.*, vol. 45, p. 375102, 2012.

X. Jin, X. Liu, H. I. Kwon, J. H. Lee, and J. H. Lee, "A subthreshold current model for nanoscale short channel junctionless MOSFETs applicable to symmetric and asymmetric double-gate structure," *Solid. State. Electron.,* vol. 82, pp. 77–81, 2013.

Z. M. Lin, H. C. Lin, K. M. Liu, and T. Y. Huang, "Analytical model of subthreshold current and threshold voltage for fully depleted double-gated junctionless transistor," *Jpn. J. Appl. Phys.*, vol. 51, no. 2 PART 2, 2012.

T. Holtij, M. Schwarz, A. Kloes, and B. Iñíguez, "2D analytical potential modeling of junctionless DG MOSFETs in subthreshold region including proposal for calculating the threshold voltage," *2012 13th Int. Conf. Ultim. Integr. Silicon, ULIS 2012*, no. 5, pp. 81–84, 2012.

T. Holtij, M. Schwarz, A. Kloes, and B. Iñíguez, "Threshold voltage, and 2D potential modeling within short-channel junctionless DG MOSFETs in subthreshold region," *Solid. State. Electron.,* vol. 90, pp. 107–115, 2013.

ATLAS: 2-D Device Simulator Version 5.14.0.R, 2013, Silvaco Int., Santa Clara, CA, USA, 2013.

T. Holtij, M. Graef, A. Kloes, and B. Iñíguez, "Modeling and performance study of nanoscale double gate junctionless and inversion mode MOSFETs including carrier quantization effects," *Microelectronics J.*, pp. 1–6, 2014.

T. Holtij, M. Graef, F. M. Hain, A. Kloes, and B. Iniguez, "Compact model for short-channel junctionless accumulation mode double gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 288–299, 2014.

A. Gnudi, S. Reggiani, E. Gnani, and G. Baccarani, "Semianalytical model of the subthreshold current in short-channel junctionless symmetric double-gate field-effect transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 4, pp. 1342–1348, 2013.

V. Kumari, N. Modi, M. Saxena, and M. Gupta, “Modeling and simulation of Double Gate Junctionless Transistor considering fringing field effects,” *Solid. State. Electron.*, vol. 107, pp. 20–29, 2015.

C. Jiang, R. Liang, J. Wang, and J. Xu, “A two-dimensional analytical model for short channel junctionless double-gate MOSFETs,” *AIP Adv.*, vol. 5, no. 5, p. 57122, 2015.

J. H. Woo, J. M. Choi, and Y. K. Choi, “Analytical threshold voltage model of junctionless double-gate MOSFETs with localized charges,” *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2951–2955, 2013.

P. Wang, Y. Zhuang, C. Li, Y. Li, and Z. Jiang, “Subthreshold behavior models for nanoscale junctionless double-gate MOSFETs with dual-material gate stack,” *Jpn. J. Appl. Phys.*, vol. 53, no. 8, 2014.

V. Kumari, N. Modi, M. Saxena, and S. Member, “Theoretical Investigation of Dual Material Junctionless Double Gate Transistor for Analog and Digital Performance,” vol. 62, no. 7, pp. 2098–2105, 2015.

A. K. Agrawal, P. N. V. R. Koutilya, and M. Jagadesh Kumar, “A pseudo 2-D surface potential model of a dual material double gate junctionless field effect transistor,” *J. Comput. Electron.*, vol. 14, no. 3, pp. 686–693, 2015.

A. Dey, A. Chakravorty, N. DasGupta, and A. DasGupta, “Analytical model of subthreshold current and slope for asymmetric 4-T and 3-T double-gate MOSFETs,” *IEEE Trans. Electron Devices*, vol. 55, no. 12, pp. 3442–3449, 2008.

R. S. Irving, *Integers, Polynomials, and Rings*, vol. 0. 2004.

W. H. Press, S. a Teukolsky, W. T. Vetterling, and B. P. Flannery, *Numerical Recipes in C: The Art of Scientific Computing*. 1997.

S. J. Choi, D. Il Moon, S. Kim, J. P. Duarte, and Y. K. Choi, “Sensitivity of threshold

voltage to nanowire width variation in junctionless transistors," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 125–127, 2011.

D.-Y. Jeon, S. J. Park, M. Mouis, M. Berthomé, S. Barraud, G.-T. Kim, and G. Ghibaudo, "Revisited parameter extraction methodology for electrical characterization of junctionless transistors," *Solid. State. Electron.*, vol. 90, pp. 86–93, 2013.

J. Lee and H. Shin, "Evanescent-Mode Analysis of Short-Channel Effects in MOSFETs," vol. 44, no. 1, pp. 50–55, 2004.

D. Monroe and J. M. Hergenrother, "Evanescent-mode analysis of short-channel effects in fully depleted SOI and related MOSFETs," in *1998 IEEE International SOI Conference Proceedings (Cat No.98CH36199)*, 1998, vol. 2, pp. 157–158.

J. M. H. Oh, Sang-Hyun, Don Monroe, "Analytic Description of Short-Channel Effects Surrounding-Gate MOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 445–447, 2000.