AUTHOR'S RELEVANT PUBLICATIONS

Journals:

[1] Balraj Singh, D. Gola, K. Singh, E. Goel, S. Kumar and S. Jit "Analytical Modeling of Channel Potential and Threshold Voltage of Double-Gate Junctionless FETs With a Vertical Gaussian-Like Doping Profile," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2299–2305, 2016.

[2] Balraj Singh, D. Gola, K. Singh, E. Goel, S. Kumar, and S. Jit, "Analytical modeling of subthreshold characteristics of ion-implanted symmetric double gate junctionless field effect transistors," *Mater. Sci. Semicond. Process.*, vol. 58, no. October 2016, pp. 82–88, 2017.

[3] Balraj Singh, D. Gola, K. Singh, E. Goel, S. Kuamr, and S. Jit, "2-D Analytical Threshold Voltage Model for Dielectric Pocket Double-Gate Junctionless FETs by Considering Source /Drain Depletion Effect," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 901–908, 2017.

[4] Balraj Singh, D. Gola, E. Goel, S. Kumar, K. Singh, and S. Jit, "Dielectric pocket double gate junctionless FET: a new MOS structure with improved subthreshold characteristics for low power VLSI applications," *J. Comput. Electron.*, vol. 15, no. 2, pp. 502–507, 2016.

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[1] B. Singh, D. Gola, K. Singh, E. Goel, S. Kumar, and S. Jit, "Performance Evaluation of Double Gate Junctionless Field Effect Transistor with Vertical Gaussian Doping Profile," in *2016 International Conference On Recent Trends In Electronics Information Communication Technology (RTEICT)*, 2016, pp. 675–679.

[2] B. Singh, D. Gola, K. Singh, E. Goel, S. Kumar, and S. Jit, "Temperature Sensitivity Analysis of Double Gate Junctionless Field Effect Transistor with Vertical Gaussian Doping Profile," in *2016 International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE)*, 2016, pp. 675–679.