# Preface

The scaling of the bulk MOSFETs in the sub-100 nm technology node has reached its bottleneck due to severe degradation of the threshold voltage roll-off, subthreshold swing, drain induced barrier lowering (DIBL), hot carrier effects (HCEs), gate oxide tunneling and increased source/drain parasitic resistance. A number of different non-conventional multiple-gate MOS transistor structures have been explored for sustaining the CMOS technology scaling for future generation high speed and low-power VLSI/ULSI applications. Different techniques such as the channel material and channel doping profile engineering, high-k gate oxide engineering, gate-electrode work function engineering, substrate engineering, source/drain engineering, source (drain)/channel junction engineering etc. have been used for optimizing the SCEs in various non-classical MOS structures. The MOS transistors with no source/channel and drain/channel junctions are expected to provide better scalability due to the absence of punchthrough phenomenon in the devices. Such transistors are known as Junctionless field effect transistors (JLFETs) where source, channel and drain are of the same type of material with similar type of doping throughout the structure. Since the multiple-gate structure improves the scalability due to improved control of the gate over the channel, the present thesis is designed to develop some theoretical models for investigating the effects of non-uniform channel doping engineering as well as the dielectric pocket (DP) engineering on the subthreshold characteristics expressed in terms of the channel potential, threshold voltage, drain induced barrier lowering, subthreshold swing and

subthreshold current of the double gate (DG) JLFETs. The thesis consists of SIX chapters which are briefly introduced in the following.

**Chapter-1** introduces various scaling theories and the adverse effects of scaling on the performance of the MOSFETs. Different techniques to mitigate the SCEs in the MOSFETs have been discussed. Various multiple-gate non-classical MOSFET structures including the DG-JLFETs have also been introduced for achieving better scalability with improved SCEs than the conventional bulk MOSFETs. Finally, the scopes of the present thesis have been outlined on the basis of the literature survey carried out in this chapter.

**Chapter-2** presents the analytical models for the two-dimensional (2D) channel potential and threshold voltage of DG-JLFETs with a vertical Gaussian-like doping profile in the channel region. The evanescent mode analysis has been used to determine the channel potential by solving 2D Poisson's equation in the channel region. The derived 2D channel potential is then used to define the effective conduction path parameter which is further used to obtain model the threshold voltage for DG-JLFETs under study. In addition to the various doping profile parameters, the effects of other device parameters on the channel potential and threshold voltage are also investigated in details. All the results obtained from the modeling have been compared with the numerical simulation data obtained by using the commercially available ATLAS $^{TM}$ 2D device simulator.

**Chapter-3** deals with the modelling and ATLAS$^{TM}$ based simulation of the subthreshold current and subthreshold swing of DG-JLFETs with the vertical Gaussian-like doping profile in the channel region as considered in **Chapter-2**. The effective conduction path potential is derived in chapter-2 is used to obtain the subthreshold swing. The effects of parameters such as gate length, straggle parameter,

oxide thickness and channel thickness on the subthreshold current and subthreshold swing have been demonstrated. Finally, theoretical results have been compared with ATLAS$^{TM}$ simulation data to validate the observed results.

**Chapter-4** is devoted to the analytical modeling and ATLAS$^{TM}$ based simulation of the channel potential and threshold voltage of the dielectric pocket (DP) based DG JLFETs with a uniform channel profile. In this case, the two dielectric pockets are used at the source and drain sides to control the opening of source/channel and drain-channel junctions. The length and thickness of the dielectric pockets provide additional flexibilities for optimizing the subthreshold characteristics of the DG JLFETs. The 2D channel potential has been derived by solving the 2D Poisson's equation with suitable boundary conditions following the evanescent mode of analysis as used in **Chapter-2**. The effects of source and drain depletion regions have been included for improving the accuracy of the model. The derived channel potential has then been used to model the threshold voltage of the device. The effects of dielectric pocket (DP) length and thickness on channel potential, threshold voltage and drain induced barrier lowering have been investigated. The proposed model results have been compared with the ATLAS $^{TM}$ based TCAD simulation results to validate the proposed models of the DP DG-JLFETs studied in this chapter.

**Chapter-5** presents the modeling of the subthreshold current and subthreshold swing of DP DG-JLFETs considered in **Chapter-4**. The effects of DP length and thickness as well as other device parameters on the subthreshold current and subthreshold swing have been discussed. Finally, the model results have been validated by comparing them with the TCAD simulation results obtained by using the commercially available ATLAS $^{TM}$ 2D device simulation software.

**Chapter-6** includes the overall conclusions of the thesis drawn from the results presented in the previous chapters. Finally, the possible future scope of research in the related area of the present thesis is presented at the end of this chapter**.**