Chapter 5

Analytical Modeling of Subthreshold Current and Subthreshold Swing of DP- DG-JLFETs

5.1 Introduction

It is already discussed in Chapter-1 that the optimization of the subthreshold current of the MOS transistors is very important for optimizing the static power loss in the CMOS circuits and systems. On the other hand, the subthreshold swing parameters of the MOS devices determine the switching of the CMOS digital switching circuits and systems. Thus, after developing the analytical model for the channel potential and threshold voltage of our newly proposed DP-DG-JLFET in Chapter-4, we have devoted the present chapter for developing analytical models for the subthreshold current and subthreshold swing characteristics of our proposed device. The outline of the present chapter is given in the following:

In Sec. 5.2, we have used the results of channel potential model developed in Sec. 4.2 for developing the subthreshold current model of the proposed DP-DG-JLFET device by including the source/drain depletion effect. Using the results of the subthreshold current, we have also modeled the subthreshold swing for the DP-DG-JLFET in this section. Section 5.3 presents results and discussions related to the subthreshold current and subthreshold swing characteristics of the DP-DG-JLFETs under study. The model

results have been compared to the simulation data for validation purposes. Finally, Sec. 5.4 includes the summary and conclusion of the present chapter.

5.2 Model Derivation

The device structure of DP-DG-JLFETs under study, shown in Fig.5.1, is same as in Chapter 4. But, we have reproduced Fig 5.1 for the better understanding of the work carried out in this chapter. In Fig.5.1, $t_{si}, L, t_{PL} = \left(\frac{t_{si}}{2} - a\right), t_{ox}, T_{side}, d_S, d_d$ and $2a$ represents the silicon channel thickness, channel length, DP length, gate oxide thickness, DP thickness, source depletion width, drain depletion width and the vertical space between the pockets with V_{gs} and V_{ds} as the gate-to-source and drain-to-source voltage, respectively. The source, drain and gate contacts are represented as S, D and G, respectively. The x and y-axes of the device are pointing towards the drain and normal to Si/SiO_2 interface respectively, as shown in the Fig.5.1.

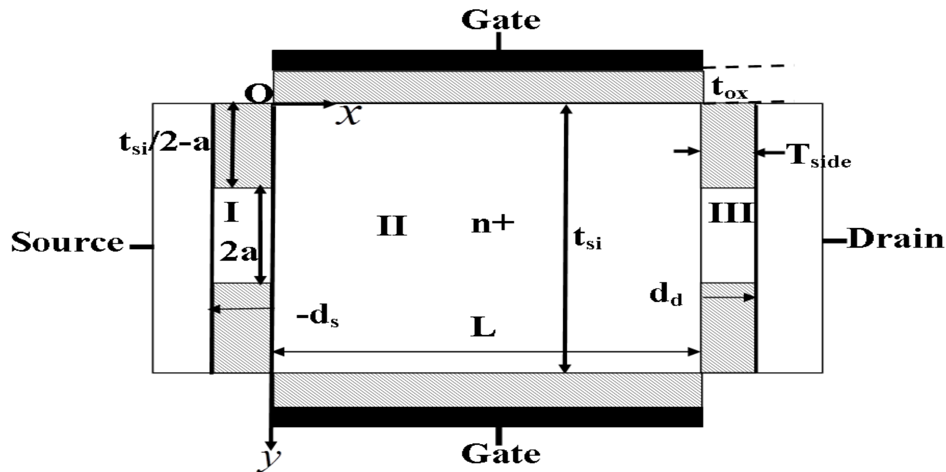

Fig.5.1: Simplified two-dimensional schematic view of DP-DG-JLFETs.

5.2.1 Subthreshold Current Model

The subthreshold current is proportional to the carrier concentration at the minimum channel potential position (virtual cathode) as calculated in subsection 4.2.1 for the same DP-DG-JLFET structure. Therefore, by employing the 2-D channel potential function derived in sub-section 4.2.1 and following the methodology used by Gnudi, *et al*. [Gnudi, *et al*.(2013)] the expression of subthreshold current can be written as follows:

The drain-to-source subthreshold current can be written as [Gnudi, *et al*. (2013)],

$$I_{DS} = \frac{q\mu_n W V_T n_{ieff}\left(1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right)}{\int_{-ds}^{L+d} d\frac{dx}{\int_{\frac{t_{si}}{2}-a}^{\frac{t_{si}}{2}+a}\exp\left(\frac{\psi(x,y)}{V_T}\right)dy}} \tag{5.1}$$

where, μ_n, W, V_T are the effective electron mobility, channel width, and thermal voltage. For analytical simplification, the subthreshold current (I_{DS}) is approximated as [Gnudi, *et al*. (2013)],

$$I_{DS} = \frac{q\mu_n W V_T n_{ieff}\left(1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right)}{\int_{x_1}^{x_2}\frac{dx}{\int_{\frac{t_{si}}{2}-a}^{\frac{t_{si}}{2}+a}\exp\left(\frac{\psi_{\min}(x,y)}{V_T}\right)dy}} \tag{5.2}$$

where, $\psi_{\min}(x,y) = U(y) + V(x_{\min}, y)$ and, x_1 and x_2 are calculated by solving the following equation[Gnudi, *et al*. (2013)],

$$\exp\left(\frac{\psi(x_{1,2}, \frac{t_{si}}{2})}{V_T}\right) = 2\exp\left(\frac{\psi_{\min}(x, \frac{t_{si}}{2})}{V_T}\right) \tag{5.3}$$

The subthreshold current finally expressed as

$$I_{DS} = \exp\left(\frac{A^2 + 4I_1I_2}{4I_1V_T}\right)\sqrt{\left(\frac{\pi V_T}{4I_1}\right)} \times \left\{erf\left(\frac{2I_1t_{si} - A}{2\sqrt{I_1V_T}}\right) - erf\left(\frac{-A}{2\sqrt{I_1V_T}}\right)\right\} \tag{5.4}$$

where,

$$I_1 = \left[\frac{qN_d}{2\varepsilon_{si}} + \frac{\eta^2}{2}\left(\frac{V_1\sinh(\eta(L - x_{\min})) + U_1\sinh(\eta x_{\min})}{\sinh(\eta L)}\right)\right] \tag{5.5}$$

$$I_2 = \left[B + \left(\frac{V_1\sinh(\eta(L - x_{\min})) + U_1\sinh(\eta x_{\min})}{\sinh(\eta L)}\right)\right] \tag{5.6}$$

5.2.2 Modeling of Subthreshold Swing (SS)

SS is an important parameter to assess the subthreshold characteristics and reflects the short channel behaviour of nanoscale devices. It estimates the amount of change in gate bias to modulate the drain current ten times. Mathematically, SS can be written as [Gnudi, *et al.(*2013)].

$$SS = \left(\frac{\partial(\log I_{DS})}{\partial V_{gs}}\right)^{-1} \tag{5.7}$$

$$SS = \frac{V_T \ln(10)}{\left(\dfrac{\partial \psi_{\min}(x, \frac{t_{si}}{2})}{\partial V_{gs}}\right)} \tag{5.8}$$

$$SS = \frac{V_T \ln(10)}{1 + \dfrac{K_S (V_1 + U_1) Cos\left(\dfrac{\eta t_{si}}{2}\right)}{2\sqrt{V_1 U_1} Sinh(\eta L)} \exp\left(\dfrac{\eta L}{2}\right)} \tag{5.9}$$

where

$$K_S = -\left(\frac{4 Sin(\eta t_{si})}{\eta\left(2t_{si} + \eta^{-1} Sin(2\eta t_{si})\right)}\right) \tag{5.10}$$

5.3 Results and Discussion

In this section, the proposed model results are compared with simulated results obtained by the ATLAS™ 2D device simulator for different device parameters. The 2D numerical simulations are carried out in a similar manner as in Chapter 4 by using the *conmob*, *fldmob* , *prpmob consrh*, *auger* and *bgn* models. While the *conmob*, *fldmob* and *prpmob* models have been used for the concentration dependent mobility, lateral electric field dependent mobility and perpendicular electric field dependent mobility, respectively. The *consrh* and *auger* models have been used in the ATLAS TCAD for the

Shockley–Read–Hall recombination with concentration dependent lifetime and auger recombination at high carrier density respectively. The *bgn* model is used to include the band gap narrowing effect due to high concentration in the channel region. For the validity of our model, we have compared our model results in chapter 4 with the ATLAS™ TCAD simulation data duly calibrated by comparing them with the experimental results for non-planar silicon-on-insulator-Junctionless Transistor (SOI-JLT) [Colinge *et al.* (2010)].

The subthreshold current has been plotted against gate-to-source voltage for different DP lengths and DP thicknesses in Fig.5.2 and Fig.5.3, respectively. The subthreshold current is decreased with increased DP length due to the increase in the source to channel potential barrier. Fig.5.3 shows that the subthreshold current is also decreased with the increased DP thickness but becomes constant for the DP thickness beyond ~5nm possibly due to the complete suppression of lateral electric field in the channel [Singh *et al.* (2016)].

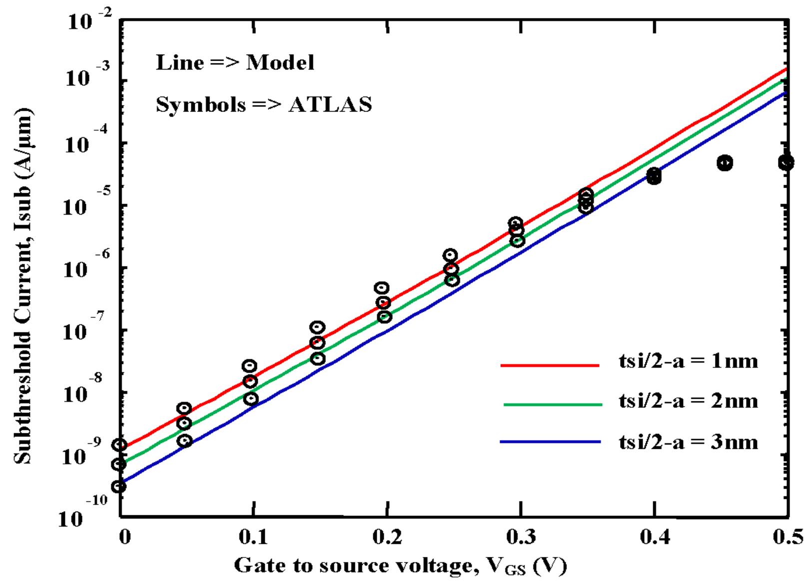

Fig.5.2 : Variation of subthreshold current against gate-to-source voltage for different DP lengths at $t_{ox} = 1.5\,\text{nm}, t_{si} = 10\,\text{nm}, T_{side} = 7\,\text{nm}, V_{ds} = 0.1\,\text{V}$.

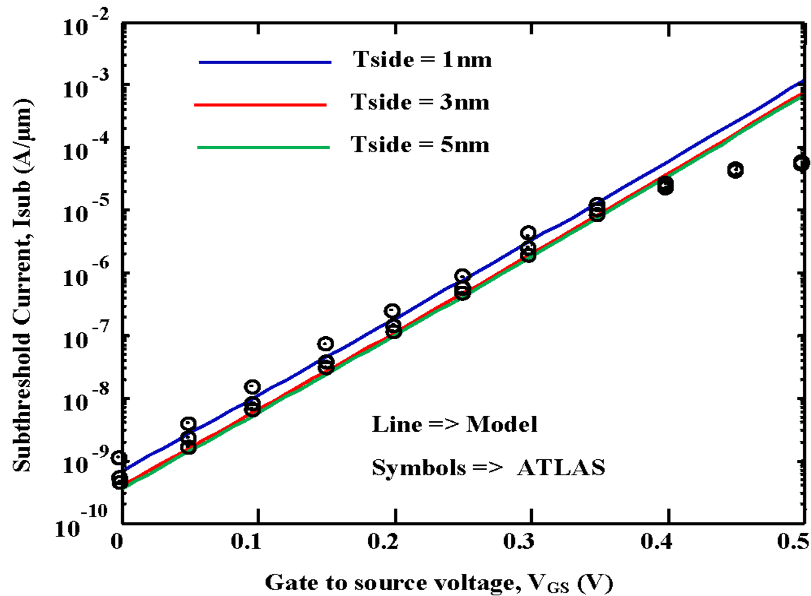

Fig.5.3: Variation of subthreshold current against gate-to-source voltage for different DP thicknesses t_{PL}=3nm, $t_{ox} = 1.5\,\text{nm}, t_{si} = 10\,\text{nm}, V_{ds} = 0.1\,\text{V}$.

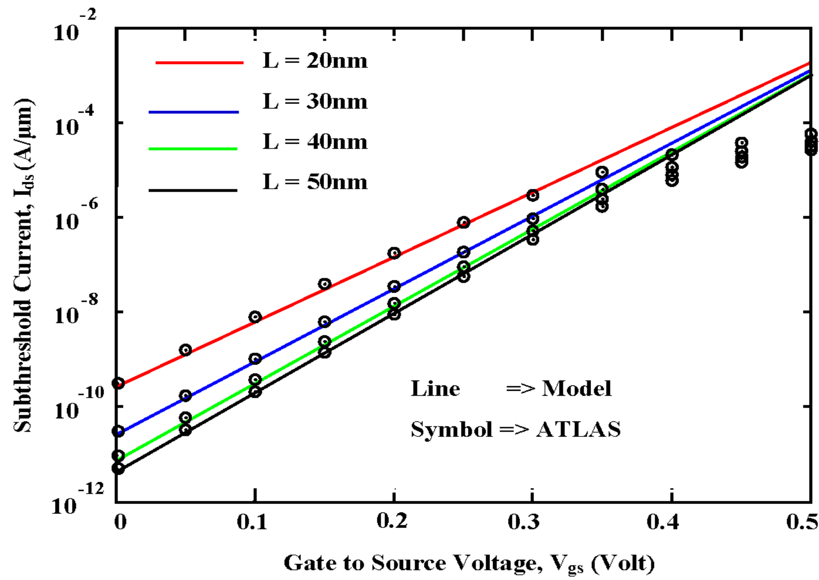

Fig.5.4: Subthreshold current variation with gate-to-source voltage for different gate lengths at t_{PL} =3nm, $t_{ox} = 1.5$ nm, $t_{si} = 10$ nm, $T_{side} = 7$ nm, $V_{ds} = 0.1$ V.

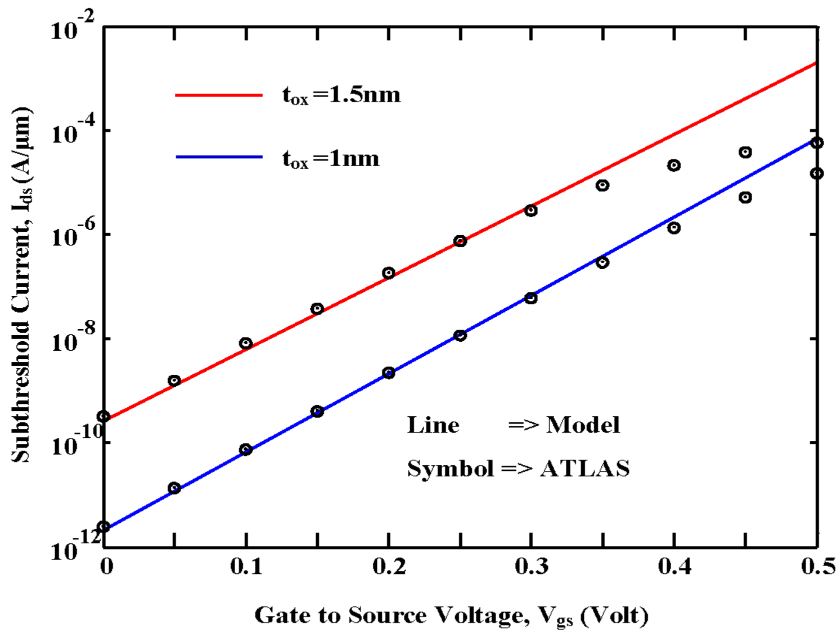

Fig.5.5: Subthreshold current versus gate-to-source voltage for different oxide thickness at t_{PL} =3nm, $t_{si} = 10$ nm, $T_{side} = 7$ nm, $V_{ds} = 0.1$ V, L=20nm.

In Fig.5.4, we have shown the variation of subthreshold current as a function of gate voltage for different channel length. It has been observed from figure that the subthreshold current increases with the decrease in the channel length. This may be due to the loss of control over the channel, due to increase in minimum central potential with decrease in channel length. The analytical results deviate from simulation results beyond certain gate voltage when the DP-DG-JLFET starts to enter into the ON state for which the proposed model is not applicable [Jiang et *al.* (2015)].

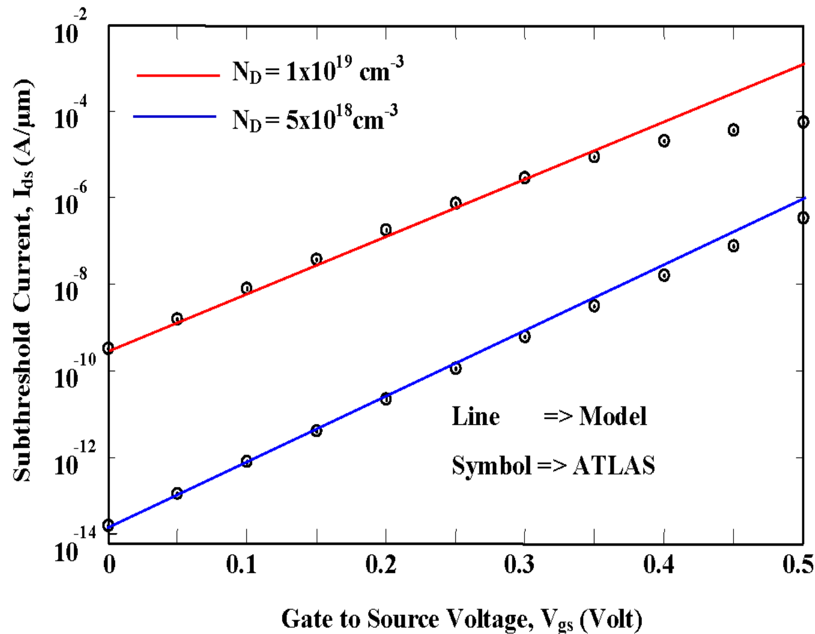

Fig.5.6: Subthreshold current versus gate-to-source voltage for different doping concentration at t_{PL}=3nm, t_{si} = 10 nm, T_{side} = 7 nm, V_{ds} = 0.1 V, L=20nm, t_{ox} = 1.5 nm.

Fig. 5.5 demonstrated the effect of gate oxide thickness on the subthreshold current for fixed gate to source voltage. The subthreshold current is observed to be decreased with

the gate oxide thickness due to the increase in gate control over the channel.

The effect of doping concentration on the subthreshold current for fixed gate-to-source voltage has been demonstrated in Fig.5.6. The increase in the subthreshold current with the doping concentration is attributed to the increase in minimum channel potential with increased channel doping.

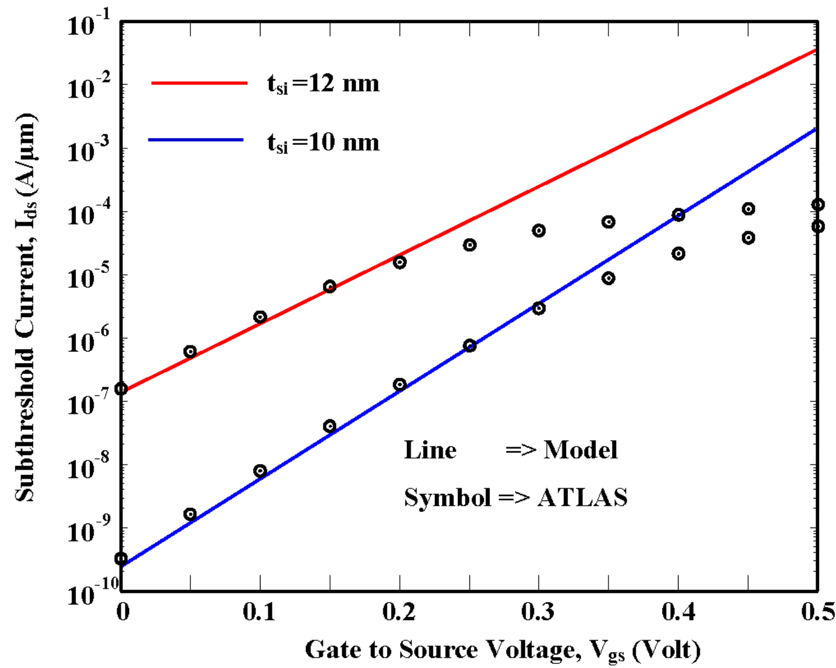

Fig.5.7: Subthreshold current versus gate-to-source voltage for different channel thickness at t_{PL}=3nm, $t_{si}=10\,\text{nm}$, $T_{side}=7\,\text{nm}$, $V_{ds}=0.1\,\text{V}$, L=20nm, $t_{ox}=1.5\,\text{nm}$.

The effect of channel thickness on the subthreshold current has been demonstrated in Fig.5.7 for t_{Si} = 10nm and 12 nm. The increase in the subthreshold current with the channel thickness is resulted from the reduction in gate control over the channel. We have investigated SS characteristics in Fig.5.8 and Fig.5.9 for different DP lengths and

DP thicknesses, respectively. Note that SS characteristics are severely degraded for the channel lengths below 60nm. While the SS improves with the increase in the DP length, it also improves significantly for DP thickness below 5nm owing to the complete suppression of the lateral electric field [Singh *et al.* (2016)]. The model results are found to be in good agreement with the TCAD simulation data.

Thus, in brief, the use of DP in the DG-JLFETs can provide better flexibility of optimization of the subthreshold characteristics of the DP-DG-JLFETs under consideration in the present chapter.

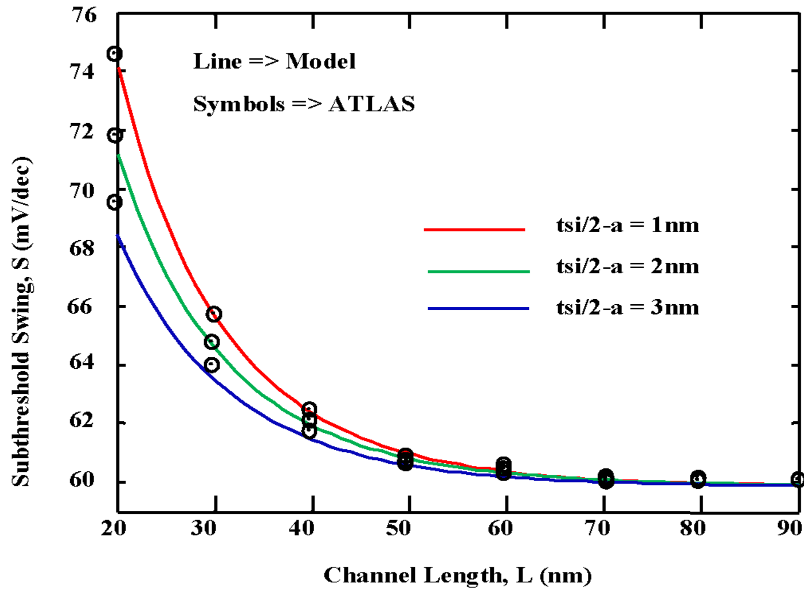

Fig. 5.8: Variation of subthreshold swing against gate-to-source voltage at t_{PL} =3nm, $t_{si} = 10\,\text{nm}, T_{side} = 7\,\text{nm},\ V_{ds} = 0.1\,\text{V},\ L\text{=20nm}, t_{ox} = 1.5\,\text{nm}$

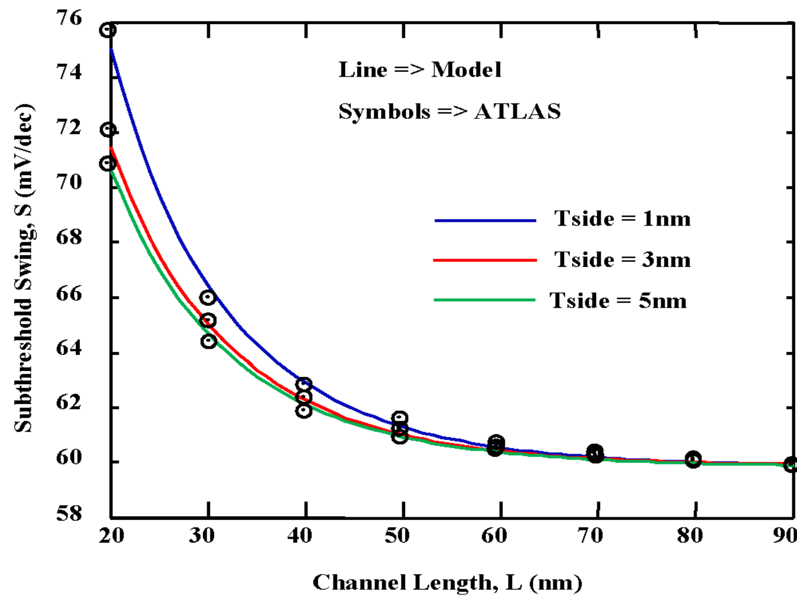

Fig.5.9: Variation of subthreshold swing against gate-to-source voltage at t_{PL}=3nm, $t_{si}=10\,\text{nm}, T_{side}=7\,\text{nm}, V_{ds}=0.1\,\text{V}, L$=20nm, $t_{ox}=1.5\,\text{nm}$.

5.4 Conclusion

This chapter reports the 2D modeling of subthreshold current and subthreshold swing of the DP-DG-JLFETs in which source/drain depletion effect has been incorporated for accurate results. It is demonstrated that the subthreshold characteristics of DP-DG-JLFETs can be controlled not only by the device parameters but also by controlling the dielectric pocket length and thickness. The subthreshold leakage current is increased with the decrease in pocket length, decrease in pocket thickness, decreased channel length; increased oxide thickness increased channel concentration and increased channel thickness. Further, SS is observed to be deteriorated very rapidly with decreased DP length and DP thickness below 60 nm. Thus, the device provides additional flexibility

for optimizing the subthreshold current and SS by optimizing the values of the DP lengths and thickness.