Chapter 4

Analytical Modeling of Channel Potential and Threshold Voltage of Dielectric Pocket DG-JLFETs

4.1 Introduction

The review of the state-of-the-art research on the dielectric pocket (DP) engineering discussed in Chapter-1 shows DPs can be used to suppress the short-channel effects, lateral electric field penetration from drain to source, gate leakage current and hot carrier effects in single and double gate (DG) MOS transistors [Jurczak *et al*.(2001), Shih *et al*.(2004), Gili *et al*.(2006), Kok *et al*.(2009), Kaur *et al.*(2007a), Kaur *et al.*(2007b), Kumari *et al.*(2012)]. Kumari *et al.* have reported an analytical model for demonstrating higher I_{on}/I_{off} ratio, higher device gain and, lower values of intrinsic delay and power dissipation of DP-DG-MOSFETs over the conventional DG-MOSFETs without DP engineering. In this chapter, an attempt has been made to develop a theoretical model for investigating the potential distribution, threshold voltage and DIBL characteristics of a newly proposed DP-DG-JLFET structure obtained by combining the features of both the DP-DG-MOSFETs and DG JLFETs in the single MOS transistor structure. It has been shown that the parameters of the DP can provide additional flexibility for the performance optimization of the DP-DG-JLFETs under study. The outline of the present chapter can be given below:

Section 4.2.1 describes the 2D channel potential function obtained by solving the 2D Poisson's equation using evanescent mode analysis method. The threshold voltage of the DP-DG-JLFETs has been modeled in Sec.4.2.2. The results and discussion have

been presented in Sec. 4.3. Finally, Sec.4.4 includes the conclusion of the present chapter.

4.2 Model Derivation

4.2.1 Channel Potential

A schematic structure of DP-DG-JLFETs used for the 2D channel potential modeling and simulation is shown in Fig. 4.1, where, t_{si}, L, $t_{PL}=\left(\frac{t_{si}}{2}-a\right)$, $t_{ox}, T_{side}, d_S, d_d$ and $2a$ represent the channel thickness, channel length, DP length, gate oxide thickness, DP thickness, source depletion width, drain depletion width, and the vertical space between the pockets with V_{gs} and V_{ds} as the gate-to-source and drain-to-source voltage respectively.

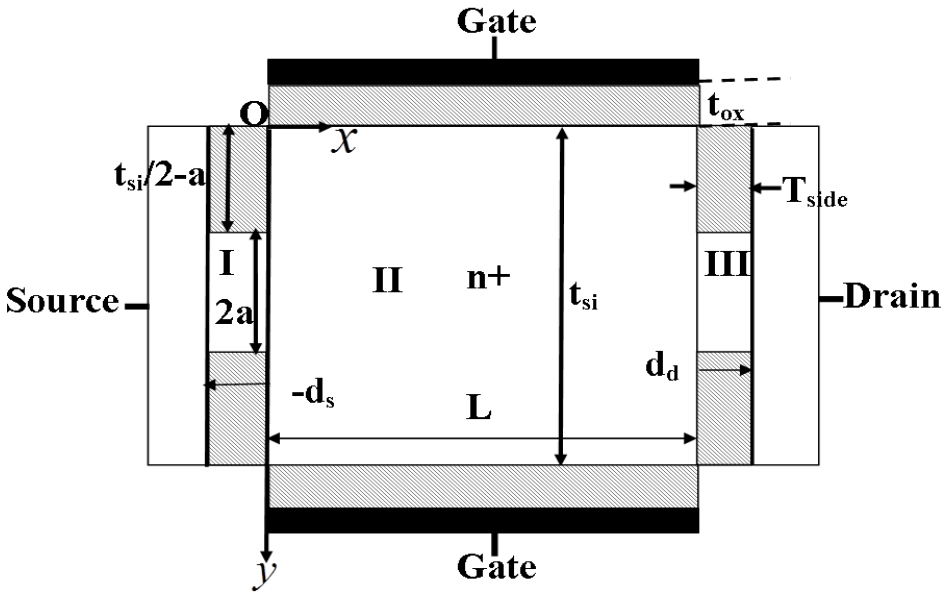

Fig.4.1: Simplified two-dimensional cross-sectional view of DP-DG-JLFET.

The source, drain, and gate contacts are denoted by S, D and G respectively. The x and y-axes of the device are pointing towards the drain and normal to Si/SiO_2 interface, respectively, as shown in the Fig.4.1.The channel is assumed to be heavily doped with a uniform doping concentration $N_d = 1\times10^{19}\,cm^{-3}$. To include the effect of band gap narrowing of Si material resulted from the high doping concentration in the channel, the change in energy band gap, effective electron affinity and effective intrinsic carrier concentration of the heavily doped Si channel can respectively be modeled as [Slotboom and Graaff (1976)]

$$\Delta E_g = BGN.E\left\{\ln\left(\frac{N_d}{BGN.N}\right)+\left[\ln\left(\frac{N_d}{BGN.N}\right)^2 + BGN.C\right]^{\frac{1}{2}}\right\} \tag{4.1}$$

$$\chi_{eff} = \chi + 0.5\left(\Delta E_g\right) \tag{4.2}$$

$$n_{ieff} = \sqrt{n_i{}^2 \exp\left(\frac{\Delta E_g}{kT}\right)} \tag{4.3}$$

where, $BGN.N = 1.0\times10^{17}\,\mathrm{cm}^{-3}$, $BGN.E = 9.0\times10^{-3}\mathrm{eV}$ and $BGN.C = 0.5$ are empirical constants; n_i is the intrinsic carrier concentration of Si.

Assuming a fully depleted channel under zero bias condition, the 2D channel potential, say $\psi(x,y)$, of the DP-DG-JLFET can be obtained by solving the following 2D Poisson's equation

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_{si}} \tag{4.4}$$

Using the Evanescent-mode analysis, $\psi(x,y)$ can be written as [Lee and Shin (2004), Dubey *et al.* (2010)]

$$\psi(x,y) = \psi_I(y) + \psi_{II}(x,y) \tag{4.5}$$

where, $\psi_I(y)$ and $\psi_{II}(x,y)$ are the 1D potential function responsible for the long-channel device characteristics and 2D potential function responsible for the short-channel effects of the device respectively.

The long-channel potential function $\psi_I(y)$ can be obtained by solving the following 1D Poisson's equation:

$$\frac{\partial^2 \psi_I(y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_{si}} \tag{4.6}$$

The general solution of equation (4.6) can be written as

$$\psi_I(y) = -\frac{qN_d}{2\varepsilon_{si}} y^2 + Ay + B \tag{4.7}$$

where the constants A and B can be obtained by using following boundary conditions in Eq.(4.7):

$$\left[\frac{\partial \psi_I(y)}{\partial y}\right]_{y=0} = -\frac{C_{ox}}{\varepsilon_{si}}\left(V_g - \psi_I(0)\right) \tag{4.8}$$

$$\left[\frac{\partial \psi_I(y)}{\partial y}\right]_{y=tsi} = \frac{C_{ox}}{\varepsilon_{si}}\left(V_g - \psi_I\left(t_{si}\right)\right) \tag{4.9}$$

where, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, $V_g = \left[V_{gs} - \frac{1}{q}(\phi_m - \chi_{e_{ff}} - \frac{E_{geff}}{2})\right]$, $E_{geff} = E_g - \Delta E_g$

[Slotboom and Graaff (1976)] and ε_{ox} are the gate oxide capacitance per unit area;

potential on gate electrode with gate bias V_{gs} and metal work function ϕ_m; effective band gap energy; and permittivity of SiO_2 respectively.

Using Eq. (4.8) and (4.9) in Eq.(4.7), the constants A and B can be written as

$$A = \frac{qN_d}{2\varepsilon_{si}} t_{si} \tag{4.10}$$

$$B = \left(V_g + \frac{\varepsilon_{si}}{C_{ox}} A \right) \tag{4.11}$$

Now, the 2D potential function, $\psi_{II}(x, y)$, can be obtained by solving the following Laplace's equation:

$$\frac{\partial^2 \psi_{II}(x,y)}{\partial x^2} + \frac{\partial^2 \psi_{II}(x,y)}{\partial y^2} = 0 \tag{4.12}$$

The general solution of Eq. (4.12) can be expressed as [Lee and Shin (2004), Dubey *et al.* (2010)]

$$\psi_{II}(x,y) = \sum_{n=1}^{\infty} \frac{\cos(\eta y)}{\sinh(\eta L)} \left[V_n \sinh\left(\eta\left(L - x\right)\right) + U_n \sinh\left(\eta x\right) \right] \tag{4.13}$$

where, V_n and U_n are arbitrary constants

It may be noted that the higher order terms in Eq. (4.13) are decayed very rapidly with the increase in n for $n \geq 2$ [Dubey *et al.* (2010)]. Thus, following the methodology reported by Dubey et al. [Dubey *et al.* (2010)], we can approximate $\psi_{II}(x, y)$ by taking only the lowest order mode with $n = 1$ for the simplicity of analysis with a better physical insight.

Thus, we obtain

$$\psi_{II}(x,y) \approx \frac{\cos(\eta y)}{\sinh(\eta L)}\left[V_1 \sinh\left(\eta\left(L-x\right)\right)+U_1 \sinh\left(\eta x\right)\right] \tag{4.14}$$

where, η is the inverse of characteristics length, which depends on the curvature of the potential at the chosen position [Oh *et al*.(2000)]. It is determined by satisfying the boundary conditions that $\psi_{II}(x,y)=0$ at Si/SiO_2 interface. This provides an equation for η.i.e. by fitting a half period of $\cos(\eta y)$ between the gate electrodes [Monroe and Hergenrother (1998), Oh *et al*. (2000)]:

$$\frac{\varepsilon_{si}}{\varepsilon_{ox}}.\tan(\frac{\eta t_{si}}{2}).\tan(\eta t_{ox})=1$$

For $t_{ox} << t_{si}$, $\eta = \dfrac{\pi}{t_{si}+\dfrac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}}}$ satisfies the above equation.

To include the effect of potential drops due to the extensions of the respective depletion lengths, d_S and d_d in the source and drain regions, the potential distributions at the source and drain regions can be respectively written by Eq.(4.15) and (4.16) described as [Gnudi *et al.*(2013)]

$$\psi(x,y)=\psi_S(x)=V_b-\frac{qN_d}{2\varepsilon_{si}}(x+d_S)^2; \qquad -d_S \le x \le 0 \tag{4.15}$$

and

$$\psi(x,y)=\psi_d(x)=V_b+V_{ds}-\frac{qN_d}{2\varepsilon_{si}}(x-L-d_d)^2; L \le x \le L+d_d \tag{4.16}$$

where $V_b = V_T \ln\left(N_d/n_{ieff}\right)$ is the quasi-Fermi potential with $V_T = kT/q$ as the thermal voltage.

The respective potentials at the source and drain ends can now be obtained from Eq.(4.15) and (4.16) as

$$\psi\left(0,\frac{t_{si}}{2}\right)=\psi_s(0)=V_b-\frac{qN_d}{2\varepsilon_{si}}d_s{}^2 \tag{4.17}$$

$$\psi\left(L,\frac{t_{si}}{2}\right)=\psi_d(L)=V_b+V_{ds}-\frac{qN_d}{2\varepsilon_{si}}d_d{}^2 \tag{4.18}$$

Assuming the $\Phi_{si\{i=1,2,3\}}(0,y)$ and $\Phi_{si\{i=1,2,3\}}(0,y)$ as the potential distributions along y at $x=0$ and $x=L$ respectively, we may define the following boundary conditions for determining the unknown constants V_1, U_1, d_S and d_d:

$$\Phi_{s1}(0,y)=\varphi_{ps}+\mathrm{P}_1 y \quad \text{for} \quad 0\le y\le\frac{t_{si}}{2}-a \tag{4.19}$$

$$\Phi_{d1}(L,y)=\varphi_{pd}+\mathrm{P}_2 y \quad \text{for} \quad 0\le y\le\frac{t_{si}}{2}-a \tag{4.20}$$

$$\Phi_{s2}(0,y)=\psi_s(0) \quad \text{for} \quad \frac{t_{si}}{2}-a\le y\le\frac{t_{si}}{2}+a \tag{4.21}$$

$$\Phi_{d2}(L,y)=\psi_d(L) \quad \text{for} \quad \frac{t_{si}}{2}-a\le y\le\frac{t_{si}}{2}+a \tag{4.22}$$

$$\Phi_{s3}(0,y)=\varphi_{ps}-\mathrm{P}_1(y-t_{si}) \quad \text{for} \quad \frac{t_{si}}{2}+a\le y\le t_{si} \tag{4.23}$$

$$\Phi_{d3}(L,y)=\varphi_{pd}-\mathrm{P}_2\lfloor y-t_{si}\rfloor \quad \text{for} \quad \frac{t_{si}}{2}+a\le y\le t_{si} \tag{4.24}$$

Where, φ_{ps}, φ_{pd} [Shih *et al.*(2004)], P_1 and P_2 can be written as

$$\varphi_{ps} = V_b - \frac{9qN_d T_{side}^2}{\varepsilon_{si}}\left[\sqrt{1+\frac{2\varepsilon_{si}V_b}{9qN_d T_{side}^2}}-1\right],$$

$$\varphi_{pd} = \left(V_b + V_{ds}\right) - \frac{9qN_d T_{side}^2}{\varepsilon_{si}}\left[\sqrt{1+\frac{2\varepsilon_{si}\left(V_b+V_{ds}\right)}{9qN_d T_{side}^2}}-1\right],$$

$$\mathrm{P}_1 = \left[\frac{\left(\psi_s(0)-\varphi_{ps}\right)}{\frac{t_{si}}{2}-a}\right] \quad \text{and}$$

$$\mathrm{P}_2 = \left[\frac{\left(\psi_d(L)-\varphi_{pd}\right)}{\frac{t_{si}}{2}-a}\right]$$

From the continuity of electric fields, we also write

$$\left.\frac{d\psi(x,y)}{dx}\right|_{x=0} = \left.\frac{d\psi_s(x)}{dx}\right|_{x=0} = -\frac{qN_d}{\varepsilon_{si}}d_s \tag{4.25}$$

$$\left.\frac{d\psi(x,y)}{dx}\right|_{x=L} = \left.\frac{d\psi_d(x)}{dx}\right|_{x=L} = \frac{qN_d}{\varepsilon_{si}}d_d \tag{4.26}$$

Note that V_1 and U_1 are the Fourier constants which can be obtained by solving the boundary conditions described by Eqs. (4.19) - (4.26) as

$$V_1 = \left[\frac{4}{2t_{si}+\eta^{-1}\sin(2\eta t_{si})}\right]\left\{\begin{matrix}\mathrm{K}_1\cos(\frac{\eta t_{si}}{2})\cos(\eta a)\\ +\mathrm{K}_2\sin(\eta t_{si})+\mathrm{K}_3\left(1+\cos(\eta t_{si})\right)\end{matrix}\right\} \tag{4.27}$$

$$U_1 = \left[\frac{4}{2t_{si} + \eta^{-1}\sin(2\eta t_{si})}\right]\left\{\begin{matrix} \mathrm{K}_4 \cos(\frac{\eta t_{si}}{2})\cos(\eta a) \\ + \mathrm{K}_5 \sin(\eta t_{si}) + \mathrm{K}_6\left(1+\cos(\eta t_{si})\right)\end{matrix}\right\} \tag{4.28}$$

where,

$$\mathrm{K}_1 = \frac{2\mathrm{P}_1}{\eta^2}, K_2 = \left[\frac{\varphi_{ps} - B}{\eta} + \frac{qN_d}{\eta^3 \varepsilon_{si}}\right], K_3 = \left[\frac{A - P_1}{\eta^2}\right]$$

$$\mathrm{K}_4 = \frac{2\mathrm{P}_2}{\eta^2}, K_5 = \left[\frac{\varphi_{pd} - B}{\eta} + \frac{qN_d}{\eta^3 \varepsilon_{si}}\right], K_6 = \left[\frac{A - P_2}{\eta^2}\right]$$

The depletion region width parameters d_S and d_d at the respective source and drain sides can be expressed as

$$d_s^2 = M_1 d_d^2 + M_2 d_d + M_3 \tag{4.29}$$

$$d_d^2 = M_1 d_s^2 - M_2 d_s + M_4 \tag{4.30}$$

where $M_1 = \frac{\exp(\eta L)}{2}$, $M_2 = \frac{\exp(\eta L)}{\eta}$,

$$M_3 = \varepsilon_{si} \frac{\left(\left(2\exp(-\eta L) - 1\right)\left(V_b - \psi_I\left(\frac{t_{si}}{2}\right)\right) - V_{ds}\right)}{qN_d \exp(-\eta L)}$$ and

$$M_4 = \varepsilon_{si} \frac{\left(\left(2\exp(-\eta L) - 1\right)\left(V_b - \psi_I\left(\frac{t_{si}}{2}\right)\right) + \left(2V_{ds}\exp(-\eta L)\right)\right)}{qN_d \exp(-\eta L)}$$

Since the minimum potential at the center is used to determine the threshold voltage of the device, from Eq. (4.5) we write

$$\psi_{\min}(x,\frac{t_{si}}{2}) = \psi_{I}(\frac{t_{si}}{2}) + \psi_{II}(x_{\min},\frac{t_{si}}{2}) \tag{4.31}$$

where $x_{\min}$ is the position of the minimum channel potential which can be obtained by solving the following relation:

$$\left.\frac{\partial\psi(x,y)}{\partial x}\right|_{x=x_{\min}} = 0 \tag{4.32}$$

which gives

$$x_{\min} = d_S + \frac{1}{2\eta}\ln\left[\frac{V_1\exp(\eta L)-U_1}{U_1-V_1\exp(-\eta L)}\right] \tag{4.33}$$

4.2.2 Threshold Voltage

The threshold voltage is the gate voltage at which the minimum central potential $\psi_{\min}(x,\frac{t_{si}}{2})$ equals to the Fermi potential V_b when the flat band voltage is measured with respect to the intrinsic Fermi level [Gnudi *et al.*(2013)]. Thus, we write

$$\psi_{\min}(x,\frac{t_{si}}{2}) = V_b \tag{4.34}$$

By solving the Eq. (4.34), the threshold voltage (V_T) can be expressed as

$$V_{Th} = \left[V_b - \frac{qN_d t_{si}^2}{8\varepsilon_{si}} + \frac{1}{q}(\phi_m - \chi_{e_{ff}} - \frac{E_{geff}}{2}) - \frac{qN_d t_{si}}{2C_{ox}} - \left\{ \left(\frac{\cos(\frac{\eta t_{si}}{2})}{\sinh(\eta L)} \right) \left[V_1 \sinh\left(\eta\left(L - x_{\min}\right)\right) + U_1 \sinh\left(\eta x_{\min}\right) \right] \right\} \right] \tag{4.35}$$

4.3 Results and Discussion

In this section, the proposed model results are compared with simulated results obtained by the ATLAS™ 2D device simulator for different device parameters. The 2D numerical simulations are carried out similarly as in Chapter 2 by using the *conmob*, *fldmob*, *prpmob consrh*, *auger* and *bgn* models. While the *conmob*, *fldmob* and *prpmob* models have been used for the concentration dependent mobility, lateral electric field dependent mobility and perpendicular electric field dependent mobility, the *consrh* and *auger* models have been used in the ATLAS TCAD for the Shockley–Read–Hall recombination with concentration dependent lifetime and auger recombination at high carrier density. The *bgn* model is used to include the band gap narrowing effect due to a high concentration in the channel region. We considered the channel thickness $t_{si} > 7\text{nm}$ for our simulation so that no significant difference is observed between the simulation results obtained with and without the inclusion of the *quantum* model as also reported by Choi *et al.* [Choi *et al.* (2011)]. We have thus deliberately excluded the quantum mechanical effects for the simplicity of our proposed model. For the validity of our model, we have compared our model results with the ATLAS™ TCAD simulation data duly calibrated by comparing them with the experimental results for non-planar silicon-on-insulator-Junctionless Transistor (SOI-JLT) [Colinge *et al.* (2010). The good matching of the TCAD data with the

experimental results for SOI-JLT in Fig.4.2 confirms the validity of the TCAD models considered in the present study. The values of gate material work function, silicon channel thickness and gate oxide thickness used for our computations are $\phi_m = 5.2eV$, $t_{si} = 10nm$ and $t_{ox} = 1.5\text{nm}$ respectively. The dielectric pockets are incorporated in the 15nm extended region of source and drain.

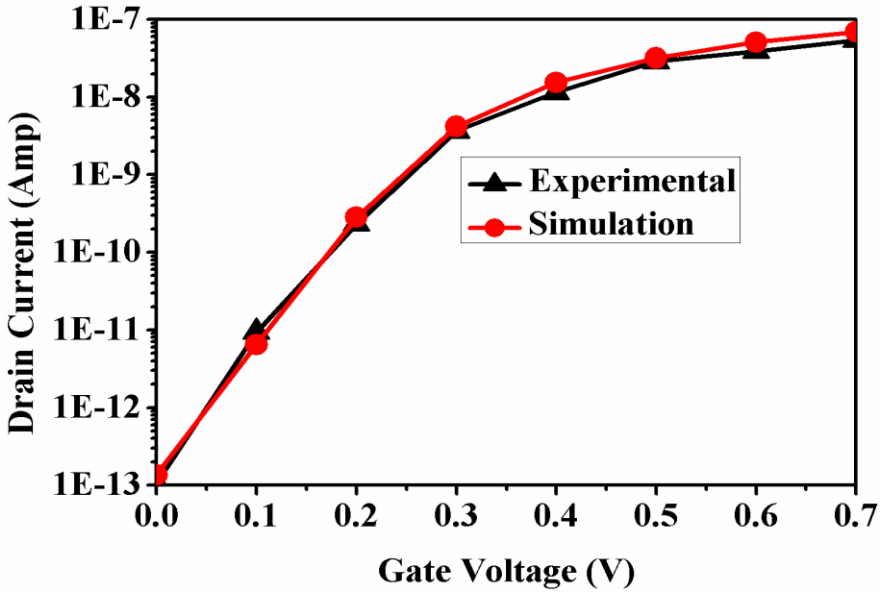

Fig.4.2: Simulation model calibration against non-planar JLFET experimental $I_{DS} - V_{GS}$ data from [Colinge *et al.* (2010)].

In Fig.4.3, we have shown the variation of central channel potential along the channel length of the device for different dielectric pocket lengths but for a fixed pocket thickness of 7nm. The central potential is significantly decreased with the increasing pocket length due to the suppression of lateral electric field in the channel region. The increased flatness of the central potential in the channel region, due to the increased pocket length, may imply the reduction in the short channel behavior of the DP-DG-JLFET structure under study. To study the effect of pocket thickness on

the channel potential, we have plotted the variation of the central potential along the channel length of the device in Fig.4.4 for different pocket thickness but with a fixed pocket length of 3nm. It is observed that the potential is decreased rapidly with the increase in the DP thickness from 1nm to 3nm. However, the rate of the decrease becomes slow and finally converges to a saturated value beyond the DP thickness of 5nm possibly due to the significant reduction in the penetration of lateral electric field into the channel. A reasonable good matching between the theory and simulation data confirms the validity of our proposed analytical model derived for the potential function of the DP DG JLFET structure under consideration.

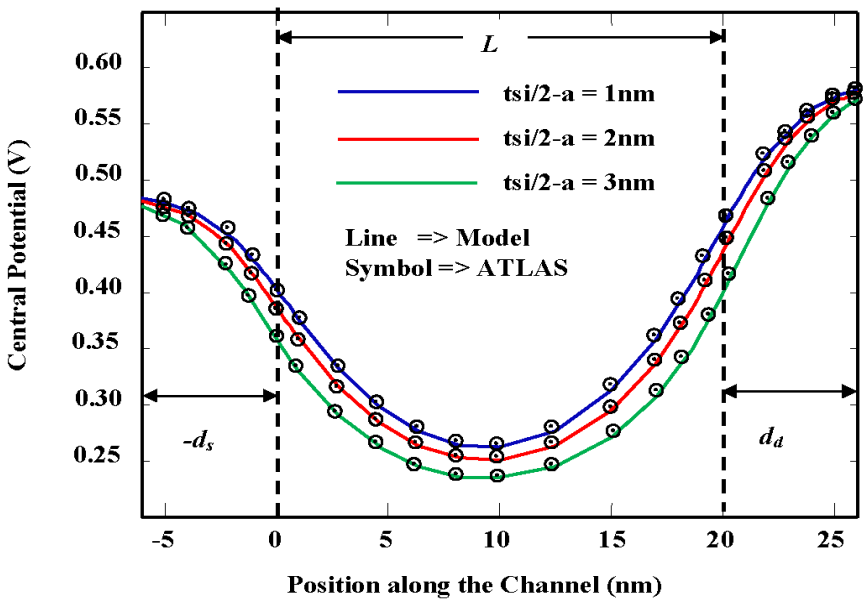

Fig.4.3: Central potential variations versus position along channel for various pocket length at $L = 20\,\text{nm}, t_{ox} = 1.5\,\text{nm}, t_{si} = 10\,\text{nm}, T_{side} = 7\,\text{nm}, V_{gs} = 0.1V$ and $V_{ds} = 0.1V$.

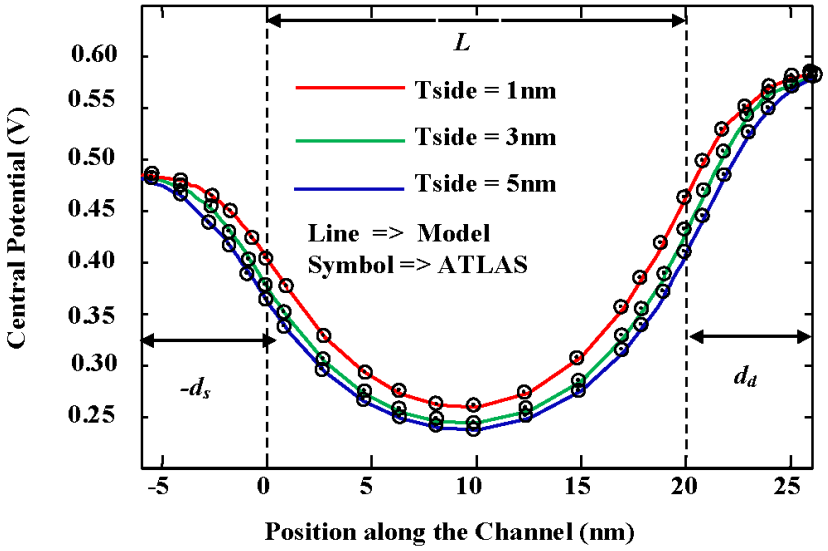

Fig.4.4: Central potential variations versus position along the channel for various pocket thickness at $L = 20\,\text{nm}, t_{ox} = 1.5\,\text{nm}, t_{si} = 10\,\text{nm}, \frac{t_{si}}{2} - a = 3\,\text{nm}$ $V_{gs} = 0.1V$ and $V_{ds} = 0.1V$.

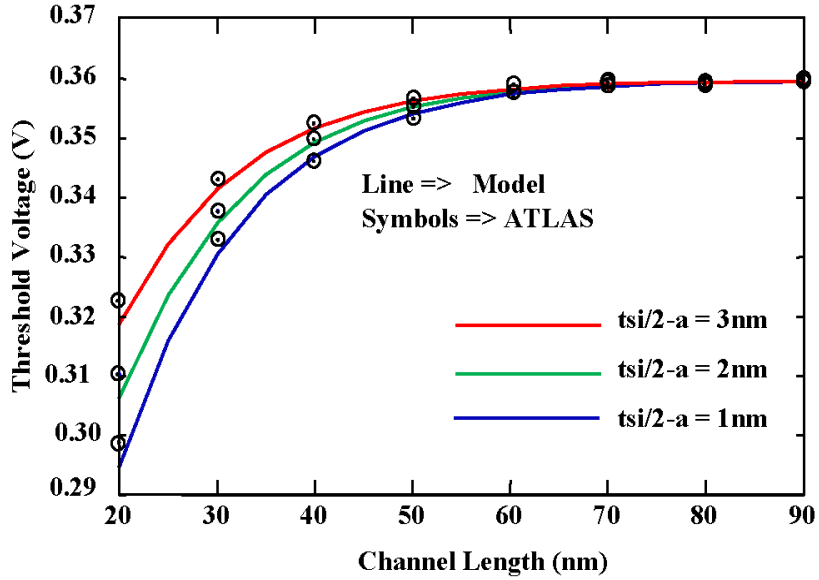

Fig.4.5: Threshold voltage variation with channel length for different pocket length at $t_{ox} = 1.5\,\text{nm}, t_{si} = 10\,\text{nm}, T_{side} = 7\,\text{nm}, V_{gs} = 0.1V$ and $V_{ds} = 0.1V$.

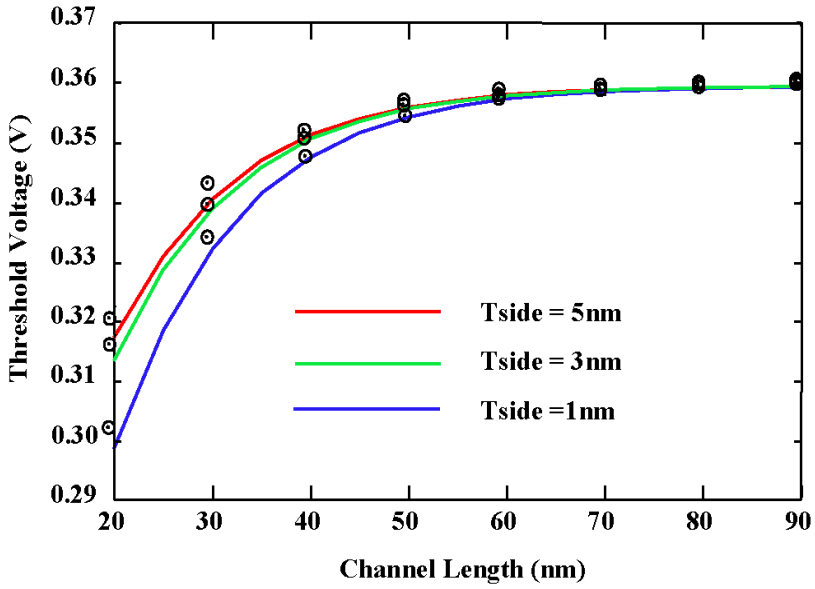

Fig.4.6: Threshold voltage variation with channel length for different pocket thickness at $t_{ox} = 1.5\,\text{nm}, t_{si} = 10\,\text{nm}, \frac{t_{si}}{2} - a = 3\,\text{nm}$ $V_{gs} = 0.1V$ and $V_{ds} = 0.1V$.

We now investigate the threshold voltage (V_{Th}) characteristics of the device as a function of channel length for different DP lengths but fixed DP thickness in Fig.4.5 and different DP thicknesses but fixed DP length in Fig.4.6. The ATLAS based simulated threshold voltage data have been extracted using constant current method [Jeon *et al.*(2013)] by assuming the drain current value $I_d = 10^{-7}\left(\frac{W}{L}\right)$ Ampere for a channel width of $W = 1\mu\text{m}$ and arbitrary channel length L. It is observed from the figures that threshold voltage, V_{Th} decreases sharply with the decrease in the gate length, DP length and DP thickness for sub-50nm gate length regime due to the increasing SCEs. In other words, the degradation in V_{Th} and V_{Th} roll-off can be compensated by increasing the length and thickness of the DP. Thus, the use of DP

can provide additional flexibility for controlling the threshold voltage of the DP-DG -JLFET structure under study.

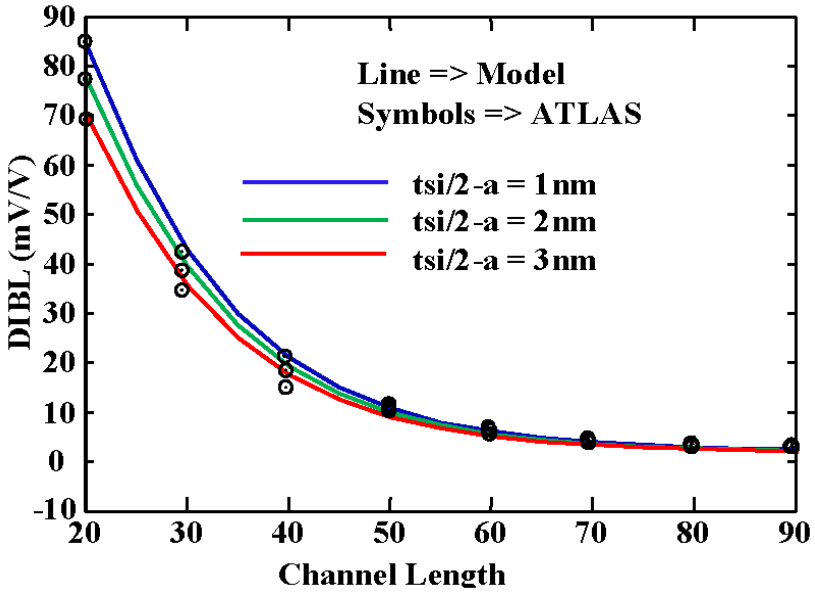

Fig.4.7: DIBL variation with channel length for different pocket length at $t_{ox} = 1.5\,\text{nm}, t_{si} = 10\,\text{nm}, T_{side} = 7\,nm, V_{ds1} = 0.1\,\text{V}$ and $V_{ds2} = 1.1\,\text{V}$.

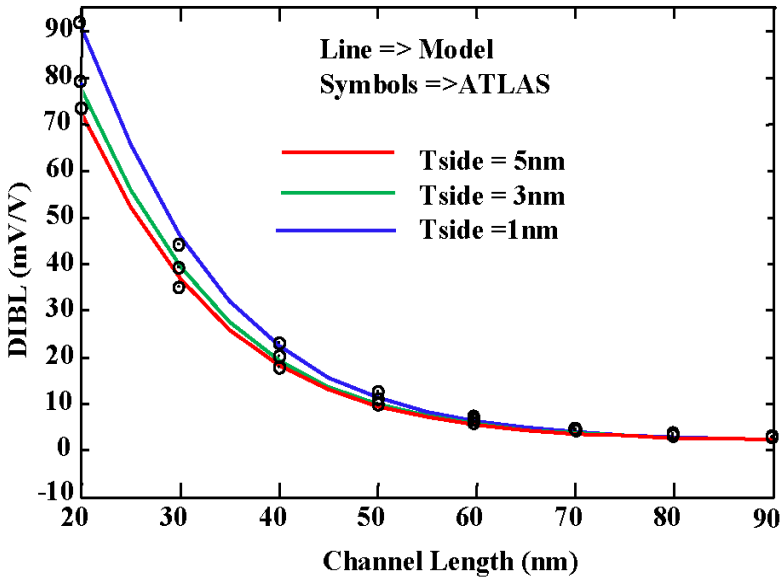

Fig.6.8: DIBL variation with channel length for different pocket thickness at $t_{ox} = 1.5\,\text{nm}, t_{si} = 10\,\text{nm}, V_{ds1} = 0.1\ \text{V},\ V_{ds2} = 1.1\,\text{V}$ and $\frac{t_{si}}{2} - a = 3\ \text{nm}$

To investigate the effect of DP dimensions on the DIBL characteristics of the device, we have defined the DIBL as the decrease in V_T for change in drain voltage from low $V_{ds1} = 0.1\,\text{V}$ to high $V_{ds2} = 1.1\,\text{V}$:

$$DIBL = \frac{V_{th}|V_{ds} = 0.1\text{V} - V_{th}|V_{ds} = 1.1\text{V}}{\left(V_{ds} = 1.1V\right) - (V_{ds} = 0.1V)} \tag{4.36}$$

The DIBL has been plotted against channel length for different DP lengths and DP widths in Fig.4.7 and Fig.4.8 respectively. In both the figures, the decrease in DIBL with the gate length is observed due to reduction in the SCEs. However, while Fig.4.7 shows an increase in the DIBL with decrease in the DP length (for a fixed DP thickness of 7 nm), the similar degradation in DIBL is also observed in Fig.4.8 for the increased DP thickness (for a fixed DP length of 3nm).

4.4. Conclusion

A new analytical model for the threshold voltage and DIBL of the newly proposed DP-DG-JLFET structure has been proposed. An analytical expression for channel potential has been derived by solving 2D Poisson's equation by taking source/drain depletion regions into consideration. The central channel potential has been used to derive the threshold voltage of the device. It is demonstrated that the degradations of the threshold voltage, threshold voltage roll-off and DIBL can be improved by increasing the DP length and DP thickness in the structure. The close matching of the model results with the ATLAS based 2D device simulation data confirms the validity of our proposed model. In brief, the additional two parameters namely the length and

thickness of the DP in the DP-DG-JLFET structure are believed to provide better flexibility of optimization of the parameters of the device considered in this chapter.