Chapter 1

Introduction and Scope of the Thesis

1.1 Introduction

The concept of the field-effect transistor (FET) was first proposed in the early 1930s by Lilienfeld [Lilienfeld (1930)] and Heil [Heil (1935)] for the possible replacement of the vacuum tube based triodes [Riordan *et al.* (1997)]. The working of a metal oxide semiconductor field effect transistor (MOSFET), first demonstrated in 1960, [D. Kahng (1960)] had initiated a revolution in the semiconductor based electronic industry in general and integrated circuit (IC) technology in particular. The MOSFETs have been the basic active devices for ICs over past few decades. The everlasting thirst of developing the fastest and energy-efficient computing systems have led to the exponential growth of the MOSFET based IC technology. The complementary semiconductor field effect transistor (CMOS) structure obtained by combining a p-channel and an n-channel MOSFET in the form of a single unit has been the basic building element in designing the modern ICs for all the modern computing and communication applications due to their negligible static power dissipation characteristics.

The miniaturization of the electronic components, called the scaling, is a process of increasing the component density per unit area in ICs. In 1965, Gordon Moore, the co-founder of Fairchild Semiconductor and Intel, had predicted a doubling in the number of components per IC every year [Moore (1965]. During the early 1970's, both Mead [C. Mead, (1972)] and Dennard *et al.* [Dennard *et al.* (1974)] proposed

"photocopy reduction" approach to feature size reduction in CMOS technology by scaling of the basic MOS transistor structure to smaller physical dimensions. Observing the progress in the scaling trend in the CMOS technology, Moore modified his forecast to doubling the number of components per IC every two years in 1975 [Moore(1975)] in place of "every year" as predicted in 1965. Interestingly, the Moore's prediction, commonly known as the *Moore's law*, has been valid over more than five decades. As consequence, the channel length of the MOS transistors has been reduced from nearly 10 µm in 1970 to sub-15nm in the present day's CMOS based IC technology. The Intel scaling trend and the Intel innovation-enabled technology pipeline have been shown in Figs. 1.1(a) and (b) respectively.

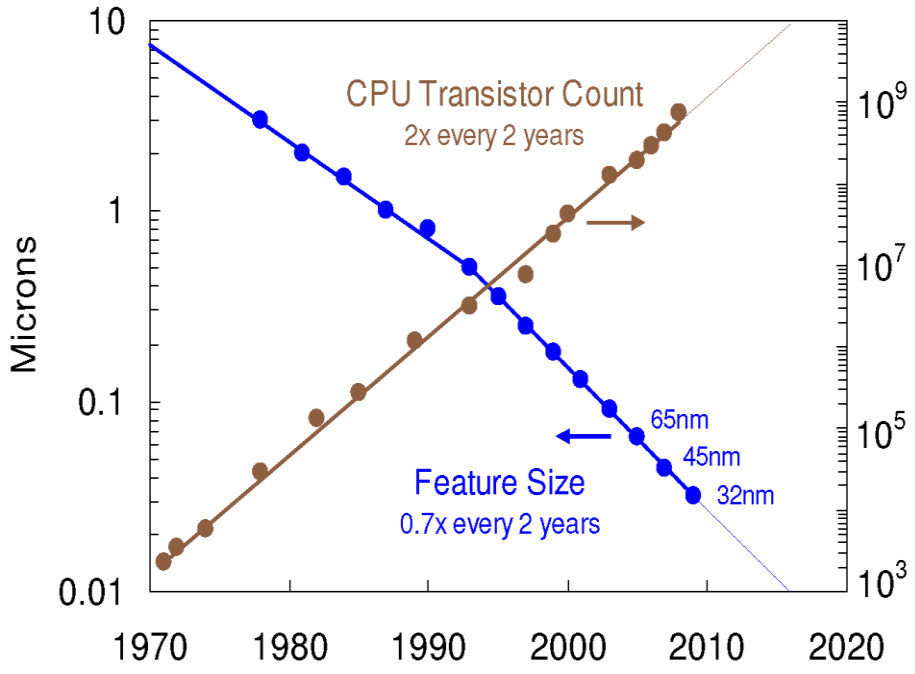

Fig.1.1 (a): Intel scaling trends and logic area scaling.

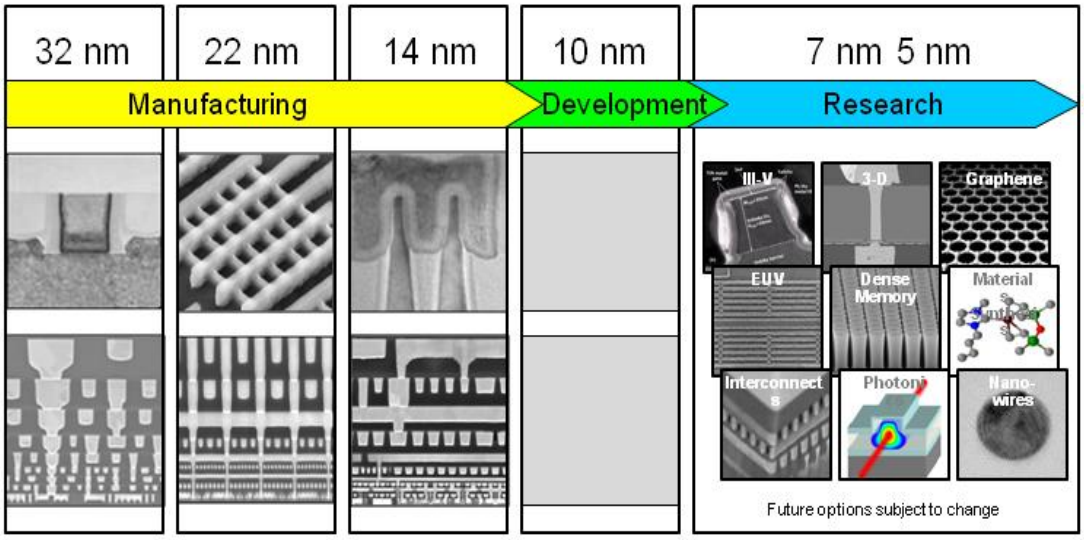

Fig.1.1 (b): Intel innovation-enabled technology pipeline [Intel and Nikon Technologists Assess Status and Future of Lithography (2017)].

The Intel scaling trend shown in Fig. 1.1 (a) follows an approximately 30% reduction in the feature size of the MOSFET [left scale] to result in a 100% increase in the transistor density on a chip every two years. This implies the reductions in the critical dimensions such as the width and length scale of a chip by a factor of $\sqrt{2}$ where the "critical dimension" refers to the term "half pitch" [Ferain *et al.* (2011), ITRS (2011)] which is defined as half the distance between identical features of a memory cell. Fig.1.1 (b) presents the Intel innovation enabled technology pipeline which shows that the Intel at present is manufacturing the 14 nm trigate Fin FET technology based ICs where 10 nm technology node is under development. The developments of 7nm and 5nm technology nodes are in the research stage [Standaert *et al.* (2016), Xie *et al.* (2015)]. Note that the "xx nm (e.g. 32 nm)" technology node refers to the average half-pitch of a memory cell at this technology level.

A number of different MOSFET scaling techniques such as the constant field scaling [Dennard *et al.* (1974)], constant voltage scaling [Critchlow (1999)], and generalized scaling [Baccarani *et al.* (1984)] have been reported in the literature for miniaturizing the MOS transistors continuously through one technology node to another. As a result, todays' electronic industry has been capable of manufacturing ICs using transistors which are 20 times faster and occupy less than 1% of the area of those built 20 years ago. The constant field scaling [Dennard *et al.* (1974)] demonstrated in Fig.1.2 suggests the scaling down of all the vertical and horizontal dimensions as well as the voltages of the device by a dimensionless constant scaling factor, k >1, with the substrate doping concentration increased by the same factor "k" to maintain the electric fields at different regions of the new device same as the unscaled device. Accordingly, the power dissipation and speed of the scaled MOS transistors are reduced by "$1/k^2$"and increased by "k" factor respectively. In the case of constant voltage scaling, all the physical dimensions of a MOS transistor are reduced by the scaling factor (k>1) similar to the constant field scaling , while the supply voltage, terminal voltages, and the threshold voltage in the MOS transistor remain unchanged. The drain current and power dissipation are increased by a factor of "k", while the power dissipation density is increased by a factor of k^3 in the constant voltage scaling [Taur and Ning (1998)]. In general, the constant field scaling is preferred for low-power applications while the constant voltage scaling is useful for designing ICs for high switching speed applications. Baccarani *et al.* [Baccarani *et al.* (1984)] have proposed a generalized scaling theory where both the electric fields and various voltages are scaled by two different extent to control both

the speed and power loss in the ICs. The three scaling rules have been compared in Table 1.1.

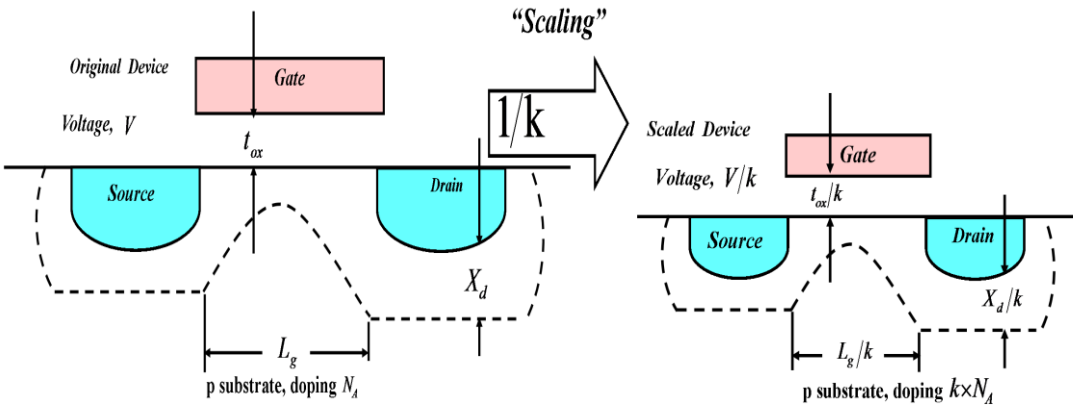

Fig.1.2: Schematic illustration of the constant field scaling of Si technology by a scaling factor "k" [Taur and Ning (1998)].

Table 1.1: MOSFET Scaling Rules [Dennard *et al.* (1974), Baccarani *et al.* (1984), Taur and Ning (1998)]

	Physical Parameters	**Multiplication Factor,** k > 1 **Scaling parameter,** α			
		Constant-field Rules	Generalized Scaling Rules		Constant Voltage Scaling
Scaling assumption	Device dimensions	1/ k	1/ k		1/ k
	Doping concentration	k	α k		K
	Voltage	1/ k	α / k		1
Derived scaling behavior of device parameters	Electric field	1	α		K
	Depletion-layer width	1/ k	1/ k		1/ k
	Capacitance	1/ k	1/ k		1/ k
	Inversion/layer charge density	1	α		K
			Long channel	**Velocity Saturation**	
	Drift Current	1/ k	α^2/k	α /k	K
	Channel resistance	1	α^2/k	α/k	1/k
	Carrier velocity	1	α	1	K
	Circuit delay time	1/ k	1/ αk	1/ k	$1/ k^2$
	Power dissipation per circuit	$1/ k^2$	α^3/ k^2	α^2/k^2	K
	Power density	1	α^3	α^2	k^3
	Power-delay product per circuit	$1/k^3$	α^2/k^3	α^2/k^3	K

The objective of different scaling rules is to ideally achieve the following major goals at every change in the technology node:

- To reduce the gate delay by 30% (by reducing the parasitic capacitance by 30%) to increase the operating frequency by nearly 43% [Borkar (1999)]
- To achieve the density of transistor per unit area nearly twice of the previous technology node [Davari *et al.* (1995)]
- To reduce the energy and active power per transition by 65% and 50% respectively [Borkar (1999)]

It is desirable that the above objectives should be achieved without deteriorating the performance of the scaled transistors. However, in reality, various performance parameters such as the threshold voltage roll-off, subthreshold current, subthreshold swing, drain induced barrier lowering, gate induced leakage current etc. are deteriorated severely due to the well-known short-channel effects (SCEs) [Taur and Ning (1998)] when the channel length of the transistors enters into sub-100nm regime. In general, a MOSFET is called a short-channel when the sum of the depletion widths formed at the source/channel and drain/channel junctions is comparable to the physical channel length of device. Thus, it is desirable that, with the scaling of the channel length, the width/depth of the depletion region at the source (drain)/channel junction should be scaled accordingly to optimize the SCEs. Since source/channel/drain forms a transistor in the conventional bulk MOSFETs shown in Fig.1.2, reduction of depletion widths below certain level is impractical in the bulk MOSFETs. As a result, the scaling of conventional bulk MOSFETs has reached to its bottleneck due to relentless scaling during last five decades. In order to eliminate the effects of source/channel and drain/channel junctions of conventional

MOSFETs, researchers have proposed the Junctionless Field Effect Transistors (JL FETs) [Colinge *et al.* (2010)], with single gate or multiple gates for achieving better scalability with improved SCEs in the MOS transistors.

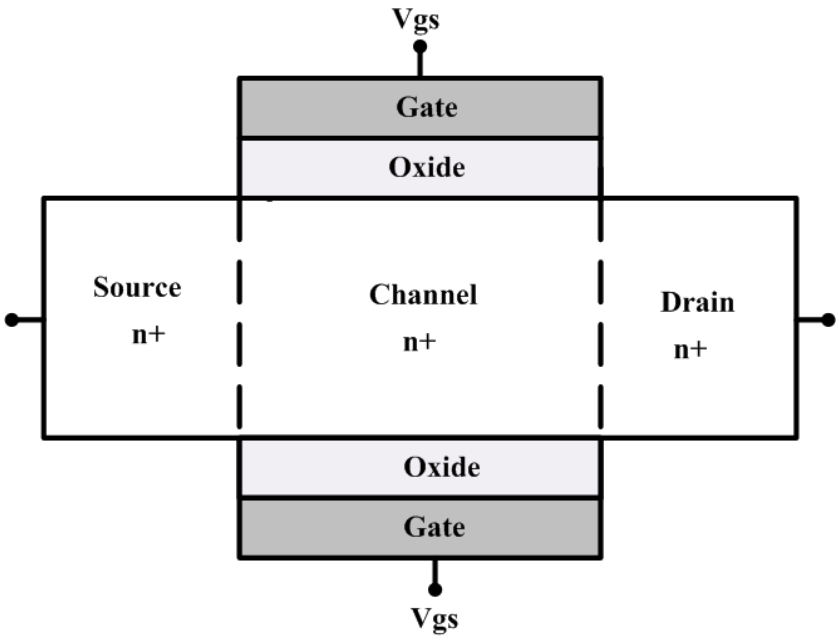

Fig.1.3: Cross-sectional view of DG JLFET.

The JLFET is a MOS transistor in which the source, channel and drain regions use same type of doping as shown in Fig.1.3. The objective of the present thesis is to develop some theoretical models for the subthreshold characteristics of the double gate (DG) JL FETs with a uniform channel doping and dielectric pockets at the source and drain sides; and DG JL FETs with a vertical Gaussian doping profile without dielectric pockets. The outline of the present chapter is given in the following.

Section 1.2 briefly introduces various SCEs in the scaled MOSFETs while Section 1.3 describes various engineering techniques to reduce/optimize the SCEs in the MOS transistors. After introducing the basic concepts and working of JL FETs in

Section 1.4, the state-of-the-art works on JL FETs have been described in Section 1.5. Finally, based on the literature survey, the scopes and chapter layout of the present thesis have been outlined in Section 1.6.

1.2 Short Channel Effects in the Scaled MOSFETs

The two main advantages of device scaling are size reduction and speed enhancement, which are the main requirements of an electronic device with good performance in today's scenario. However, the above benefits are achieved at the cost of a number of drawbacks of scaling, collectively known as the short channel effects (SCEs) in the MOS transistors. Various types of SCEs which deteriorate the electrical characteristics of the device are discussed briefly in the following subsections.

1.2.1 Threshold Voltage Roll-off

In general, the threshold voltage of long channel MOSFETs is independent of channel length. But at short channel lengths, the charge sharing between the source and drain increases thereby leading to a large amount of electric field penetration from the drain to source region [Taur and Ning (1998)] as shown in Fig.1.4. This results in lowering the potential barrier height at the source/channel junction which reduces the threshold voltage of the devices. In other words, the threshold voltage is reduced with the reduction in the channel lengths of the MOSFETs. Broadly, the threshold voltage roll-off of a MOSFET can be defined as the difference between the threshold voltages of the long-channel (i.e. the channel lengths above which the threshold voltage becomes independent of channel length) and short-channel (i.e. the

channel lengths for which the threshold voltage becomes a function of the channel length) MOSFETs.

It is important to note that the reduced source/channel barrier height allows more number of mobile charge carriers to cross the source/channel junction barrier, which, in turn, increases the subthreshold drain current in the MOS device. The increased subthreshold current increases the static power dissipation in the MOS devices which is completely undesirable for high performance and low-power IC technology.

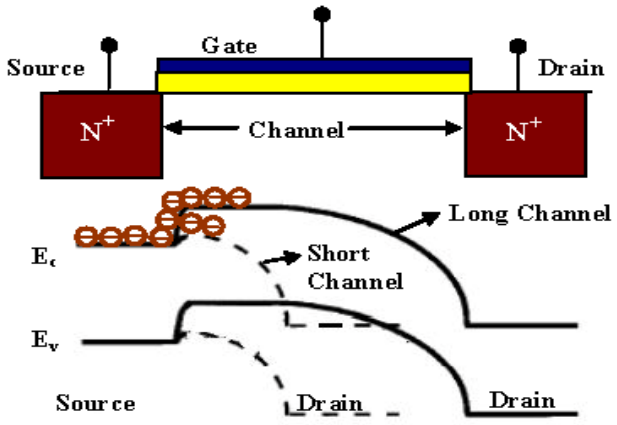

Fig.1.4: Energy band diagram for n-channel MOSFET between source and drain in off-state to describe the threshold voltage roll-off. [Taur and Ning (1998)].

1.2.2 Drain Induced Barrier Lowering (DIBL)

The threshold voltage of long channel MOSFETs is independent of the drain voltage. In such devices, any rise in the drain voltage is accounted by the lowering of energy band only at the drain side with the barrier height at the source/channel junction independent of the drain voltages. In this case, the electric field in the depletion region of the channel becomes one dimensional and can be obtained by solving the

1D Poisson's equation. However, at short channel lengths, the drain electrode starts working as the second gate and the electric field becomes two-dimensional in nature which is obtained by solving a 2D Poisson equation [Troutman (1979)]. This is known as the two dimensional effects of MOSFETs. For the small geometry MOS devices, the increase in drain voltage reduces the potential barrier height in source/channel junction which is known as the drain induced barrier lowering (DIBL) effect in the MOS transistors [Streetman (2009)]. Clearly, the DIBL results in the reduction in the threshold voltage with the increase in drain voltage due to the reduction of the source/channel barrier. Figure 1.5 (a) shows the cross sectional view of the short channel and long channel MOSFETs while Fig. 1.5(b) demonstrates the effect of drain voltage in the reduction of the source/channel barrier height due to the DIBL phenomenon.

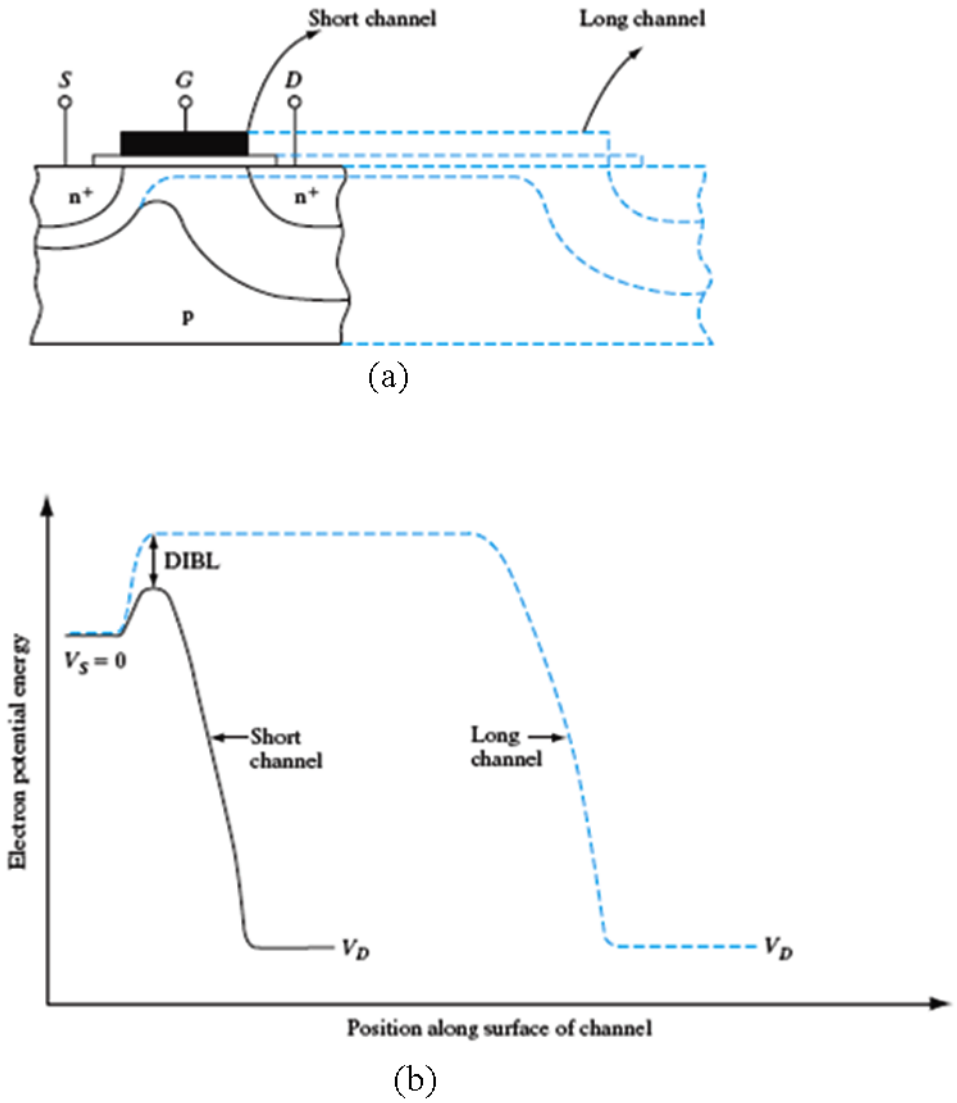

Fig.1.5: (a) Cross sections view of small channel and long channel MOSFETs **(b)** conduction band edge along the channel length for a short channel and long channel MOSFET. [Streetman (2009)].

1.2.3 Channel Length Modulation

When the drain voltage becomes greater than saturation voltage $(V_{dsat} = V_{GS} - V_{TH})$, the channel pinch-off point starts moving towards the source side with the increase in the drain voltage due to the widening of the drain depletion region as shown in

Fig.1.6. As a result, the channel length is reduced by ΔL_g (say) which, in turn, increases the drain current in the saturation region. This is known as channel length modulation in the MOSFETs [Arora (2007)]. For long channel devices where L $>> \Delta L_g$, the change in drain current is negligible and hence saturation current becomes nearly constant.

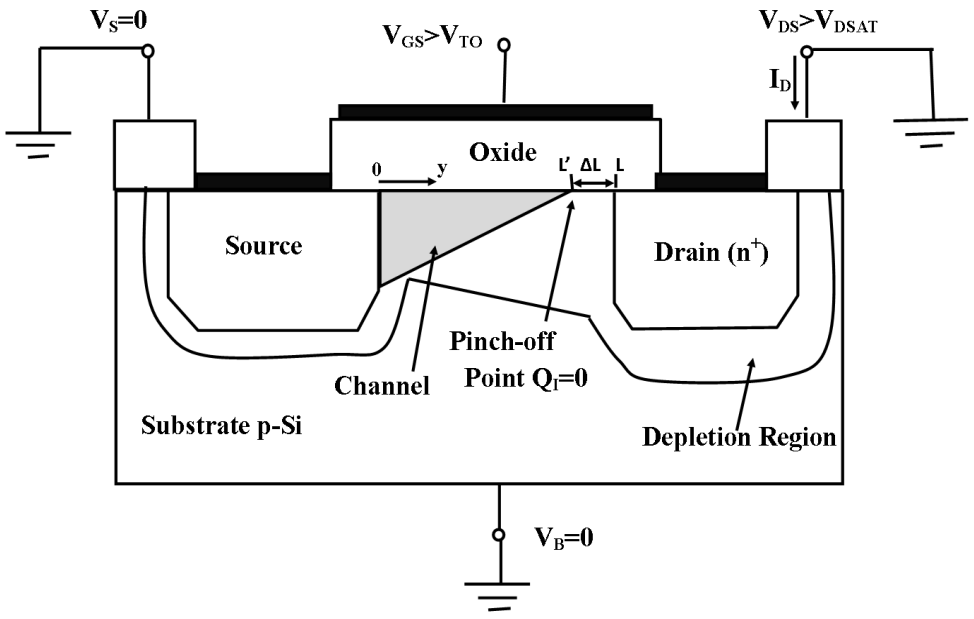

Fig.1.6: Schematic illustration of channel length modulation effect [Arora (2007)]

1.2.4 Punchthrough

Punchthrough is the extreme case of channel length modulation in a MOSFET. For zero drain voltage and gate voltage below the threshold voltage, the identical depletion regions are formed at the source/channel and drain/channel junctions of the MOSFETs. As the gate voltage exceeds the threshold voltage, a conduction path forms between source and drain. For a fixed gate voltage, the drain side depletion width expands towards the source side with the increase in the drain voltage. If the drain voltage is further increased, the drain depletion region touches the source

depletion region at certain drain voltage. This lowers the source/channel potential barrier, which in turn, increases the drain current even when the gate voltage is below the threshold voltage. The device operates abnormally due to loss of gate control over the drain. This phenomenon is called punchthrough and the current induced due to drain voltage is called punchthrough current which is demonstrated in Fig.1.7. The punchthrough is responsible for source-drain breakdown at short channel MOS devices. This phenomenon may be minimized with thinner oxides, larger substrate doping, shallower junction and obviously with larger channel lengths [Arora (2007)].

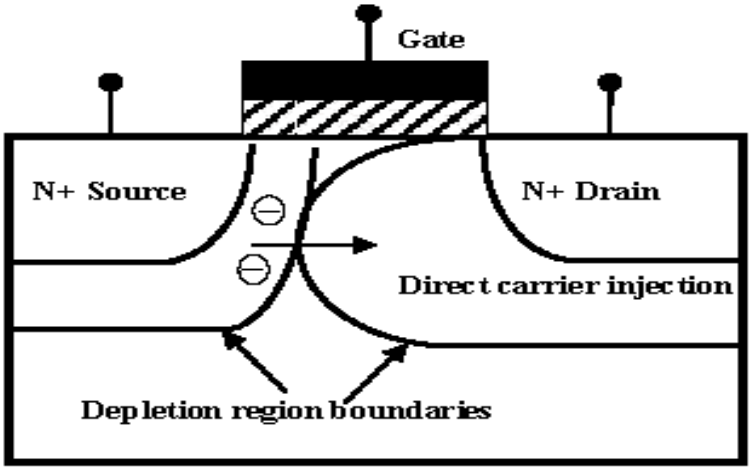

Fig.1.7: Schematic view of Punchthrough phenomena in a MOSFET [Arora (2007)]

1.2.5 Hot Carrier Effects

Hot carrier effects (HCEs) are one of the significant considerations in device design as it affects device reliability. The mobile charge carriers flowing from the source to drain acquire sufficient kinetic energy due to the high electric field at the reverse biased drain-channel junction and causes impact ionization [Arora (2007)]. Some of the carriers having energy higher than Si-SiO_2 interface barrier can lead to

conduction current through the gate and some enter into the oxide leading to degradation in device electrical characteristics as shown in Fig.1.8. The carriers having energy higher than thermal energy (kT) are called hot carriers.

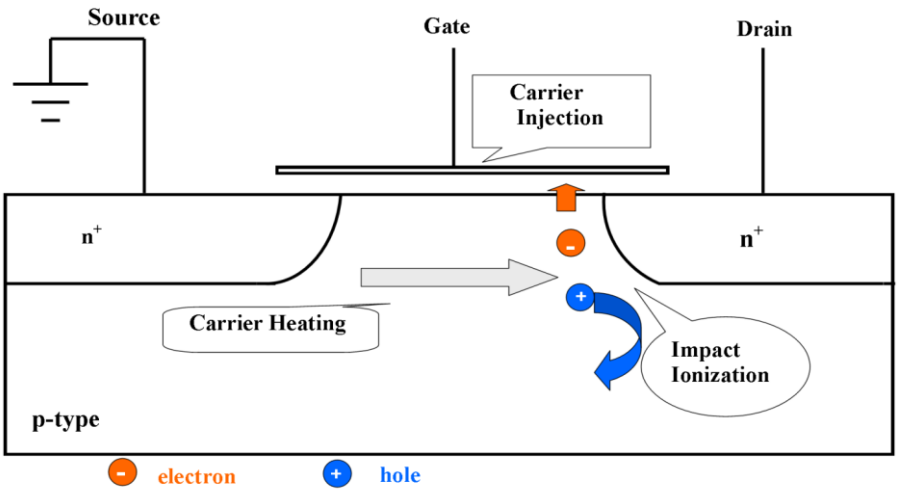

Fig.1.8: Cross-section of a MOSFET showing hot-carrier effects

1.2.6 Sub-Threshold Swing

Sub-threshold swing (SS), defined as the change of the gate voltage in sub-threshold regime to have a decade change in the drain current, is given by [Taur and Ning (1998)]:

$$SS = \underbrace{\left[1+\frac{C_s}{C_{ins}}\right]}_{m} \times \underbrace{\frac{kT}{q}\ln 10}_{n} \qquad (1.1)$$

where, C_s, C_{ins}, T and q are the channel depletion capacitance, gate oxide capacitance, temperature in degree Kelvin, q is the charge of electron , and m is the body factor of the device which represents the coupling of gate oxide to the channel, and n is the current factor which is dependent on current transport phenomenon. The minimum value, called the Boltzmann limit, of the SS is 60mV/decade for the

conventional long channel bulk MOS devices [Taur and Ning (1998)] while an ideal value of 0 mV/decade is desirable. However, for short-channel devices, the value of SS is increased with the decrease in the channel length and hence the switching performance of the device is degraded when it is used in digital circuit applications.

1.3 Device Engineering Techniques for Future Generation Technology Scaling

It is already mentioned that the scaling of conventional MOSFETs has reached its bottleneck due to severe SCEs such as the DIBL, threshold voltage roll-off, subthreshold swing, subthreshold leakage current, etc. as discussed above. The increased standby power loss due to subthreshold leakage current with reduced channel lengths has become the critical issue for sustaining future scaling of the conventional bulk MOSFETs. Establishing a tradeoff between speed and power loss with satisfactory performance of the ICs with conventional bulk MOS devices has become difficult. In view of the above, the bulk MOSFETs have been engineered in different ways for making them suitable for sustaining future generation technology scaling with reduced SCEs [Kim (2010), Ferain *et al.* (2011)]. The following subsections have been devoted to discuss some of the common engineering techniques for reducing the SCEs and sustaining scaling of the MOS devices.

1.3.1 Gate Dielectric Material Engineering

The physical thickness of SiO_2 in the MOS devices has been reached to its theoretical tunneling limit of 1.0-1.5 nm due to continuous scaling over last 5 decades. Since the

gate leakage current is increased with the reduction of the oxide thickness due to the increased quantum mechanical tunneling, the further scaling of SiO_2 thickness below 1 nm has become impossible in the MOS devices. Thus, it is important to replace the conventional SiO_2 by a high-k dielectric material so that a larger gate oxide thickness of high-k material can be used to achieve the same gate oxide capacitance as obtained by using the SiO_2 of certain thickness [Chau *et al.* (2004), Gusev *et al.* (2006)].

Suppose that ε_{SiO_2} and ε_{high-K} are the permittivities of the SiO_2 and high-k materials of respective physical thicknesses of t_{SiO_2} and t_{high-k}. For achieving the same gate oxide capacitance in both gate dielectric materials, we may write

$$\frac{\varepsilon_{high-K}}{t_{high-k}} = \frac{\varepsilon_{SiO_2}}{t_{SiO_2}} \Rightarrow t_{high-k} = \left(\frac{\varepsilon_{high-K}}{\varepsilon_{SiO_2}} \right) t_{SiO_2} \tag{1.2}$$

Since $t_{high-k} >> t_{SiO_2}$ for $\varepsilon_{high-k} >> \varepsilon_{SiO_2}$, we can use larger gate oxide thickness using high-k material than that of the convention SiO_2 material to reduce the gate tunneling current and increase the gate oxide thickness scalability of the MOS devices.

1.3.2 III-V Group Material Based MOSFET Technology

The mobility of carriers in the Si channel of conventional MOSFETs is degraded with the scaling in the nanoscale regime due to increased surface scattering. To overcome the situation, a number of III-V group materials such as GaAs, InP, InGaAs, and InAlAs have been proposed for channel material due to their higher

channel mobility than the Si [Sealy (1987)]. However, higher barrier height at the channel/gate oxide interface for Si channels than that of III-V channel materials make the Si channel based devices more reliable than the III-V materials based devices [Oktyabrsky (2010), Ueda (2010)]. Further, III-V material based devices have higher source/drain series resistance than that of the Si based devices [Passlack *et al.* (2007), Xuan *et al.* (2008)].

1.3.3 Strained-Silicon Channel Based MOSFETs

Semiconductor industries have been using the strained Si channel technology since the introduction of the 32 nm technology nodes [Takagi (2007)] for improving the on-state drain current by improving the mobility in the stained-Si of the MOS transistors [Rim *et al.* (2003), Buflera and Fichtner (2002)]. Both the uniaxial strain and biaxial strain have been explored. The uniaxial strain is created within transport surface usually in the longitudinal or channel direction, whereas the biaxial strain is normally introduced over the whole surface. However, the uniaxial strained Si MOSFETs are preferred over the biaxially strained devices due to the following reasons:

- The uniaxial strain is easier to introduce in the channel than the biaxial strain in nanoscaled MOS devices to enhance the mobility of carriers in the channel. It is very difficult to introduce biaxial strain beyond 90 nm technology nodes [Thompsom *et al.* (2004)]
- The threshold voltage variation due to uniaxial strain is much smaller than that of the biaxial strain in the channel of the MOS devices. This feature can be very useful for high-k/metal gate devices [Thompsom *et al.* (2006)].

- The hole mobility in channels with uniaxial strain can be enhanced at both low stress and high electric field due to the large band wrapping in the valance band induced effective mass reduction [Thompsom *et al.* (2004)].

1.3.4. Source/Drain Engineering

Extended lightly doped source/drain technique is used to suppress the SCEs in the scaled MOS devices [Ogura (1980)]. An angled ion implantation method is used to fabricate self-aligned n- regions between the channel and n+ source/drain regions in fully overlapped lightly doped drain (FOLD) MOSFETs as shown in Fig.1.9 [Kumar *et al.* (2000)]. The lightly doped region near drain side minimizes the electric field to control the hot carrier effect, impact ionization, punchthrough and threshold voltage of the device. This structure also offers smaller source-drain overlapping area which helps to improve the frequency response of the device [Hsu and Chiu (1984), Frank *et al.* (2001)]. However, the device shows higher source/drain resistance due to lower doping of n- regions which results in smaller on-state current than the conventional MOSFETs.

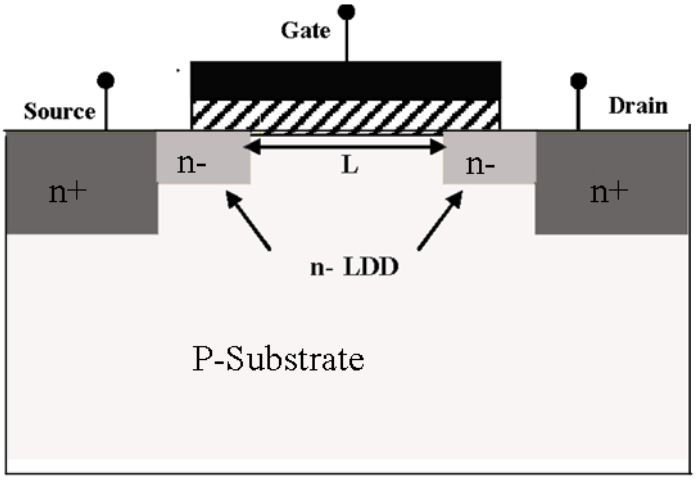

Fig1.9: Schematic diagram of the LDD MOSFET [Kumar (2000)]

1.3.5 Lateral Channel Engineering

The primary motive of lateral channel engineering is to reduce the off-state leakage current due to SCEs of the device. Halo implantation is one of the solutions to reduce the SCEs in the bulk MOSFET [Shih(2003)]. The halo implanted MOSFET is obtained by introducing highly doped pockets at the lower portion of gate controlled space charge regions as shown in the Figure.1.10 [Shih(2003)].

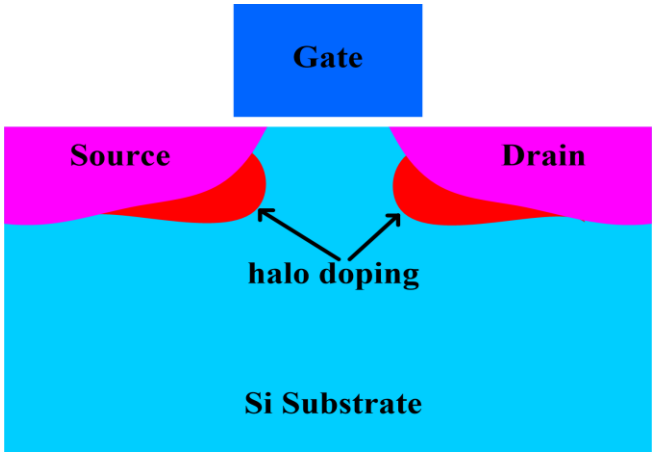

Fig.1.10: Schematic view of the halo MOSFET

This highly doped pocket is used to suppress the depletion region and off-state leakage current of the device [Schwierz (2010)]. Thus, the SCEs are minimized in terms of reduced off-state current ([Hwang et al. (1996) Shih (2003)]. However, the halo implant MOSFETs increases the risk of hot carrier effect and avalanche breakdown [Shih et al. (2003)]. Further, the performance of the device is degraded due to higher junction capacitance and larger band-to-band tunneling current.

Instead of introducing lightly doped drain/source or halo implanted regions, a new concept of introducing dielectric pockets (DP) at the source/drain sides of the channel in the bulk MOSFETs as shown in Figure1.11 has been reported in the literature [Jurczak *et al.* (2001)] to suppress the SCEs [Shih *et al.* (2003)] by removing the drawbacks of the halo implantation and lightly doped regions discussed above. The dielectric pocket (DP) MOSFETs have drawn considerable interests due to their excellent capability of suppressing the subthreshold leakage current [Jurczak *et al.* (2001), O.P. Kok and Ibrahim (2009)] by suppressing the penetration of both the lateral electric field and diffusion of carriers from the source/drain into the channel by using the DP in the side walls of the MOSFETs as shown in Fig.1.11 [Shih *et al.* (2004), Jayanarayanan *et al.* (2009), Kumari *et al.* (2012)]. Some key advantages of the DP-MOSFETs are given below:

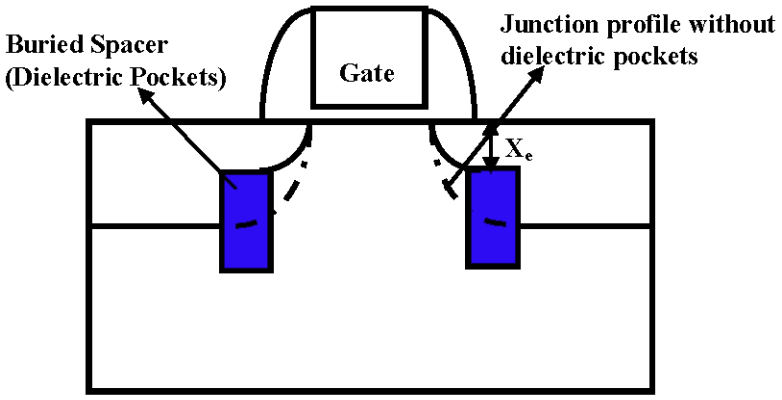

Fig 1.11: Cross-sectional view of DP-MOSFET

- DPs reduce the electrostatic source to drain coupling due to isolation of channel from source and drain.
- DPs also act as diffusion stopper for source/drain region and helps to suppress the effect of punch-through without increasing the channel doping [Kumari *et al.*(2012)]
- DPs reduce the electric field in the drain side which results in decreasing the electron. Thus, the hot carrier effects (HCEs) are reduced in DP-MOSFET.

The DP-MOSFETs have higher on-to-off state current ratio. However, the drive current and transconductance of the DP MOSFETs are smaller than the conventional MOSFETs [Jurczak *et al.* (2001)].

1.3.6 Gate Material Engineering

The carrier transport in the channel is directly related to electric field distribution in the channel. The increased lateral electric field due to decreased channel length increases the carrier velocity in the channel. For a fixed channel length, the carries may gain sufficient kinetic energy from the high electric field present near the drain side of the channel due to reverse biased drain/channel junction. Some of the

electrons may gain kinetic energy more than 3.2 eV and overcome the energy barrier at the Si-SiO_2 interface barrier. This results in undesired increase in the gate leakage current. Further, the electrons with sufficient kinetic energy may cause impact ionization at the drain side [Tam *et al.* (1984)]. This increases the probability of tunneling of carriers to enter into the gate thereby increasing the leakage current at the drain/gate junction. However, some of the tunneling carriers are trapped in gate oxide and modify the undesirable oxide charges to cause performance degradation of the MOS devices. The carriers with energy more than the thermal energy are called *hot carriers* and the performance degradation due to hot carriers is called hot carrier effects (HCEs).

The efficient way to minimize the HCEs is the use of two or more number of gate electrode materials of different work functions in a non-overlapping manner to form the gate electrode. The materials are placed in the descending order of their work functions so that the materials with the highest and lowest work function are placed at the source and drain sides respectively. Such a gate is known as hetero-material-gate (HMG) [Shur (1989)]. The HMG structures with two and triple materials have been reported as dual-material gate (DMG) [Reddy and Kumar (2005)] and triple material gate (TMG) respectively [Zhou and Long (1998), Zhou (2000)]. The presence of hetro-gate structure creates steps in the potential profile at each junction of two different materials. The highest and lowest work function materials are used to increase electric field at the source side and reduce electric field at drain side respectively. The reduced electric field at the drain side reduces the energy of the carriers to reduce the HCEs.

1.3.7 Gate Structure Engineering: Multiple Gate MOS Transistor Structures

According to the scaling theory discussed in Section 1.1, the substrate doping has been increasing continuously due to relentless scaling of the MOSFETs from one technology node to another during more than last five decades. The increased substrate doping reduces the mobility of the carriers due to increased impurity scattering, which in turn, reduces the channel current and speed of operation of the MOS devices. As a result, the scaling of single-gate MOSFETs has reached its bottleneck even after introducing all types of device engineering techniques discussed so far. Thus, researchers have introduced multi-gate MOSFET structures for sustaining scaling for future generation technology nodes. The multi-gate MOS transistor structures include FinFET (double gate) [Huang *et al.* (1999), Colinge (2004)], Trigate MOSFET [doyle *et al.* (2003)], gate-all-around (GAA) MOSFETs [Coling *et al.* (1990)], Π(pi)-gate SOI MOSFETs [Park *et al.* (2001)] and Ω(omega)-gate MOSFET [Yang *et al.* (2002)]. Figure 1.12 shows the different ways in which the gate electrodes can be wrapped over the channel region of the multi-gate MOS devices. The multiple gate MOS structures reduces the SCEs by improving the control over the channel. The above MOS devices are different from the conventional classical bulk MOSFETs and hence are called “non-classical MOSFETs.” The multiple channels formed under multiple gates of the non-classical MOS structures results in larger drive current with smaller SCEs than the conventional single gate MOS devices. The SCEs and capability of the non-classical

MOS structures can be further improved/controlled by introducing various device engineering discussed in the above subsections.

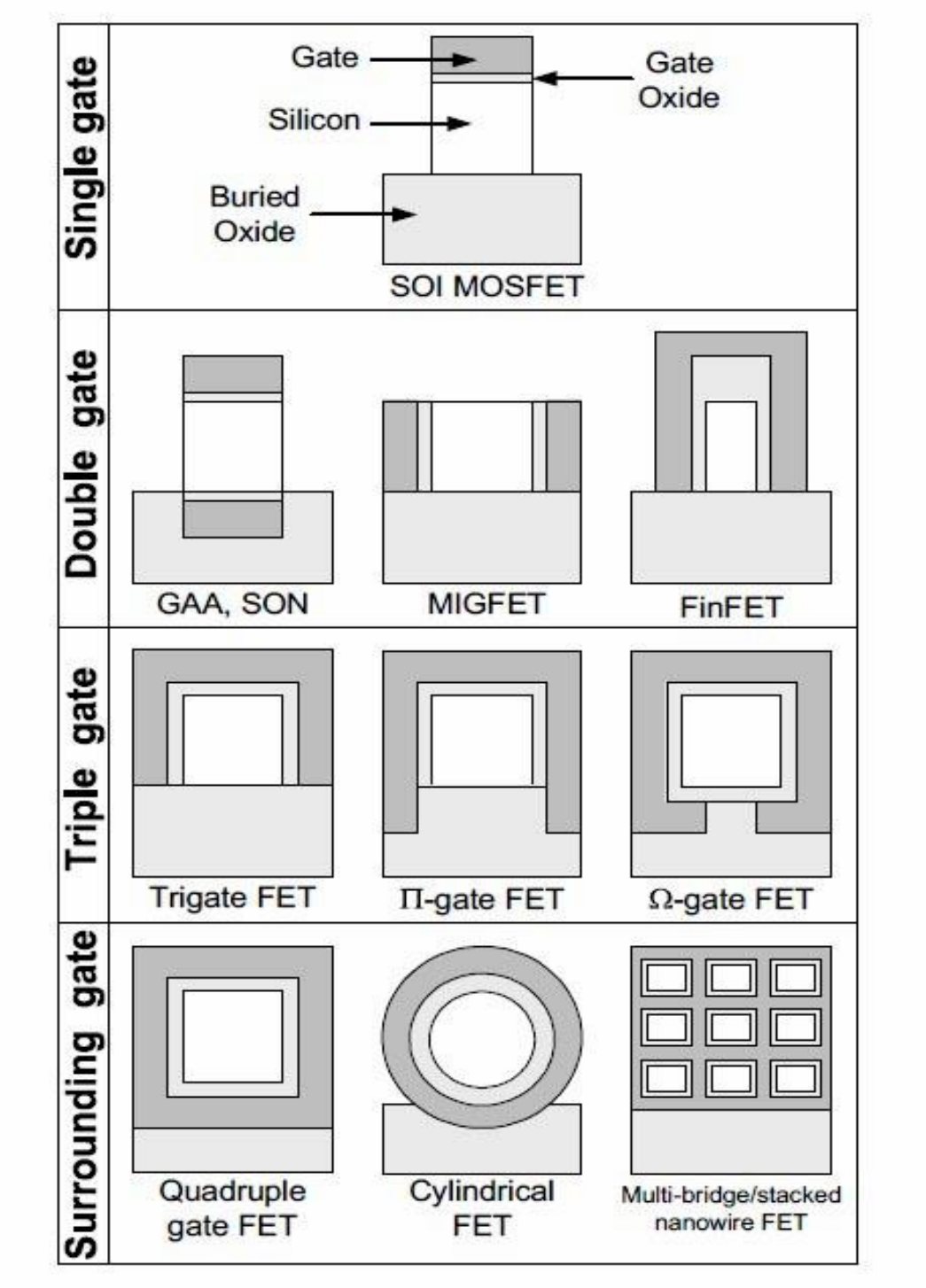

Fig.1.12: Different types of gate configuration in MOS structures to improve drive current and scalability of the MOS transistors [Colinge (2004)]

1.3.8 The Channel Doping Engineering

Doping is an important parameter for the performance optimization of the MOS devices. In general, the threshold voltage and carrier mobility are dependent on the channel doping concentration of the MOSFETs. The concept of uniform channel doping commonly assumed in the conventional MOS devices is a hypothetical one in practical MOS transistors due to the natural demand of some fabrication steps like diffusion and ion-implantation required for the threshold voltage adjustment of the device [Suzuki *et al.* (2007), Zhang *et al.* (2008)]. The ion-implantation technique results in Gaussian doping function in the channel. It may be also required to introduce non-uniform channel doping for engineering the performance characteristics of MOS transistors by changing the threshold voltage of the device. Among various doping profiles, the Gaussian function is perhaps the most general doping profile since a number of other doping profiles may be derived by changing the values of projected range (R_p) and straggle parameter σ_p of the Gaussian function $\left(N_g(x)\right)$ [Sze (1981), Zhang *et al.* (2008)] described as

$$N_g(x) = N_p \exp\left(-\left(\frac{x - R_p}{\sqrt{2}\sigma_p}\right)\right) \tag{1.3}$$

As per the designer requirement, the Gaussian channel profile may provide additional flexibility for performance optimization in terms of two additional parameters namely R_p and σ_p.

The channel electric field and potential distribution become two dimensional in nature at short channel lengths. In the subthreshold region, the channel potential and

threshold voltage could be derived by solving the Poisson's equation in the channel region. Several researchers have tried to obtain numerical as well as the analytical model for the threshold voltage of the FETs with a Gaussian channel profile [Pandey *et al.* 2004, Tiwari *et al.* (2010), Zhang *et al.* (2008)]. However, the non-analytic nature (i.e. non-integrable nature of the Gaussian function over any finite interval) puts a major hindrance in deriving analytical models of different performance parameters of the MOS transistors. In order to achieve closed form solutions for various device parameters, Dasgupta *et al.* [Dasgupta *et al.(*1987), Dasgupta *et al.*(1998)] approximated the function of Eq. (1.3) by an analytic Gaussian-like function given by:

$$N_g(x) \approx N_{GL}(x) = N_{pk}\, c\left(\left(a + 2b\alpha X\right)^2 - 2b\right)\exp\left(-a\alpha X - bX^2\right) \qquad (1.4)$$

where, $X = \frac{x - R_p}{x_b}$, R_p is the projected range, $x_b = \sqrt{2}\,\sigma_p$, σ_p is the straggle of Gaussian doping profile. N_{pk} is the peak doping at x = Rp; α = +1 for x > 0 and α = -1 for x < 0, a, b and c are fitting constants with values a = 1.786, b = 0.646 and c = 0.56.

Figure 1.13 compares the actual Gaussian function and Gaussian-like function. Except at the peak, both functions are found to be closely matched at other portions. Thus, researchers can safely use the Gaussian-like function described by Eq. (1.2) as the channel doping profile for the analytical modeling of various performance characteristics of advanced MOS transistors.

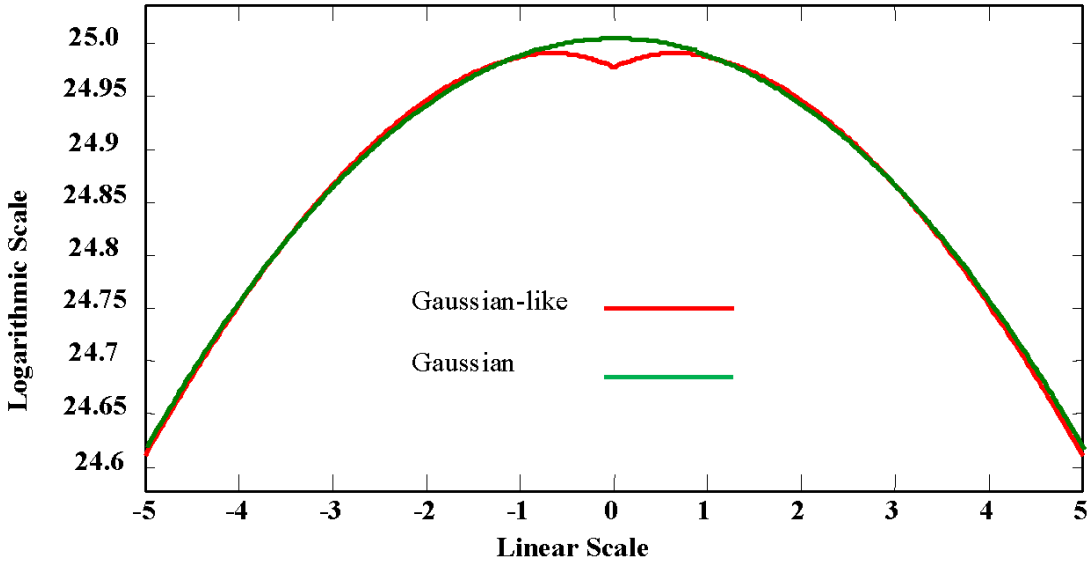

Fig 1.13: Gaussian function versus Gaussian-like function.

1.4 The Junctionless Field Effect Transistors (JLFETs): A Potential MOS Transistor for Future Generation Technology Scaling

The depletion regions formed at the source/channel and drain/channel junction restricts the scaling of MOS transistors since the channel length is required to be maintained greater than the sum of the above two depletion widths to avoid the "punchthrough" phenomenon. Clearly, scalability of the MOS transistors can be improved by reducing the widths of the source and drain depletion regions which can be achieved through increased substrate doping. However, the increased substrate doping decreases the mobility of channel carriers which has already been discussed earlier. Further, the reverse biased n^+-p junction at the drain side causes significant reverse biased leakage current in the MOS devices which in turn, increases the undesired power loss in the device. To increase the scalability of the MOS devices

with reduced leakage current, J.P. Colinge *et al.* [Colinge *et al.* (2010)] fabricated a new MOS transistor at Tyndall National Institute, Ireland in 2010 which was obtained by replacing the $\mathbf{n^+}$(source)-**p**(substrate)-$\mathbf{n^+}$(drain) of the conventional MOSFETs by $\mathbf{n^+}$(source)- $\mathbf{n^+}$(channel)-$\mathbf{n^+}$(drain) as shown in Fig. 1.3. Since the device uses a heavily doped semiconductor for all the source, channel and drain regions, the MOS transistor [Colinge *et al.* (2010)] is known as the Junctionless Field Effect Transistor (JLFET) in the literature. Clearly, the JLFETs require no junction formation for the source and drain regions, they are easier to fabricate over the conventional MOSFETs. Further, the device has better scalability and lower leakage current due to non-existence of depletion regions at the source/drain. Moreover, the device is free from the punch-through phenomenon.

The working principles of the JLFETs are entirely different from those of the conventional junction-based MOS transistors where a surface conduction path is formed at the gate-oxide/substrate interface by the inversion of the substrate material [Colinge *et al.* (2010)]. In the JLFETs, the large difference between the work functions of the gate material and semiconductor channel is maintained to make the channel region fully depleted in the Off-state of operation of the device. The objective of applying a suitable gate voltage is to convert the channel region from the fully depleted to a partially/zero depleted region so that it can work as a semiconductor resistor under operation. Contrary to the surface conduction, the JLFETs uses the bulk conduction mechanism of the semiconductor. Thus, the bulk mobility degradation of the channel carriers due to various scattering mechanisms is smaller in JLFETs than the degradation of surface mobility in the conventional MOS

devices under high electric field [Colinge *et al.* (2010)]. In general, the entire channel is maintained to be fully depleted at the normal off state at zero gate voltage by maintaining a large difference in the gate-electrode material and the channel material. Since there are no free carriers in the channel, in the off-state, the JLFET results in negligible/low drain current in the off-state for a given drain voltage. However, when a gate voltage is above a certain voltage called the threshold voltage to convert the channel from the fully depleted to the partially/zero depleted, the device may result in a significant drain current for different drain voltages.

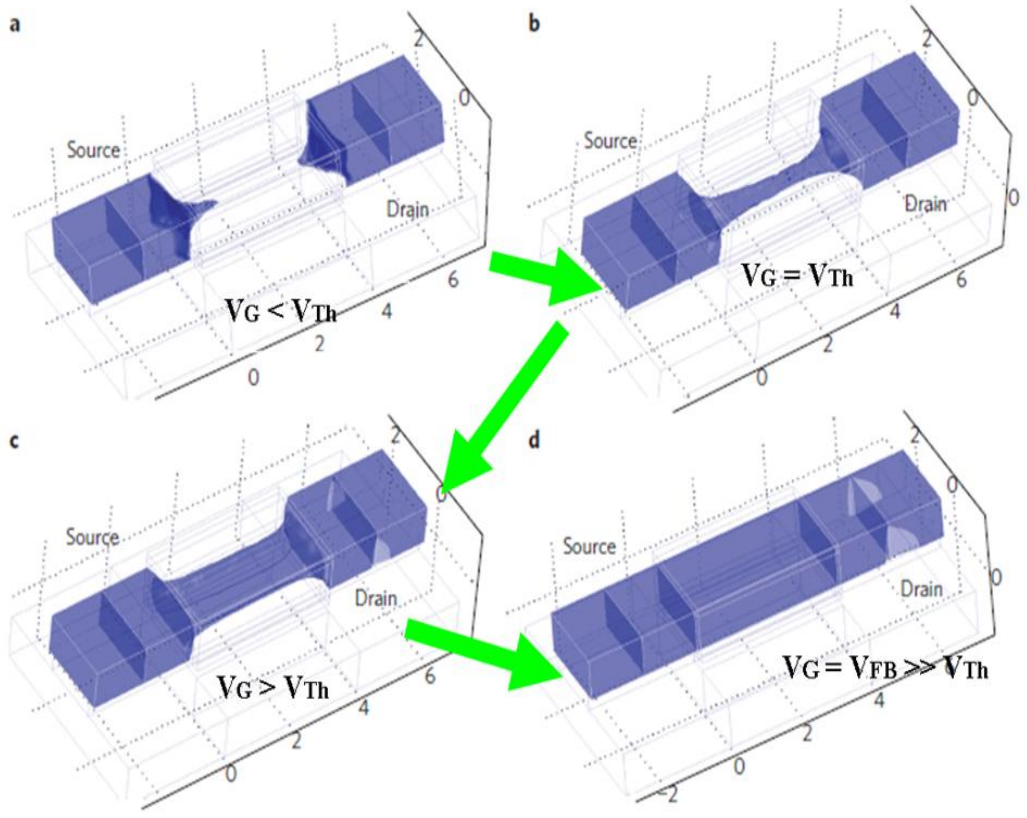

Fig1.14: Electron concentration contour plots in an n-type JLFET [Colinge *et al.* (2010)].

The working principle of the JLFET is illustrated in **Fig. 1.14**. Figure 1.14 (a) shows that there is no conduction path formation in between source and drain when the gate voltage is less than the threshold voltage of the device. The device enters into a partially depleted state to strat the current conduction when the gate voltage exceeds threshold as depicted in Fig. 1.14(b). The current conducting segment slowly increases with the increasing gate voltage until flat band condition is reached as shown in Fig 1.14 (c). When the gate voltage becomes equal to flat band voltage, the depletion region is disappeared completely and the channel becomes fully neutral as shown in Fig 1.14 (d). The accumulation of carriers starts for gate voltage beyond the flat band voltage [Colinge *et al.* (2011)].

Like the conventional MOSFETs, the nanoscaled JLFETs also suffer from the SCEs due to two dimensional electric field in the depleted channel region of the device. Thus, the multiple gate structures discussed in Subsection 1.3.7 can be used in the JLFETs to improve the scalability and SCEs of the devices. The double gate (DG) is the simplest multiple gate MOS structure introduced by T.Sekigawa and Y.Hayashi in 1984 [Sekigawa and Hayashi (1984)]. Since then, the DG MOS structure has been widely explored in the CMOS technology scaling [Wong (2001), Fiegna *et al.* (1992.), Frank *et al.* (1992)] due to its better scalability, enhanced mobility, better switching characteristics, higher drive current and higher transconductance and linearity as compared to the single gate structures. Because of various merits of the DG MOS structures, few researchers [Chiang (2012), Gnani *et al.* (2012)] have studied the DG JLFET structure shown in Fig.1.3.

1.5 State-of-the-Art-Works of JLFETs

We have already mentioned that multiple gate structures can also be used in JLFETs to improve the scalability and SCEs of the device. Double gate Junctionless field effect transistor (DG-JLFET) is one of the potential MOS structures for future generation technology scaling. In view of the above, the present thesis aims to develop some theoretical models for the subthreshold characteristics of the DG JLFETs. Before describing the scopes of the thesis, we would like to review some important state-of-the-art-research works reported in the area of JLFETs which are described briefly in the following subsections.

1.5.1 Review of Some Simulation-Based Study on JLFETs

As discussed earlier that the JLFET has been the topic of research as a promising MOS transistor since its introduction by Colinge *et al.* [Colinge *et al.* (2010)] in 2010. The device has drawn special interests due its lower leakage current, better subthreshold swing, lower mobility degradation (due to bulk conduction) and lower electric field perpendicular to the current flow than those of the conventional inversion mode MOSFETs [Lee et al (2009a), Lee *et. al.*(2009b), Colinge *et. al.* (2010a), Colinge et al (2010b), Lee *et. al.*(2010)]. The conduction mechanism, threshold voltage variation with device dimensions and intrinsic device performance of Junctionless nanowire transistor (JNT) have been analyzed by Colinge *et. al.* [Coling *et al.* (2011), Gnani *et al.* (2011)]. They [Coling *et al.* (2011)] have shown that the device has nearly ideal subthreshold swing with smaller DIBL and larger electron mobility over other structures. However, it has large variation in the

threshold voltage, on-state current, subthreshold leakage current and drain induced barrier lowering due to random dopant fluctuation [G. Leung and C. O. Chui (2012), Taur *et al.*(2012), Gnudi *et al.*(2012)]. Su *et al.* [Su *et al*. (2011)] have reported that the JLFETs have higher ON/OFF current ratio and lower series resistance of source/drain as compared to the inversion mode FETs. Based on a simulation study of a Junctionless Gate-all-around Si nanowire device with 3.1 nm channel length and 1.2 nm diameter, Ansari et al. [Ansari *et al*. (2010)] have demonstrated that the device can work well at this channel length with good subthreshold characteristics, good electrostatic control over the channel and excellent On-to-Off current ratio of ~10^6. This shows that the device may be scaled in the sub-5nm regime without significant performance degradation.

Doria *et al.* [Doria *et al.*(2011)] have investigated the analog performance of N-channel multigate Junctionless transistor and compared their results with inversion mode multigate MOSFET of same dimensions. They [Doria *et al.(2011)*] have investigated the effect of temperature and fin width on the analog performance of the device. They [Doria *et al*.(2011)] observed higher early voltage and intrinsic gain than the conventional multigate MOSFETs. However, the variations of early voltage and intrinsic gain with fin width are observed to be more sensitive in multigate JLFETs than those of the trigate MOSFETs.

Mondal *et al.* [Mondal *et al.* (2013)] reported a JL-FET in silicon-on-insulator (SOI) with a vertical Gaussian doping profile in the channel with the maximum concentration at the top and minimum concentration in the bottom of the device. In an another study, Mondal *et al.* [Mondal *et al.(*2015)] have also investigated the subthreshold characteristics of the JLFETs with a vertical Gaussian doping profile

[Mondal *et al.(*2015)]. They have observed that the ON to OFF state current ratio can be optimized by optimizing the Off state current of the device by controlling the doping concentration in the channel.

All the reported works discussed so far are based on simulation studies. However, it is always important to develop theoretical models for the better physical insight of the devices. Therefore, we will now review some important state-of-the-art-research works on the theoretical modeling of electrical characteristics of the DG JLFETs in the following subsections.

1.5.2 Review of Modeling of Long Channel DG JLFETs

Duarte *et al.* [Duarte *et al.*(2011)] proposed the bulk conduction current model of long channel DG-JLFETs by solving the one dimensional Poisson's equation for channel potential. They [Duarte *et al.*(2011)] have approximated the depletion width by Taylor's expansion at threshold voltage point to model the subthreshold bulk conduction current of the device.

Gnani *et al.* [Gnani *et al.* (2012)] have reported an improved depletion approximation by using the Boltzmann statistics based solution of the Poisson's equation. They modelled the drain current using gradual channel approximation. Finally, they used drain current model to calculate the subthreshold swing and threshold voltage.

Chen *et al.* [Chen *et al*. (2012)] have derived a surface potential model of symmetric long channel DG JLFETs for full depletion, partial depletion, and accumulation conditions. They have modelled the drain current using the Pao–Sah's integral which

is valid for all the subthreshold, linear and saturation regions. The model results are validated by comparing them with the TCAD simulation data.

An analytical drain current model based on depletion approximation has been derived by Sahu, *et al.* [Sahu *et al.* (2014)] for long channel DG JLFETs. They have defined the threshold voltage as the gate voltage at which the depletion width becomes equal to half of the channel thickness so that no current flows between the source and drain at this gate voltage. Finally, they have obtained the drain current formula by integrating the mobile charge density from source to drain region.

For long channel DG JLFETs, a charge based analytical model for surface and center potential has been developed by Cerderia *et al.* [Cerderia *et al.* (2013)]. The relation between surface potential and gate voltage has been calculated numerically.

Jin *et al.* [Jin *et al.* (2013)] have proposed the unified continuous drain current models for both the DG JLFET and conventional inversion mode MOSFETs. They have assumed that the Poisson's equation at zero charge density in the channel of the JLFETs can represent Poisson's equation of the inversion mode MOSFETs. They have assumed the potential function proposed by Taur *et al*. [Taur *et al.* (2004)] which is then put in the Poisson's equation to obtain an approximated solution for the channel potential of the DG JLFET. The channel potential model is then used to finally derive the drain current model of the DG JLFETs.

Sallese *et al*. [Sallese *et al.* (2011)] and Duarte *et al.* [Duarte *et al* (2011)] have proposed charge based analytical models for the drain current and charge density for the long channel DG-JLFETs which are valid for the subthreshold, linear and

saturation regimes of operations of the device. Both the models are shown to be in good agreement with the TCAD simulation results.

Lime *et al.* [Lime *et al.* (2013)] have proposed a simple and compact model for the charge density of the symmetrical long channel DG-JLFETs. They have obtained the charge density by integrating the Boltzmann's distribution. They have shown that the mobile charge density has a Gaussian distribution in the middle of the channel when the channel potential is approximated as parabolic function in the full depletion mode. They have linked the mobile charge density to the difference between center and surface potential using boundary conditions. They have derived some appropriately approximated analytical solutions for the charge density in depletion and accumulation modes. Finally, due to discontinuity problem between depletion and accumulation mode, they have modelled the drain current by trial and error method.

A compact model for the quantum electron density of the long channel DG JLFETs in the subthreshold regime has been proposed by Duarte et al. [Duarte et al. (2012)]. Ignoring the mobile charge carrier in the subthreshold region, they have decoupled the Schrödinger equation from the Poisson's equation. Using this assumption, they have modelled the center potential and threshold voltage by following the method described by Sallese *et al.* (2011) [Sallese *et al.* (2011)] and Duarte *et al.* (2011) [Duarte *et al.* (2011)]. They have shown that the threshold voltage shift due to quantum confinement effect is higher in DG JLFETs than that in the conventional inversion DG MOSFETs at higher channel thickness. However, the shift in the

threshold voltage is lower in DG JLFETs than that of the inversion mode DG MOSFETs for lower channel thickness.

Hwang *et al.* [Hwang *et al.* (2015)] have derived an analytical model of channel potential for long channel DG JLFETs in depletion, partial depletion, and accumulation regimes of operations of the device. With the help of the central potential and surface potential, they have derived an expression for the mobile charge carriers using the parabolic approximation of potential in the perpendicular direction of the channel length. They have also derived an expression for the electric field in the channel direction. Finally, they have derived the expression for the drift current and diffusion currents in the channel.

Jazaeri *et al.* have reported the trans-capacitance modeling of long channel DG JLFETs and gate-all-around nanowire JLFETs [Jazaeri *et al.* (2013), Jazaeri *et al.* (2014)]. They have derived an analytical charge based trans-capacitance model valid for the linear to saturation regions (i.e., from deep depletion region to accumulation region). The analytical expression of the charge densities at source, drain, and gate are used to model the intrinsic capacitance network which is the very basic step for AC analysis of circuits based on JLFETs.

1.5.3 Review of Modeling of Short-Channel DG-JLFETs

In short-channel DG-JLFETs, the channel potential distribution and electric field become inevitably two-dimensional in nature. Under subthreshold conditions, the channel potential is derived by solving the two-dimensional (2D) Poisson's equation in the channel region. The threshold voltage, subthreshold current and subthreshold

swings are the key parameters of the MOS transistors for determining the static power dissipation and switching characteristics of the transistor acting as a switch. Thus, accurate models for the threshold voltage, subthreshold current and the subthreshold swing of DG-JLFETs are main concern of many researchers for the optimization of subthreshold characteristics of the device for VLSI/ULSI circuits. We will now review some important literatures related to the modeling of subthreshold characteristics of short-channel DG-JLFETs as discussed below.

A number of theoretical models dealing with the subthreshold characteristics of DG-JLFETs have been reported in the literature. Chiang [Chiang (2012)] has proposed a bulk conduction based quasi-2D threshold voltage model for the short channel DG-JLFET for the first time. He [Chiang (2012)] has obtained the channel potential function of the device by solving the 2D Poisson's equation by using parabolic approximation. Chiang [Chiang (2012)] has defined the threshold voltage of the DG JLFET as the gate voltage at which the minimum central potential is equal to zero. The effects various device parameters such as gate oxide thickness, drain bias, channel length, and channel thickness on the threshold voltage have been discussed. The proposed model is shown to be extended for both the accumulation mode/inversion mode operations of DG-JLFETs and junction based conventional DG-MOSFETs. The model results are validated by comparing them with the TCAD simulation results.

A number of researchers [Jin *et al*. (2012), Lin *et al*.(2012), Jin *et al.* (2013)] have solved the 2D Poisson's equation by using the evanescent mode analysis to obtain the 2D channel potential distribution function of the short-channel DG JLFETs. In this method, the 2D Poisson's equation is assumed to be the summation of the 1D

Poisson's equation of long channel devices and 2D Laplace's equation. The proposed channel potential method [Jin *et al.* (2012), Lin et al. (2012), Jin *et al.* (2013] has then been used to model the subthreshold characteristics of DG-JLFETs. Jin *et al.* [Jin *et al.* (2012), Jin *et al.* (2013)] have proposed the modeling of subthreshold current and subthreshold swing with good agreement of their model results with the simulation data. Lin *et al.* [Lin *et al.* (2012)] have reported analytical models for the channel potential, threshold voltage, subthreshold current and subthreshold swing. They [Lin *et al.* (2012)] have defined the threshold voltage as the gate voltage at which the minimum central potential is equal to $V_T \ln\left(\frac{N_D}{M_{cric} n_i}\right)$, where, V_T is the thermal voltage, N_D is the channel doping and $M_{cric} \times n_i$ is the critical value of electron density. They [Lin *et al.* (2012)] have shown that $M_{cric} \times n_i$ is typically about one or two orders in magnitude lower than the doping density (N_D). Their [Lin *et al.* (2012)] model results for the threshold voltage roll-off, subthreshold current, and subthreshold swing have been validated with TCAD simulation results.

Holtij *et al.* [Holtij *et al.* (2012), Holtij *et al.* (2013), Holtij *et al*. (2014)] have published a number of articles on the subthreshold characterstics of the short channel DG-JLFETs. They [Holtij *et al.* (2012), Holtij *et al.* (2013)] have developed the 2D channel potential model by solving the 2D Poisson's equation using evanescent method alongwith the Schwarz–Christoffel conformal mapping technique [Holtij *et al.* (2012)]. The gate voltage at which the minimum channel central potential becomes equal to the Fermi potential has been considered to be the threshold voltage of the device. In an another work, Holtij et al. [Holtij et al(2014)] have used the

channel potential for developing simple models for the threshold voltage and subthreshold swing. With the help of Lambert's W-function and a smoothing function for the transition between the depletion and accumulation regions, they have also reported a unified charge model for depletion to accumulation regions.

Gnudi *et al.* [Gnudi *et al.* (2013)] have reported a parabolic approximation based 2D semianalytical model for the electrostatic channel potential and subthreshold current of symmetric DG-JLFETs by considering the source/drain depletion effects. They have solved the drift-diffusion drain transport equation for the subthreshold current of the device. They have also modelled the subthreshold swing and DIBL of the DG JLFETs.

Kumari *et al.* [Kumari *et al.* (2015)] have reported the 2D analytical modeling of subthreshold current of DG-JLFETs by considering the fringing fields from the gate to source/drain region using conformal mapping technique. They have included the effect of band gap narrowing due to heavy channel doping in their proposed model. The threshold voltage roll-off, subthreshold swing and DIBL have also been modeled by Kumari *et al.* [Kumari *et al.* (2015)]. The model results have been shown to be closely matched with the simulation results.

Jiang *et al.* [Jiang *et al*. (2015)] have proposed an analytical model for the channel potential of short channel DG-JLFETs by solving the 2D Poisson's equation by series expansion method. The potential function is then used for developing the models for the threshold voltage, subthreshold swing, and subthreshold current of the DG-JLFETs. They have also modelled the subthreshold current using similar method as proposed by Gnudi *et al.* [Gnudi *et al.* 2013]. The results obtained from the

analytical model have been shown to be in good agreement with the simulation results.

Woo *et al.* [Woo *et al.* (2013)] have reported an analytical model for the channel potential and threshold voltage by considering the localized charge effects [Jean *et al.* (1997), Kang *et al.*] near the drain side.

A number of researchers [Wang *et al.* (2014), Kumari *et al.* (2015)] have also reported the modelling of the electrostatic channel potential of double material (DM) DG-JLFETs by solving 2D Poisson's equation using the evanescent mode analysis [Monroe and Hergenrother (1998) Chen et al.(2002), Dubey et al.(2010)]. From the current continuity equation and 2D channel potential, they have derived the subthreshold current and subthreshold swing models of the DM DG-JLFETs by neglecting the length of the source and drain regions. The model proposed by Kumari *et al.* [Kumari *et al.* (2015)] has been developed by assuming Schottky source/drain contacts. The effects of different device parameters such as the channel thickness, gate oxide thickness, and ratio of two gate lengths on the subthreshold current and subthreshold swing have been discussed.

Agrawal *et al.* [Agrawal *et al.* (2015)] have reported the 2D modeling of the surface potential of DM-DG-JLFETs for full depletion, partial depletion, and accumulation operating modes of the device. The channel potentials in the full depletion and partial depletion modes of operation of the device have been modelled by following the method proposed by Chiang [Chiang (2012)]. They have also proposed a model for determining the depletion thickness of the channel. Finally, they [Agrawal *et al.*

(2015)] have solved the Poisson's equation by using Taylor' series approximation for the potential function in the accumulation region of operation of the device.

1.5.4 Summary of the Literature Survey: Motivation Behind the Present Thesis

We have reviewed some important state-of-the-art-research works reported in the literature related to the modeling and simulation of JLFETs. In this section, we will summarize some important observations outlined as follows:

- The JLFETs [Lee et al (2009a), Lee *et. al.*(2009b), Colinge *et. al.* (2010a), Colinge et al (2010b), Lee *et. al.*(2010)] are considered to be the important MOS structures with better scalability and higher speed over the conventional MOSFETs due to the absence of source(drain)/channel depletion region and higher carrier mobility respectively. In addition, the JLFETs possess (i) lower thermal budget, (ii) better (near-ideal) subthreshold swing, (iii) lower degradation of mobility with gate voltage, (iv) lower electric field perpendicular to current flow, (v) lower DIBL, and (vi) better possibility of the device for RF and analog applications [Doria et al (2011)] over the conventional inversion mode based MOSFETs. The above mentioned advantages of JLFETs may make it suitable for low-power high-speed digital logic and analog circuit applications [Colinge *et. al.* (2010)].
- Non-uniform body doping offers additional degrees of freedom for optimizing the threshold voltage [Tour et al (1998)]. For example, besides the peak doping concentration, the projected range and straggle parameter of the

ion implanted Gaussian doping profile [sze (1983), Suzuki *et al.(*2007)] can also be explored for the performance optimization of various non-classical MOS transistors [Dubey et al.(2010), Mondal *et al.* (2013), Mondal *et al.* (2015)].

- Due to retrograde channel doping in the vertical channel engineering [Yu *et al.* (2001)], the original implanted ions get altered after thermal annealing and the annealed profile becomes uniform in the lateral direction and non-uniform in the vertical direction [Zhang et al(2008)]. Based on the above facts, some simulation based works have been reported in the literature [Mondal et al (2013), Mondal et al(2015)] for studying the effects of the profile parameters of a vertical Gaussian doping profile on the performance of JLFETs. However, to the best of our knowledge, no theoretical investigation has been carried out for modeling the subthreshold characteristics the short-channel DG-JLFETs with a ion-implanted vertical Gaussian profile.
- The major difficulty in modeling the subthreshold characteristics of any MOS transistor using a Gaussian doping profile in the channel is the non-integrable nature of the Gaussian function over any finite interval. Thus, many researchers [Dubey *et al.*(2010), Goel *et al.* (2016)] have replaced the actual non-analytic Gaussian function by an analytic Gaussian-like doping function originally proposed by Dasgupta et al [Dasgupta et al.(1986)].
- A number of different models have been reported for the threshold voltage of the short-channel DG-JLFETs [Chiang (2012), Lin *et al.* (2012), Holtij *et al.* (2012), Holtij *et al.* (2013), Gnudi *et al.* (2013), Woo *et al.* (2013), Wang *et al.* (2014), Agrawal *et al.* (2015)] by assuming a uniformly doped channel.

However, to the best of our knowledge, no significant model has been reported so far for the threshold voltage of short-channel DG JLFETs with a non-uniform channel doping. Thus, there is a need for developing an analytical threshold voltage model for DG-JLFETs with a non-uniform doping profile (e.g. the Gaussian-like profile) in the channel.

- A number of models have been reported on the subthreshold current [Lin *et al*. (2012), Jin *et al.* (2013), Gnudi *et al.* (2013)] and subthreshold swing [Lin *et al.* (2012), Jin et al(2012), Jin et al (2013) , Gnudi *et al.* (2013), Kumari et al (2015)] of uniformly doped short-channel DG-JLFETs by using the surface potential function obtained by solving the 2D Poisson's equation in the channel depletion region. However, to the best of our knowledge, no work has yet been reported on the modeling of the subthreshold current and subthreshold swing of the short-channel DG-JLFETs with a non-uniformly doped channel. Thus, there are ample scopes of work in developing analytical models for the subthreshold current and subthreshold swing characteristics of the DG-JLFETs with different non-uniform channel doping profiles including the vertical Gaussian-like doping profile [Dasgupta et al.(1986)].
- It has been reported that the dielectric pockets can be used to control the subthreshold characteristics of the MOSFETs by controlling the SCEs [Shih *et al.* (2004), Jayanarayanan *et al.* (2009), Kumari *et al.* (2012)]. However, to the best of our knowledge, no work has been reported so far to investigate the effects of dielectric pocket engineering on the subthreshold characteristics of DG JLFETs. Thus, there are ample scopes for analytical modeling of the subthreshold characteristics of DG JLFETs with dielectric pocket engineering

for controlling the SCEs.

In brief, there is a lot of opportunity in the modeling and simulation of the subthreshold characteristics of DG-JLFETs with Gaussian channel doping engineering as well as dielectric pocket engineering for future generation technology nodes. Based on the above observations from the literature, the scopes of the present thesis have been outlined in the following section.

1.6 Scopes and Chapter Outline of the Thesis

The objective of the present thesis is to present the analytical modeling and simulation of subthreshold characteristics in terms of the threshold voltage, subthreshold current and subthreshold swing of the short-channel DG JLFETs with channel doping engineering and dielectric pocket engineering. Based on the observations of the literature survey summarized in the Section 1.6, the scopes of this thesis have been outlined in Chapter-2, Chapter-3, Chapter-4 and Chapter-5 while the Chapter-6 includes the overall summary and conclusion of the thesis. Excluding Chapter-1 (i.e. the present chapter), the remaining FIVE chapters out of the total SIX chapters of the present thesis are outlined as follows:

Chapter-2 presents the analytical modeling and simulation of the channel potential and threshold voltage of short channel DG-JLFETs with a vertical Gaussian-like doping profile in the channel region of the device. The two-dimensional (2D) Poisson's equation in the channel region has been solved by using the evanescent mode of analysis to model the 2D channel potential distribution of the device. The derived 2D channel potential is used to model the effective conduction path

parameter which is then explored to model the threshold voltage for DG-JLFETs under study. The effects of various doping profile parameters as well as other device parameters on the threshold voltage have been investigated in details. All the results obtained from the modeling have been compared with the numerical simulation data obtained by using the commercially available ATLAS ™ 2D device simulator.

Chapter-3 reports the modeling of the subthreshold current and subthreshold swing of short channel DG-JLFETs with the vertical Gaussian-like doping profile in the channel region considered in **Chapter-2**. The effects of parameters such as gate length, straggle parameter, oxide thickness and channel thickness on the subthreshold current and subthreshold swing have been demonstrated. The proposed model results have been validated by comparing them with the ATLAS ™ based TCAD simulation data.

Chapter-4 presents the analytical modeling of the channel potential and threshold voltage of the dielectric pocket (DP) DG-JLFETs with a uniform channel profile. In this case, the two dielectric pockets are used at the source and drain sides to control the opening of source/channel and drain-channel junctions. The length and thickness of the dielectric pockets provide additional flexibilities for optimizing the subthreshold characteristics of the DG-JLFETs. The channel potential has been derived by solving the 2D Poisson's equation with suitable boundary conditions following the evanescent mode of analysis as used in **Chapter-2**. The effects of source and drain depletion regions have been included for improving the accuracy of the model. The derived channel potential has then been used to model the threshold voltage of the device. The effects of dielectric pocket (DP) length and thickness on

channel potential, threshold voltage and drain induced barrier lowering have been investigated. The proposed model results have been compared with the ATLAS ™ based TCAD simulation results to validate the proposed models of the DP DG-JLFETs studied in this chapter.

Chapter-5 deals with the modeling of the subthreshold current and subthreshold swing of DP DG-JLFETs considered in **Chapter-4**. The effects of DP length and thickness as well as other device parameters on the subthreshold current and subthreshold swing have been discussed. Finally, the model results have been validated by comparing them with the TCAD simulation results obtained by using the commercially available ATLAS ™ 2D device simulation software.

Chapter-6 includes the summary and conclusions of the thesis. The major findings of the present study are summarized in this chapter. Finally, the possible future scopes of research in the related area of the present thesis are presented at the end of this chapter**.**