

LIST OF FIGURES

Fig 1.1(a):	Intel scaling trends and logic area scaling	2
Fig 1.1(b):	Intel innovation-enabled technology pipeline [Intel and Nikon Technologists Assess Status and Future of Lithography (2017)]	3
Fig 1.2:	Schematic illustration of the constant field scaling of Si technology by a scaling factor “k” [Taur and Ning (1998)]	5
Fig 1.3:	Cross-sectional view of DG JLFET	8
Fig 1.4:	Energy band diagram for n-channel MOSFET between source and drain in off-state to describe the threshold voltage roll-off. [Taur and Ning (1998)].	10
Fig 1.5(a):	Cross sections view of small channel and long channel MOSFETs [Streetman (2009)].	12
Fig 1.5(b):	Conduction band edge along the channel length for a short channel and long channel MOSFET [Streetman (2009)].	12
Fig 1.6:	Schematic illustration of channel length modulation effect [Arora (2007)].	13
Fig 1.7:	Schematic view of Punchthrough phenomena in a MOSFET [Arora (2007)]	14
Fig 1.8:	Cross-section of a MOSFET showing hot-carrier effects	15
Fig 1.9:	Schematic diagram of the LDD MOSFET [Kumar (2000)].	20
Fig 1.10:	Schematic view of the halo MOSFET	20
Fig 1.11	Cross-sectional view of DP-MOSFET [Jurczak <i>et al.</i> (2001)].	22
Fig 1.12	Different types of gate configuration in MOS structures to improve drive current and scalability of the MOS transistors [Colinge (2004)]	25
Fig 1.13	Gaussian function versus Gaussian-like function	28
Fig 1.14:	Electron concentration contour plots in an n-type JLFET [Colinge <i>et al.</i> (2010)].	30
Fig 2.1:	Simplified two-dimensional schematic view of DG- JLFET.	51
Fig 2.2:	The simulated view of Gaussian doped DG-JLFET.	51
Fig 2.3:	Simulation model calibration against non-planar JLFET experimental $I_{DS} - V_{GS}$ data from [Colinge <i>et al.</i> (2010)].	62

Fig 2.4:	Conduction path potential variation along channel length for various straggle.	63
Fig 2.5:	Conduction path potential variation along channel length for various doping concentration.	63
Fig 2.6:	Conduction path potential variation for short channel length at different drain voltages.	64
Fig 2.7:	Conduction path potential variation for long channel length at different drain voltages.	65
Fig 2.8:	Threshold voltage variation with channel length for different straggle.	66
Fig 2.9:	Threshold voltage variation with channel length for different drain voltages.	66
Fig 2.10:	Threshold voltage variation with channel length for different silicon thicknesses (t_{si}).	68
Fig 2.11:	Threshold voltage variation with channel length for different oxide thicknesses.	68
Fig 2.12:	Threshold voltage variation with channel length for different peak doping concentrations.	69
Fig 2.13:	DIBL variation with channel length for different straggle.	70
Fig 3.1:	Simplified two-dimensional cross-sectional view of DG- JLFET.	74
Fig 3.2:	Subthreshold current variation with gate-to-source voltage for different gate lengths.	79
Fig 3.3:	Subthreshold current variation with gate-to-source voltage for different straggle parameter.	80
Fig 3.4:	Subthreshold current versus gate-to-source voltage for different oxide thickness.	80
Fig 3.5:	Subthreshold current versus gate-to-source voltage for different peak doping concentration.	81
Fig 3.6:	Subthreshold current versus gate-to-source voltage for different channel thickness.	82
Fig 3.7:	Subthreshold current versus gate-to-source voltage for different projected range (R_p).	82
Fig 3.8:	Subthreshold swing versus device channel length for different channel thicknesses.	83

Fig 3.9:	Subthreshold swing versus device channel length for different gate oxide thicknesses.	84
Fig 4.1:	Simplified two-dimensional cross-sectional view of DP-DG-JLFET.	87
Fig 4.2:	Simulation model calibration against non-planar JLFET experimental $I_{DS} - V_{GS}$ data from [Colinge <i>et al.</i> (2010)].	97
Fig 4.3:	Central potential variations versus position along channel for various pocket length at $L = 20 \text{ nm}$, $t_{ox} = 1.5 \text{ nm}$, $t_{si} = 10 \text{ nm}$, $T_{side} = 7 \text{ nm}$, $V_{gs} = 0.1 \text{ V}$ and $V_{ds} = 0.1 \text{ V}$.	98
Fig 4.4:	Central potential variations versus position along the channel for various pocket thickness at $L = 20 \text{ nm}$, $t_{ox} = 1.5 \text{ nm}$, $t_{si} = 10 \text{ nm}$, $\frac{t_{si}}{2} - a = 3 \text{ nm}$ $V_{gs} = 0.1 \text{ V}$ and $V_{ds} = 0.1 \text{ V}$.	99
Fig 4.5:	Threshold voltage variation with channel length for different pocket length at $t_{ox} = 1.5 \text{ nm}$, $t_{si} = 10 \text{ nm}$, $T_{side} = 7 \text{ nm}$, $V_{gs} = 0.1 \text{ V}$ and $V_{ds} = 0.1 \text{ V}$.	99
Fig 4.6:	Threshold voltage variation with channel length for different pocket thickness at $t_{ox} = 1.5 \text{ nm}$, $t_{si} = 10 \text{ nm}$, $\frac{t_{si}}{2} - a = 3 \text{ nm}$ $V_{gs} = 0.1 \text{ V}$ and $V_{ds} = 0.1 \text{ V}$.	100
Fig 4.7:	DIBL variation with channel length for different pocket length at $t_{ox} = 1.5 \text{ nm}$, $t_{si} = 10 \text{ nm}$, $T_{side} = 7 \text{ nm}$, $V_{ds1} = 0.1 \text{ V}$ and $V_{ds2} = 1.1 \text{ V}$.	101
Fig 4.8:	DIBL variation with channel length for different pocket thickness at $t_{ox} = 1.5 \text{ nm}$, $t_{si} = 10 \text{ nm}$, $V_{ds1} = 0.1 \text{ V}$, $V_{ds2} = 1.1 \text{ V}$ and $\frac{t_{si}}{2} - a = 3 \text{ nm}$.	101
Fig 5.1:	Simplified two-dimensional schematic view of DP-DG-JLFETs.	105
Fig 5.2:	Variation of subthreshold current against gate-to-source voltage for different DP lengths at $t_{ox} = 1.5 \text{ nm}$, $t_{si} = 10 \text{ nm}$, $T_{side} = 7 \text{ nm}$, $V_{ds} = 0.1 \text{ V}$.	110
Fig 5.3:	Variation of subthreshold current against gate-to-source voltage for different DP thicknesses $t_{PL} = 3 \text{ nm}$, $t_{ox} = 1.5 \text{ nm}$, $t_{si} = 10 \text{ nm}$, $V_{ds} = 0.1 \text{ V}$.	110
Fig 5.4:	Subthreshold current variation with gate-to-source voltage for different gate lengths at $t_{PL} = 3 \text{ nm}$, $t_{ox} = 1.5 \text{ nm}$, $t_{si} = 10 \text{ nm}$,	111

$$T_{side} = 7 \text{ nm}, V_{ds} = 0.1 \text{ V}.$$

- Fig 5.5:** Subthreshold current versus gate-to-source voltage for different oxide thickness at $t_{PL}=3\text{nm}$, $t_{si}=10\text{nm}$, $T_{side}=7\text{nm}$, $V_{ds}=0.1\text{V}$, $L=20\text{nm}$. **111**
- Fig 5.6:** Subthreshold current versus gate-to-source voltage for different doping concentration at $t_{PL}=3\text{nm}$, $t_{si}=10\text{nm}$, $T_{side}=7\text{nm}$, $V_{ds}=0.1\text{V}$, $L=20\text{nm}$, $t_{ox}=1.5\text{nm}$. **112**
- Fig 5.7:** Subthreshold current versus gate-to-source voltage for different channel thickness at $t_{PL}=3\text{nm}$, $t_{si}=10\text{nm}$, $T_{side}=7\text{nm}$, $V_{ds}=0.1\text{V}$, $L=20\text{nm}$, $t_{ox}=1.5\text{nm}$. **113**
- Fig 5.8:** Variation of subthreshold swing against gate-to-source voltage at $t_{PL}=3\text{nm}$, $t_{si}=10\text{nm}$, $T_{side}=7\text{nm}$, $V_{ds}=0.1\text{V}$, $L=20\text{nm}$, $t_{ox}=1.5\text{nm}$. **114**
- Fig 5.9:** Variation of subthreshold swing against gate-to-source voltage at $t_{PL}=3\text{nm}$, $t_{si}=10\text{nm}$, $T_{side}=7\text{nm}$, $V_{ds}=0.1\text{V}$, $L=20\text{nm}$, $t_{ox}=1.5\text{nm}$. **115**