List of Publications

Journal Papers:

- S. Chatterjee and K. Sarawadekar, "An Optimized Architecture of HEVC Core Transform using Real-valued DCT Coefficients," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 12, pp. 2052-2056, Dec 2018.
- S. Chatterjee and K. Sarawadekar, "WHT and Matrix Decomposition Based Approximated IDCT Architecture for HEVC," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 6, pp. 1043-1047, June 2019.
- S. Chatterjee and K. Sarawadekar, "Approximated Core Transform Architectures for HEVC Using WHT Based Decomposition Method," in IEEE Transactions on Circuits and Systems–I: Regular Papers, accepted for publication.
- S. Chatterjee and K. Sarawadekar, "Exploiting Trigonometric Properties to Optimize Higher Order DCT Architecture in HEVC," in IEEE Transactions on Circuits and Systems for Video Technology, revised and resubmitted.
- S. Chatterjee and K. Sarawadekar, "A Constant Throughput Integer DCT VLSI Architecture for HEVC," - to be communicated.

Conference Papers:

- S. Chatterjee and K. Sarawadekar, "Constant throughput HEVC core transform design," in IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), Abu Dhabi, 2016, pp. 1-4, doi: 10.1109/MWSCAS.2016.7870111.

- S. Chatterjee and K. Sarawadekar, "A low cost, constant throughput and reusable 8×8 DCT architecture for HEVC," in IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), Abu Dhabi, 2016, pp. 1-4, doi: 10.1109/MWSCAS.2016.7869994.